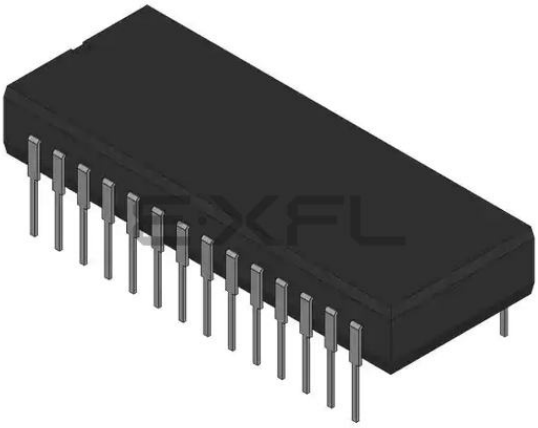

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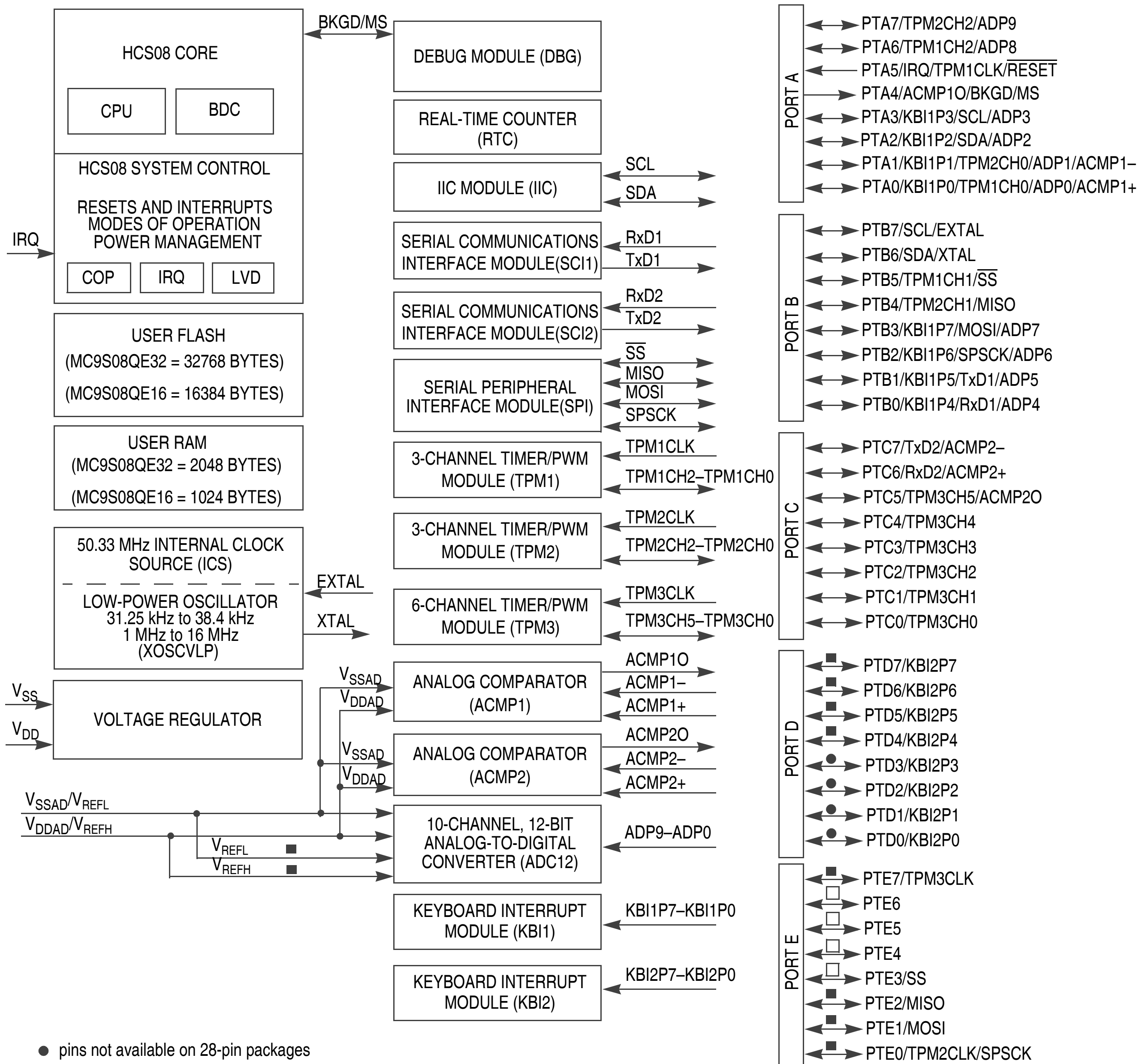
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qe16cwl

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08QE32 MCU.



● pins not available on 28-pin packages

■ pins not available on 28-pin or 32-pin packages

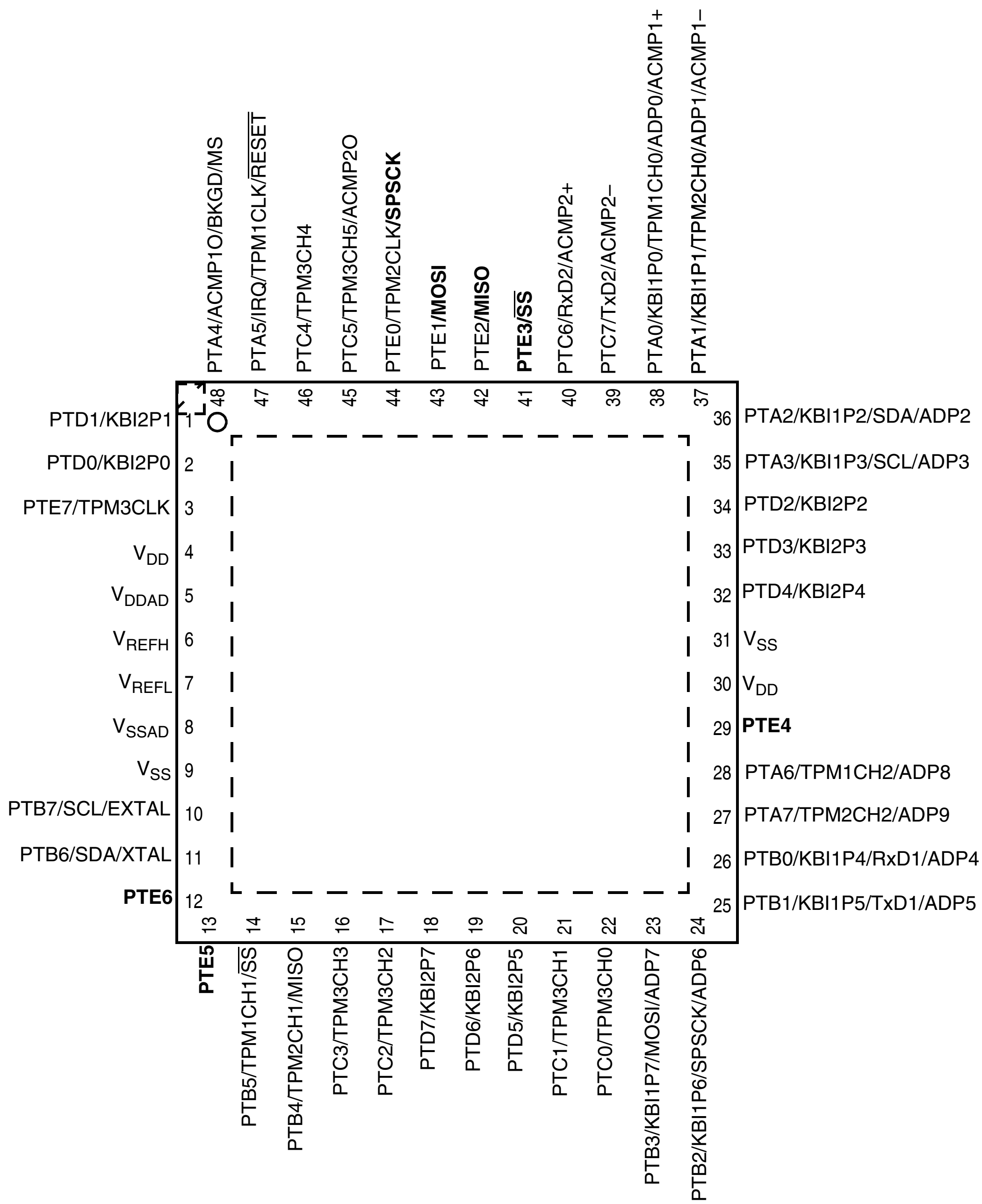
□ pins not available on 28-pin, 32-pin, or 44-pin packages

Notes: When PTA5 is configured as RESET, pin becomes bi-directional with output being open-drain drive containing an internal pullup device.
When PTA4 is configured as BKGD, pin becomes bi-directional.
For the 28-pin packages, V_{SSAD}/V_{REFL} and V_{DDAD}/V_{REFH} are double bonded to V_{SS} and V_{DD} respectively.
The 48-pin package is the only package with the option of having the SPI pins (SS, MISO, MOSI, and SPSCK) available on PTE3-0 pins.

Figure 1. MC9S08QE32 Series Block Diagram

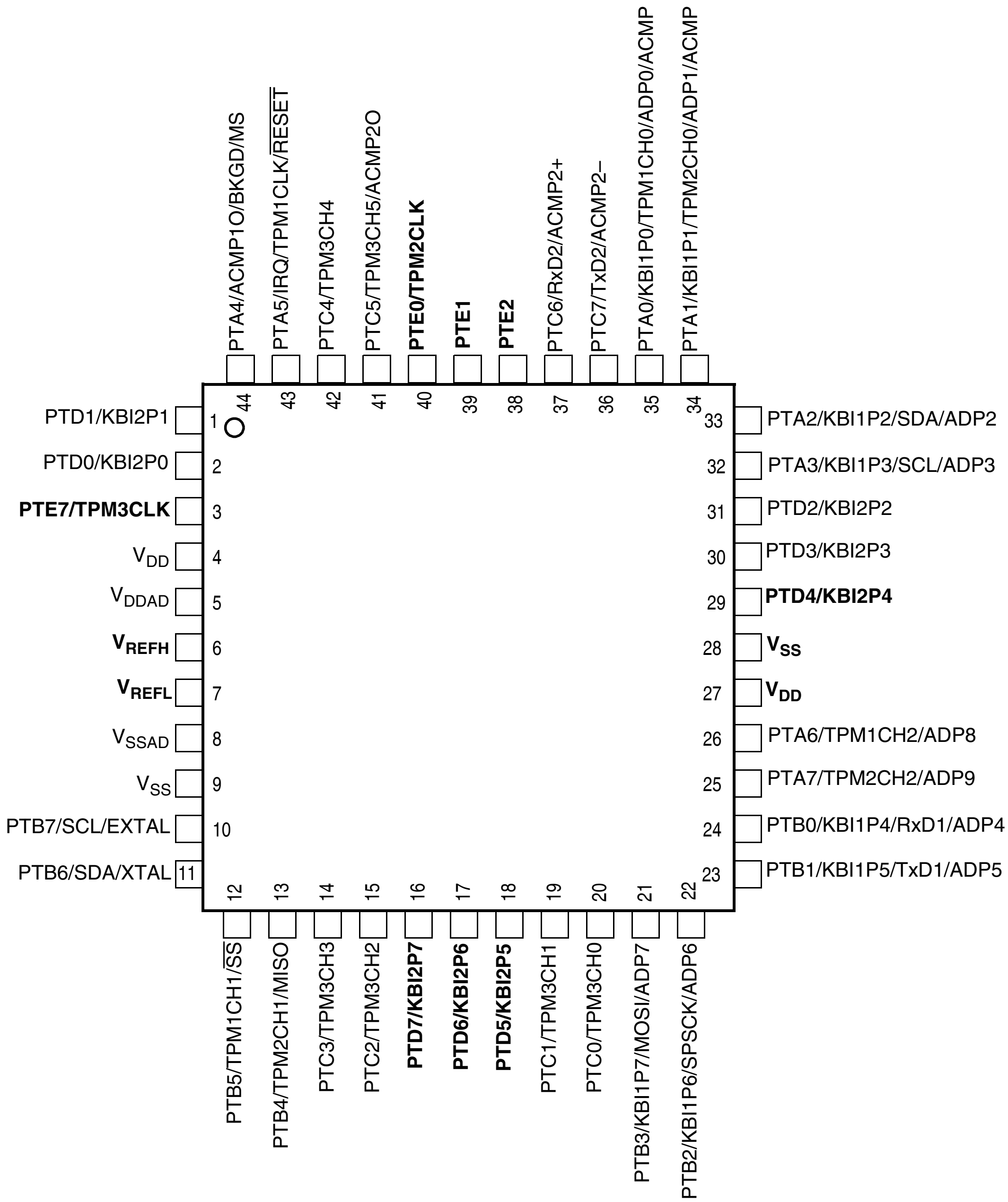
2 Pin Assignments

This section shows the pin assignments for the MC9S08QE32 series devices.



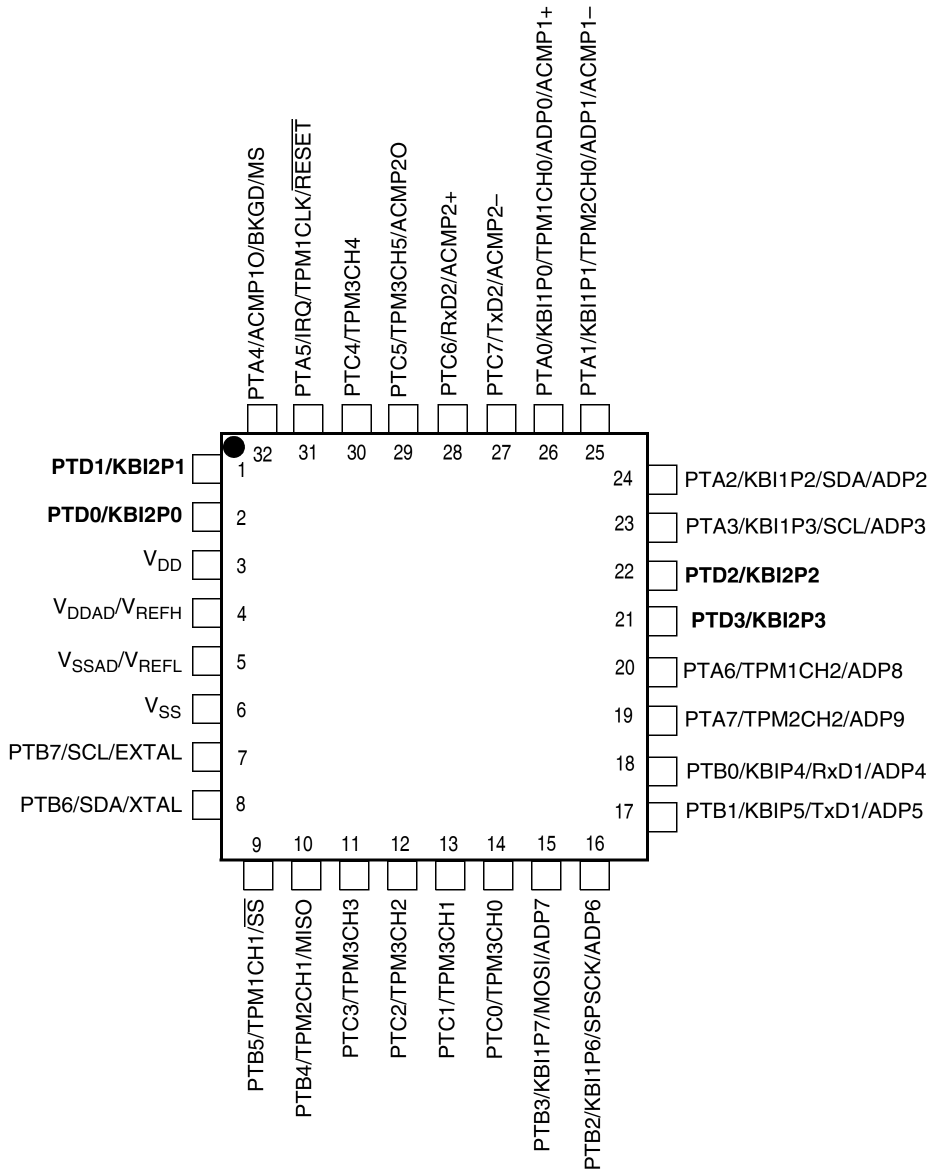
Pins in **bold** are lost in the next lower pin count package.

Figure 2. 48-Pin QFN



Pins in **bold** are lost in the next lower pin count package.

Figure 3. 44-Pin LQFP



Pins in **bold** are lost in the next lower pin count package.

Figure 4. 32-Pin LQFP/QFN

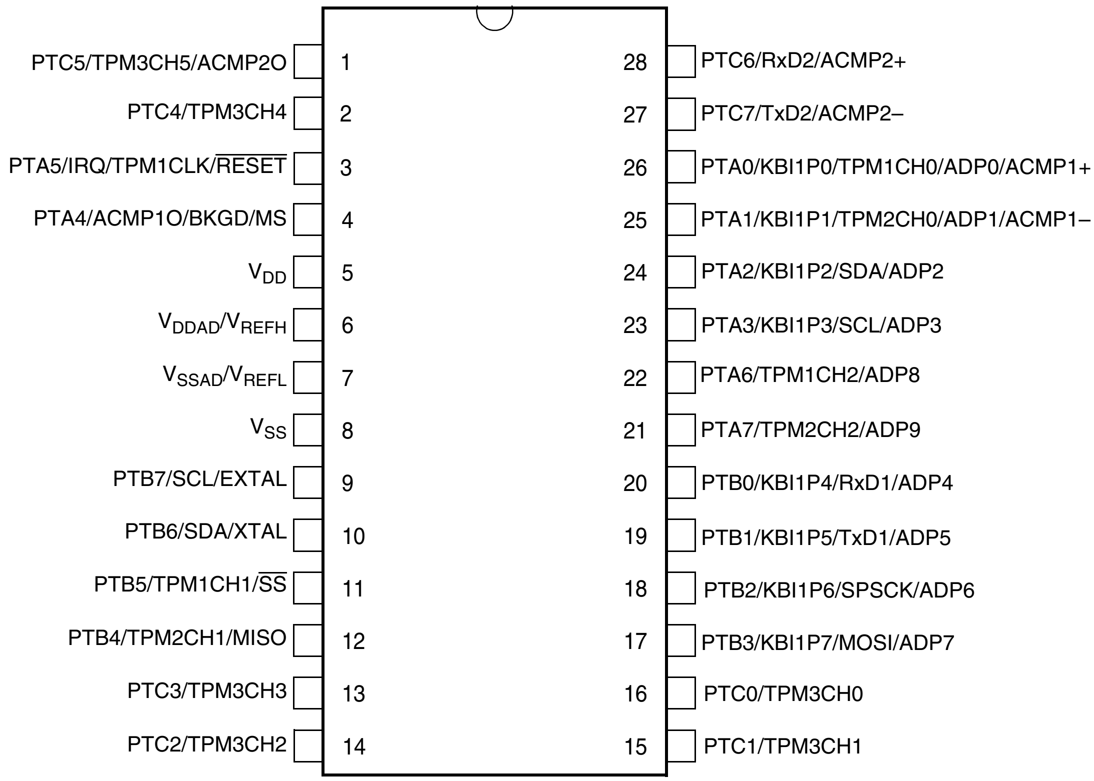


Figure 5. 28-Pin SOIC

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority

Pin Number				<-- Lowest	**Priority**	--> Highest		
48	**44**	**32**	**28**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	—	PTD1	KBI2P1			
2	2	2	—	PTD0	KBI2P0			
3	3	—	—	PTE7	TPM3CLK			
4	4	3	5					V_{DD}
5	5	4	6					V_{DDAD}
6	6							V_{REFH}
7	7	5	7					V_{REFL}
8	8							V_{SSAD}
9	9	6	8					V_{SS}
10	10	7	9	PTB7	SCL[1]			EXTAL
11	11	8	10	PTB6	SDA[1]			XTAL
12	—	—	—	PTE6				
13	—	—	—	PTE5				
14	12	9	11	PTB5	TPM1CH1	$\overline{SS}$[2]		
15	13	10	12	PTB4	TPM2CH1	MISO[2]		
16	14	11	13	PTC3	TPM3CH3			
17	15	12	14	PTC2	TPM3CH2			
18	16	—	—	PTD7	KBI2P7			

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority (continued)

Pin Number				<-- Lowest **Priority** --> Highest				
48	**44**	**32**	**28**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
19	17	—	—	PTD6	KBI2P6			
20	18	—	—	PTD5	KBI2P5			
21	19	13	15	PTC1	TPM3CH1			
22	20	14	16	PTC0	TPM3CH0			
23	21	15	17	PTB3	KBI1P7	MOSI[2]		ADP7
24	22	16	18	PTB2	KBI1P6	SPSCK[2]		ADP6
25	23	17	19	PTB1	KBI1P5	TxD1		ADP5
26	24	18	20	PTB0	KBI1P4	RxD1		ADP4
27	25	19	21	PTA7	TPM2CH2			ADP9
28	26	20	22	PTA6	TPM1CH2			ADP8
29	—	—	—	PTE4				
30	27	—	—					V_{DD}
31	28	—	—					V_{SS}
32	29	—	—	PTD4	KBI2P4			
33	30	21	—	PTD3	KBI2P3			
34	31	22	—	PTD2	KBI2P2			
35	32	23	23	PTA3	KBI1P3	SCL[1]		ADP3
36	33	24	24	PTA2	KBI1P2	SDA[1]		ADP2
37	34	25	25	PTA1	KBI1P1	TPM2CH0	ADP1[3]	ACMP1–[3]
38	35	26	26	PTA0	KBI1P0	TPM1CH0	ADP0[3]	ACMP1+[3]
39	36	27	27	PTC7	TxD2			ACMP2–
40	37	28	28	PTC6	RxD2			ACMP2+
41	—	—	—	PTE3	$\overline{\text{SS}}$[2]			
42	38	—	—	PTE2	MISO[2]			
43	39	—	—	PTE1	MOSI[2]			
44	40	—	—	PTE0	TPM2CLK	SPSCK[2]		
45	41	29	1	PTC5	TPM3CH5			ACMP2O
46	42	30	2	PTC4	TPM3CH4			
47	43	31	3	PTA5	IRQ	TPM1CLK	$\overline{\text{RESET}}$	
48	44	32	4	PTA4	ACMP1O	BKGD	MS	

1 IIC pins, SCL and SDA can be repositioned using IICPS in SOPT2; default reset locations are PTA3 and PTA2.

2 SPI pins ($\overline{\text{SS}}$, MISO, MOSI, and SPSCK) can be repositioned using SPIPS in SOPT2. Default locations are PTB5, PTB4, PTB3, and PTB2.

3 If ADC and ACMP1 are enabled, both modules will have access to the pin.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE32 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance Single-layer board			
48-pin QFN	θ_{JA}	81	°C/W
44-pin LQFP		68	
32-pin LQFP		66	
32-pin QFN		92	
28-pin SOIC		57	
Thermal resistance Four-layer board			
48-pin QFN	θ_{JA}	26	°C/W
44-pin LQFP		46	
32-pin LQFP		54	
32-pin QFN		33	
28-pin SOIC		42	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

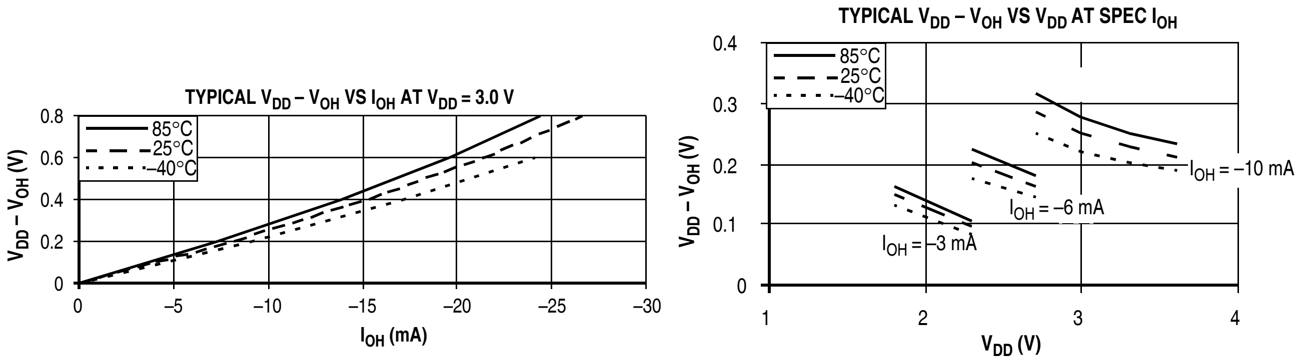


Figure 10. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25.165 MHz	3	13	14	mA	–40 to 25
	P					14	15		85
	T			20 MHz		13.75	—		–40 to 85
	T			8 MHz		5.59	—		
	T			1 MHz		1.03	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25.165 MHz	3	11.5	12.3	mA	–40 to 85
	T			20 MHz		9.5	—		
	T			8 MHz		4.6	—		
	T			1 MHz		1.0	—		
3	T	Run supply current LPRS = 0, all modules off	RI_{DD}	16 kHz FBILP	3	152	—	μA	–40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPRS = 1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	21.9	—	μA	–40 to 85
	T	Run supply current LPRS = 1, all modules off, running from RAM				7.3	—		
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25.165 MHz	3	5.74	6.00	mA	--40 to 85
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
6	P	Stop2 mode supply current		$S2I_{DD}$	—	3	0.35	0.65	µA	–40 to 25C
	C				—		0.8	1.0		70
	P				—		2.0	4.5		85
	C				—	2	0.25	0.50		–40 to 25
	C				—		0.65	0.85		70
	C				—		1.5	3.5		85
7	P	Stop3 mode supply current no clocks active		$S3I_{DD}$	—	3	0.45	1.00	µA	–40 to 25
	C				—		1.5	2.3		70
	P				—		4	8		85
	C				—	2	0.35	0.70		–40 to 25
	C				—		1	2		70
	C				—		3.5	6.0		85
8	T	Low power mode adders:	EREFSTEN=1		32 kHz	3	500	—	nA	–40 to 85
9	T		IREFSTEN=1		32 kHz		70	—	µA	
10	T		TPM PWM		100 Hz		12	—	µA	
11	T		SCI, SPI, or IIC		300 bps		15	—	µA	
12	T		RTC using LPO		1 kHz		200	—	nA	
13	T		RTC using ICSERCLK		32 kHz		1	—	µA	
14	T		LVD		n/a		100	—	µA	
15	T		ACMP		n/a		20	—	µA	

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				–40°C	25°C	70°C	85°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]	—	63	70	77	81	µA
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	µA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	22	23	µA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	µA

1 Not available in stop2 mode.

3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits.

Table 10. XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	f_{lo} f_{hi} f_{hi}	32 1 1	— — —	38.4 16 8	kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1 C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	— — —	— 10 1	— — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	— 100 0 0 0 0	— — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	t_{CSTL} t_{CSTH}	— — — —	200 400 5 15	— — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	40 40	MHz MHz

1 Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

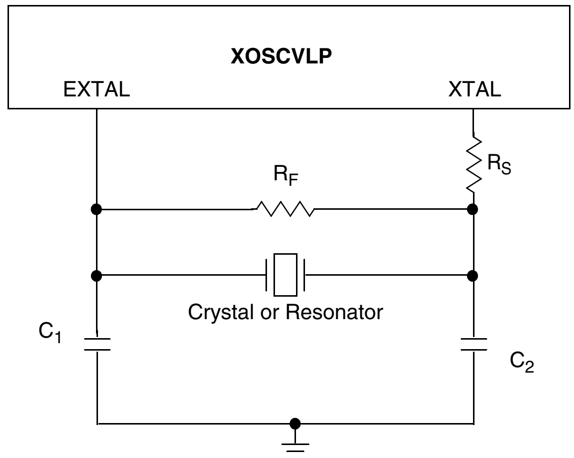


Figure 11. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

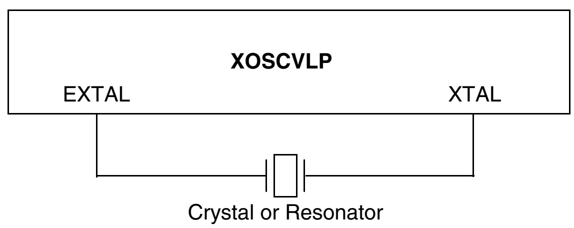


Figure 12. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed		f_{int_t}	—	32.768	—	kHz
2	C	Average internal reference frequency — untrimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	5	10	μs
4	P	DCO output frequency trimmed[2]	Low range (DFR = 00)	f_{dco_u}	16	—	20	MHz
	P		Mid range (DFR = 01)		32	—	40	
	P		High range (DFR = 10)		48	—	60	
5	P	DCO output frequency[2] reference = 32768 Hz and DMX32 = 1	Low range (DFR = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DFR = 01)		—	39.85	—	
	P		High range (DFR = 10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[3]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.
2 The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.
3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

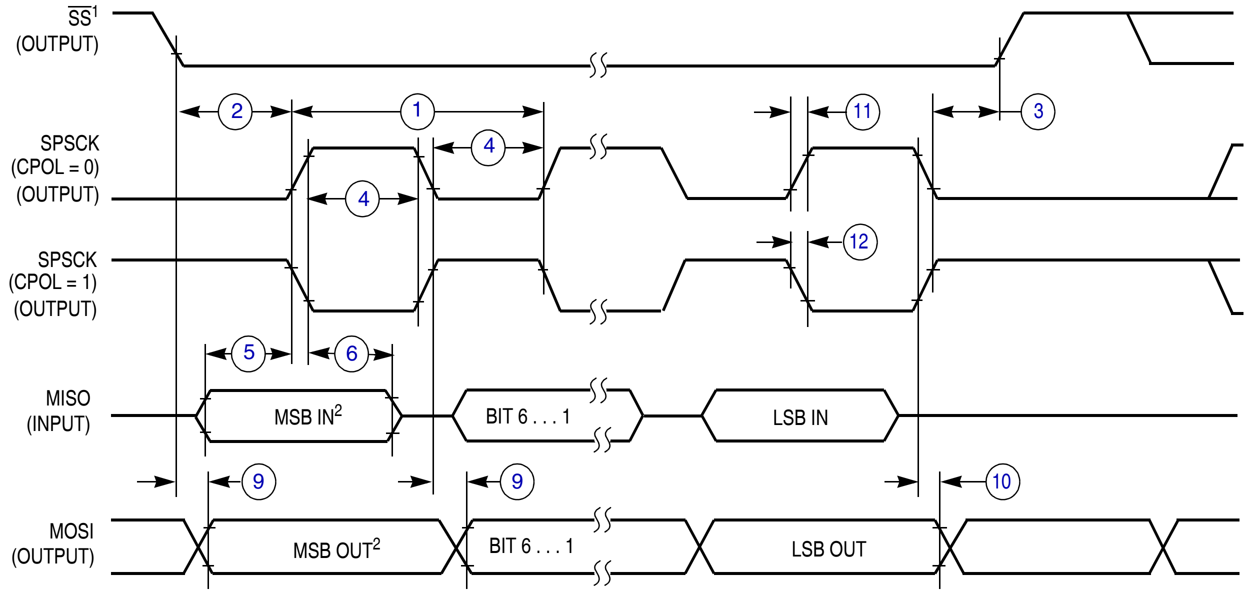
3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

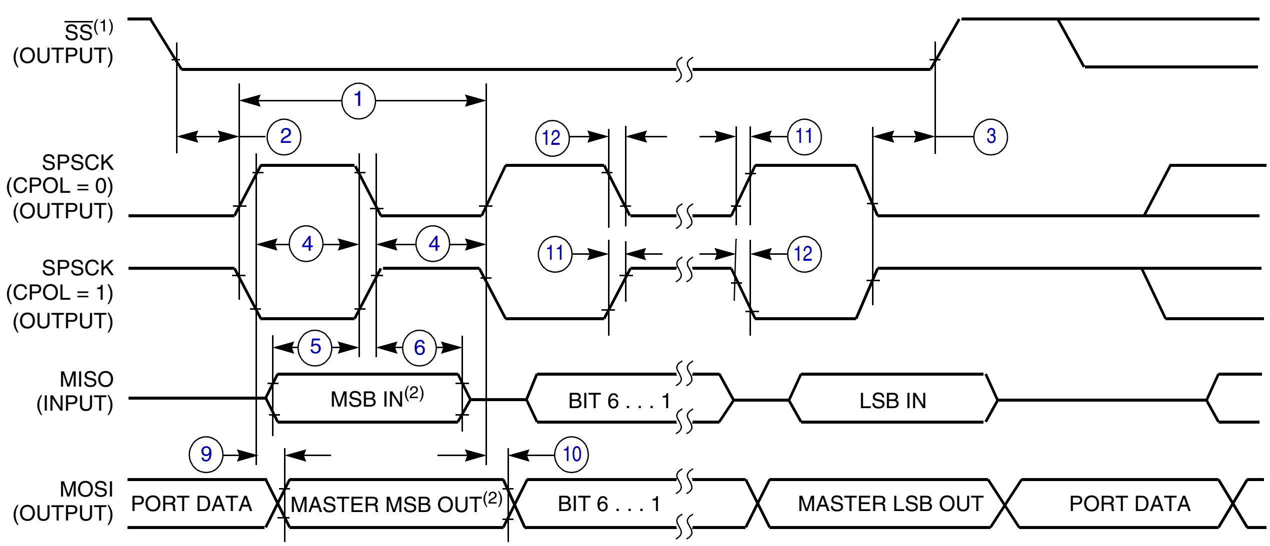
Table 12. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$) $V_{DD} \leq 2.1V$ $2.1 < V_{DD} \leq 2.4V$ $V_{DD} > 2.4Vs$	f_{Bus}	DC	—	10 20 25.165	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns



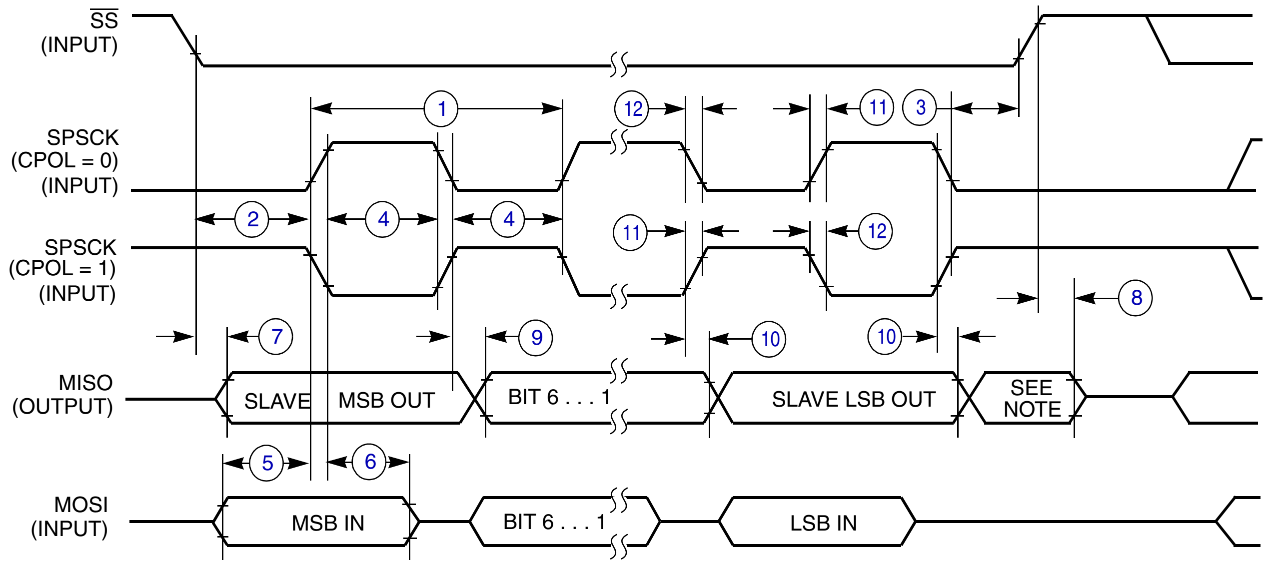
NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

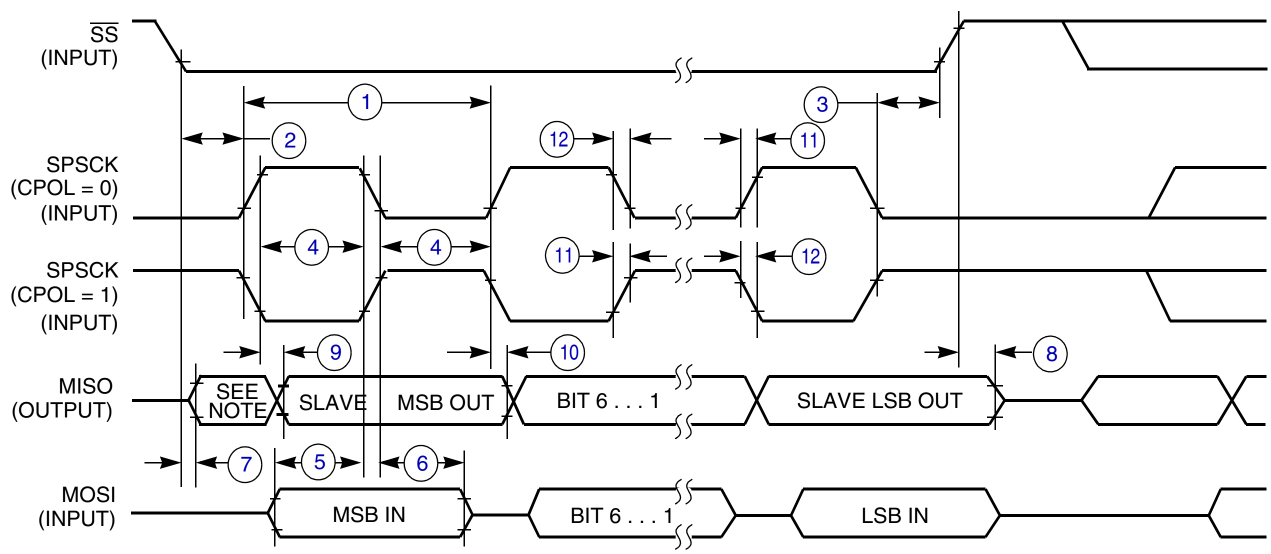
Figure 18. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 19. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 20. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 15. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
P	Supply current (active)	I_{DDAC}	—	20	35	µA
D	Analog input voltage	V_{AIN}	$V_{SS} – 0.3$	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}	—	20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs

3.12 ADC Characteristics

Table 16. 12-Bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	—
		Delta to V_{DD} (V_{DD} – V_{DDAD})[2]	ΔV_{DDAD}	–100	0	100	mV	—
D	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSAD})[2]	ΔV_{SSAD}	–100	0	100	mV	—
D	Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
C	Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
C	Input resistance	—	R_{ADIN}	—	5	7	kΩ	—
C	Analog source resistance	12-bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
		10-bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz		 — —	 — —	 5 10		
		8-bit mode (all valid f_{ADCK})		—	—	10		
D	ADC conversion clock freq.	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
		Low power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

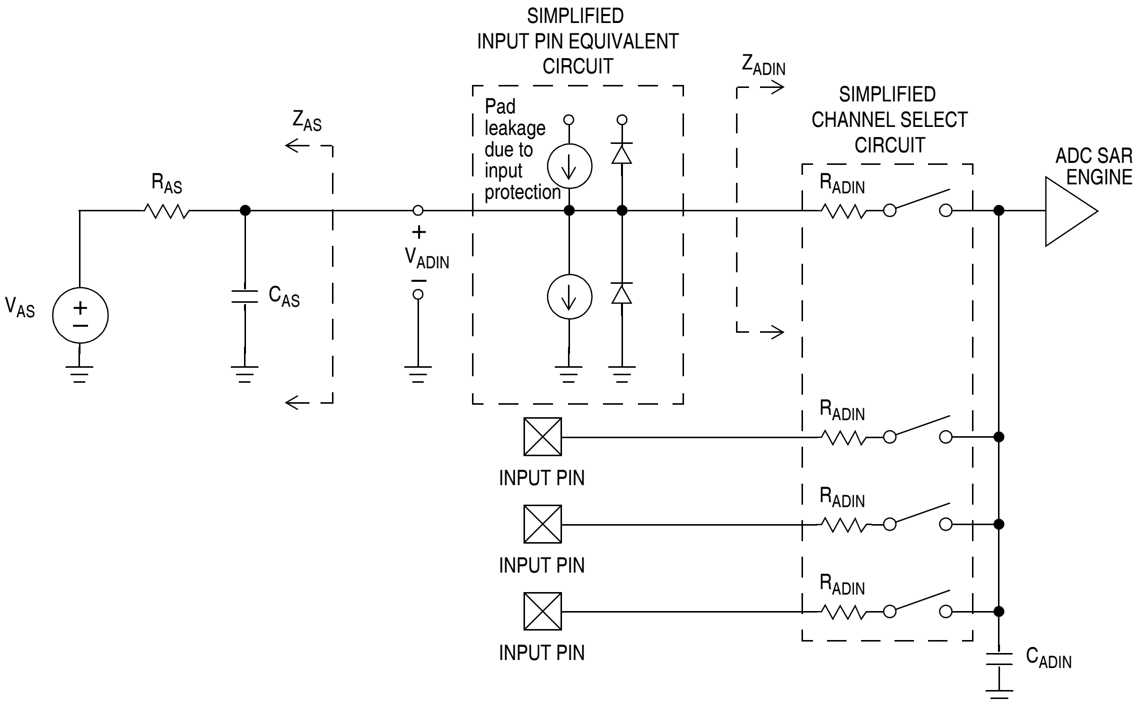


Figure 21. ADC Input Impedance Equivalency Diagram

Table 17. ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	120	—	µA	
T	Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	202	—	µA	
T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	288	—	µA	
P	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	0.532	1	mA	
P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low power (ADLPC = 1)		1.25	2	3.3		

Table 17. ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$) (continued)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long sample (ADLSMP = 1)		—	40	—		
P	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long sample (ADLSMP = 1)		—	23.5	—		
D	Temp sensor slope	–40 °C– 25 °C	m	—	1.646	—	mV/°C	
		25 °C– 85 °C		—	1.769	—		
D	Temp sensor voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	
T	Total unadjusted error	12-bit mode, 3.6> V_{DDAD} > 2.7	E_{TUE}	—	–1 to 3	–2.5 to 5.5	LSB[2]	Includes quantization
T		12-bit mode, 2.7> V_{DDAD} > 1.8V		—	–1 to 3	–3.0 to 6.5		
P		10-bit mode		—	±1	±2.5		
P		8-bit mode		—	±0.5	±1.0		
T	Differential non-linearity	12-bit mode	DNL	—	±1.0	–1.5 to 2.0	LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
P		8-bit mode[3]		—	±0.3	±0.5		
T	Integral non-linearity	12-bit mode	INL	—	±1.5	–2.5 to 2.75	LSB[2]	
T		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		
T	Zero-scale error	12-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSAD}$
P		10-bit mode		—	±0.5	±1.5		
P		8-bit mode		—	±0.5	±0.5		
T	Full-scale error	12-bit mode	E_{FS}	—	±1.0	–3.5 to 1.0	LSB[2]	$V_{ADIN} = V_{DDAD}$
P		10-bit mode		—	±0.5	±1		
P		8-bit mode		—	±0.5	±0.5		
D	Quantization error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	
		10-bit mode		—	—	±0.5		
		8-bit mode		—	—	±0.5		
D	Input leakage error	12-bit mode	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode		—	±0.2	±4		
		8-bit mode		—	±0.1	±1.2		

[1] Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
[2] 1 LSB = $(V_{REFH} – V_{REFL})/2^N$
[3] Monotonicity and No-missing-codes guaranteed in 10-bit and 8-bit modes
[4] Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see MC9S08QE32 Series Reference Manual Chapter 4 Memory.

Table 18. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
P	Byte program time (random location)(2)	t_{prog}		9		t_{Fcyc}
P	Byte program time (burst mode)(2)	t_{Burst}		4		t_{Fcyc}
P	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
P	Mass erase time(2)	t_{Mass}		20,000		t_{Fcyc}
	Byte program current[3]	R_{IDDBP}	—	4	—	mA
	Page erase current[3]	R_{IDDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40 °C to 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

[1] The frequency of this clock is controlled by software setting.
[2] These values are hardware state machine controlled. User code does not need to count cycles. This information is supplied for calculating approximate time to program and erase.
[3] The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.
[4] **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.
[5] **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*