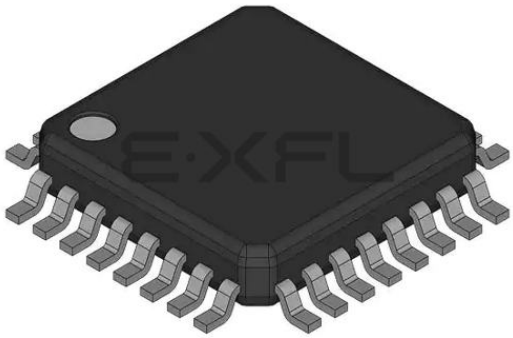

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Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08qe32clcr

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	7/2/2008	Initial public released.
2	10/7/2008	Updated the Stop2 and Stop3 mode supply current, and RI_{DD} in FEI mode with all modules on at 25.165 MHz in the Table 8 Supply Current Characteristics. Replaced the stop mode adders section from Table 8 with an individual Table 9 Stop Mode Adders with new specifications.
3	11/4/2008	Updated operating voltage in Table 7.
4	5/4/2009	Added 10×10 mm information to 44 LQFP in the front page. In Table 7, added $\|I_{OZTOT}\|$. In Table 11, updated typicals and Max. for $t_{IRST.}$ In Table 16, removed the Rev. Voltage High item. Updated Table 17.
5	8/27/2009	Updated f_{int_t} and f_{int_ut} in the Table 11.
6	10/13/2009	Corrected the package size descriptions on the cover
7	9/16/2011	Added new package of 32-pin QFN.

Related Documentation

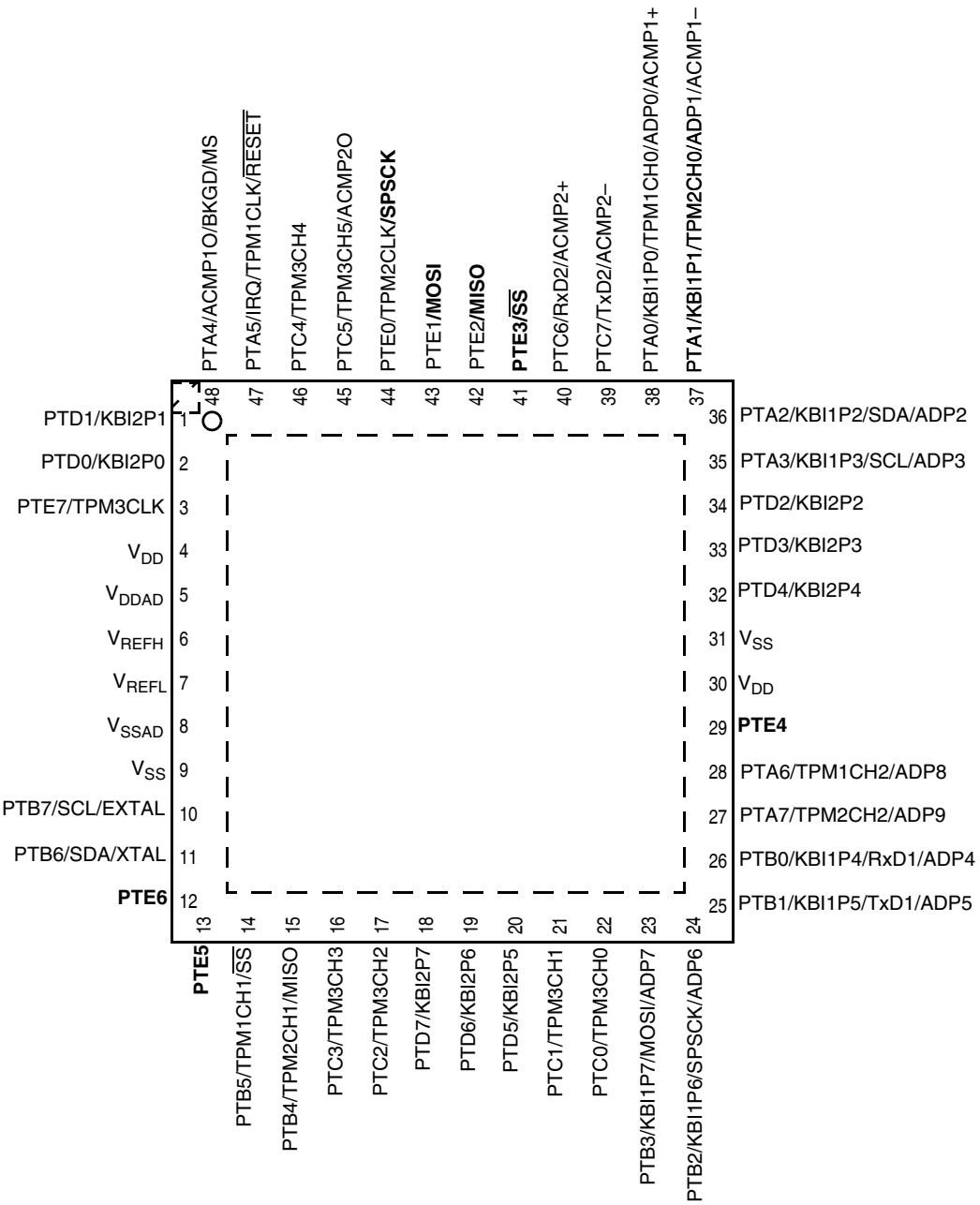
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08QE32RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

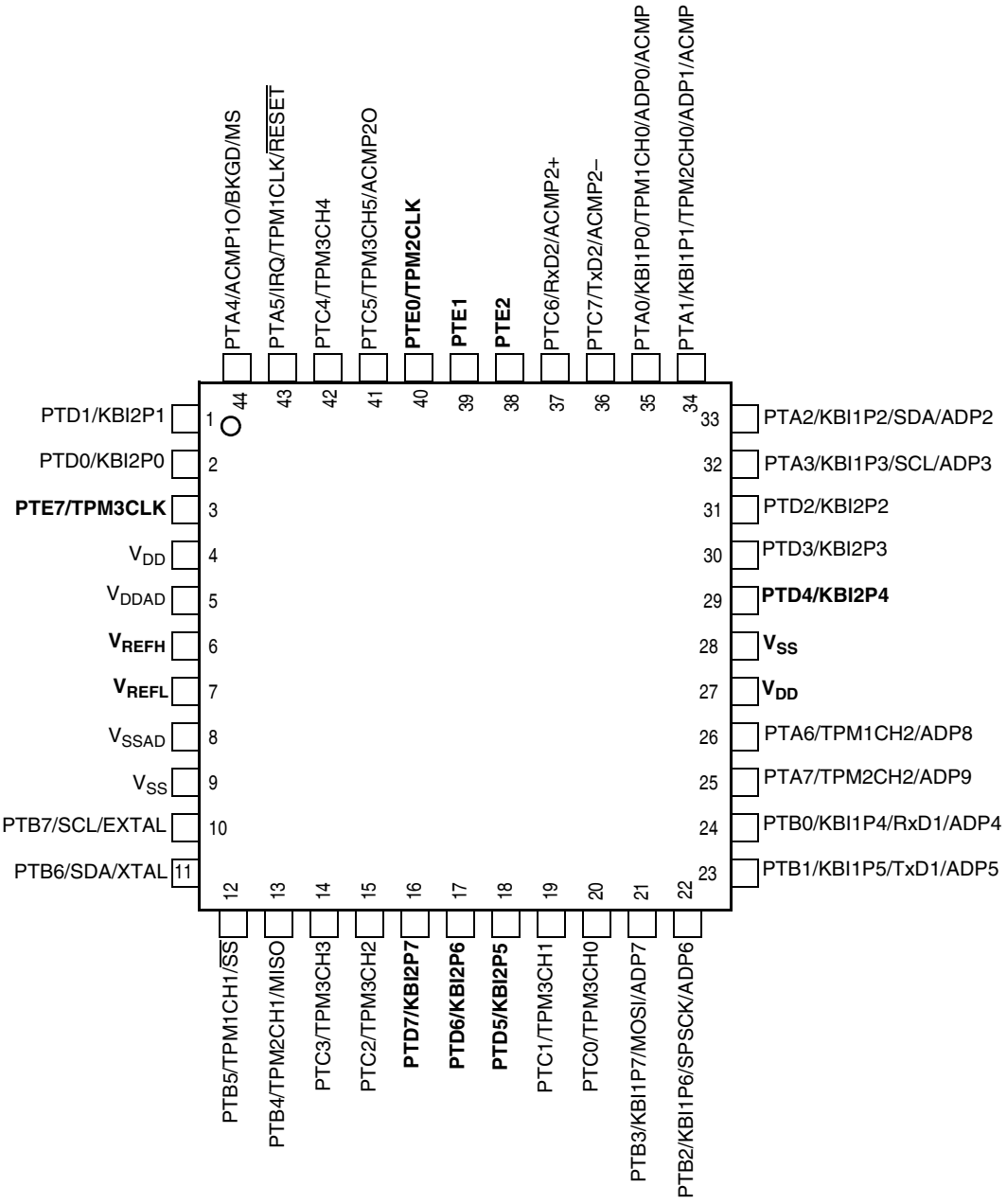
2 Pin Assignments

This section shows the pin assignments for the MC9S08QE32 series devices.



Pins in **bold** are lost in the next lower pin count package.

Figure 2. 48-Pin QFN



Pins in **bold** are lost in the next lower pin count package.

Figure 3. 44-Pin LQFP

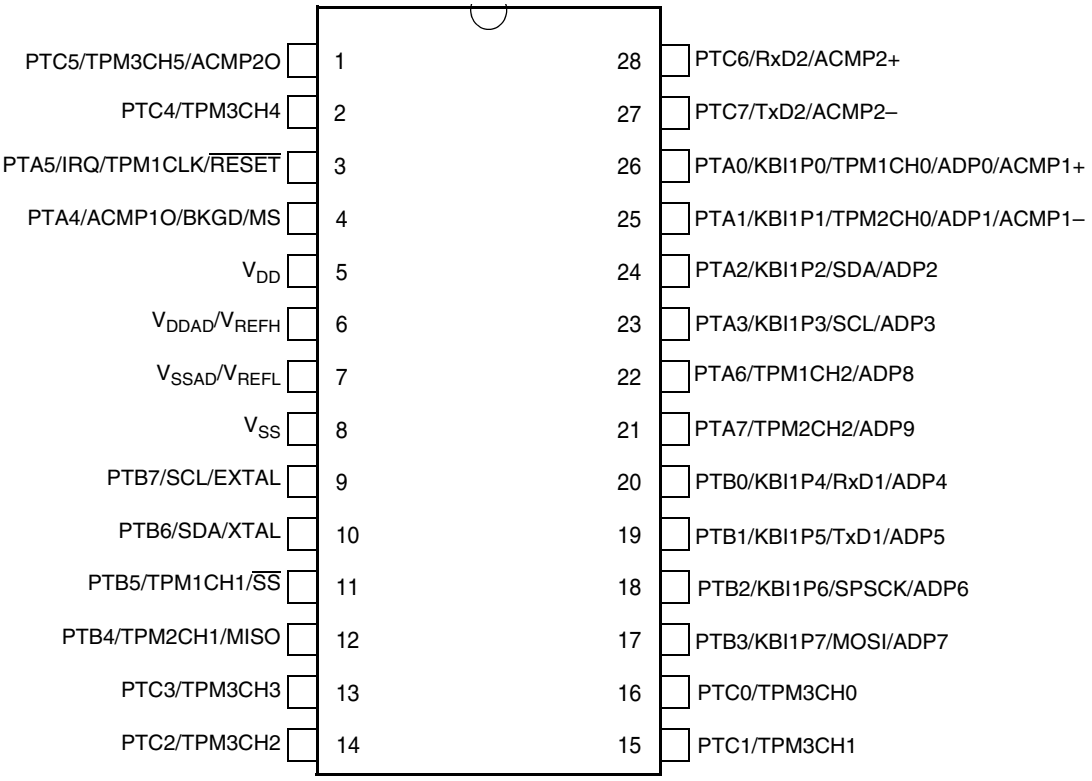


Figure 5. 28-Pin SOIC

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority

Pin Number				<-- Lowest **Priority** --> Highest				
48	**44**	**32**	**28**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	—	PTD1	KBI2P1			
2	2	2	—	PTD0	KBI2P0			
3	3	—	—	PTE7	TPM3CLK			
4	4	3	5					V_{DD}
5	5	4	6					V_{DDAD}
6	6							V_{REFH}
7	7	5	7					V_{REFL}
8	8							V_{SSAD}
9	9	6	8					V_{SS}
10	10	7	9	PTB7	SCL[1]			EXTAL
11	11	8	10	PTB6	SDA[1]			XTAL
12	—	—	—	PTE6				
13	—	—	—	PTE5				
14	12	9	11	PTB5	TPM1CH1	$\overline{SS}$[2]		
15	13	10	12	PTB4	TPM2CH1	MISO[2]		
16	14	11	13	PTC3	TPM3CH3			
17	15	12	14	PTC2	TPM3CH2			
18	16	—	—	PTD7	KBI2P7			

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance Single-layer board			
48-pin QFN	θ_{JA}	81	°C/W
44-pin LQFP		68	
32-pin LQFP		66	
32-pin QFN		92	
28-pin SOIC		57	
Thermal resistance Four-layer board			
48-pin QFN	θ_{JA}	26	°C/W
44-pin LQFP		46	
32-pin LQFP		54	
32-pin QFN		33	
28-pin SOIC		42	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typical[1]	Max	Unit
1		Operating Voltage V_{DD} rising V_{DD} falling			 2.0 1.8	—	3.6	V
2	C	Output high voltage[2] — All I/O pins, low-drive strength	V_{OH}	1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P	All I/O pins, high-drive strength		2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	T			2.3 V, I_{Load} = –6 mA	V_{DD} – 0.5	—	—	
	C			1.8V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	D	Output high current — Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
4	C	Output low voltage — All I/O pins, low-drive strength	V_{OL}	1.8 V, I_{Load} = 2 mA	—	—	0.5	V
	P	All I/O pins, high-drive strength		2.7 V, I_{Load} = 10 mA	—	—	0.5	
	T			2.3 V, I_{Load} = 6 mA	—	—	0.5	
	C			1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current — Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
6	P	Input high voltage — all digital inputs	V_{IH}	V_{DD} > 2.3 V	0.70 x V_{DD}	—	—	V
	C			V_{DD} ≤ 1.8 V	0.85 x V_{DD}	—	—	
7	P	Input low voltage — all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C			V_{DD} ≤ 1.8 V	—	—	0.30 x V_{DD}	
8	C	Input hysteresis — all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
9	P	Input leakage current — all input only pins (Per pin)	$\lvert I_{In} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	1	μA
10	P	Hi-Z (off-state) leakage current — all input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	1	μA
11	C	Total leakage combined for all inputs and Hi-Z pins — All input only and I/O	$\lvert I_{OZTOT} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	2	μA
11	P	Pullup, Pulldown resistors — all digital inputs, when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
12	D	DC injection current [3, 4, 5] — Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
		Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
13	C	Input Capacitance, all pins	C_{In}		—	—	8	pF
14	C	RAM retention voltage	V_{RAM}		—	0.6	1.0	V
15	C	POR re-arm voltage[6]	V_{POR}		0.9	1.4	2.0	V

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
6	P	Stop2 mode supply current		$S2I_{DD}$	—	3	0.35	0.65	μA	–40 to 25C
	C				—		0.8	1.0		70
	P				—		2.0	4.5		85
	C				—	2	0.25	0.50		–40 to 25
	C				—		0.65	0.85		70
	C				—		1.5	3.5		85
7	P	Stop3 mode supply current no clocks active		$S3I_{DD}$	—	3	0.45	1.00	μA	–40 to 25
	C				—		1.5	2.3		70
	P				—		4	8		85
	C				—	2	0.35	0.70		–40 to 25
	C				—		1	2		70
	C				—		3.5	6.0		85
8	T	Low power mode adders:	EREFSTEN=1		32 kHz	3	500	—	nA	–40 to 85
9	T		IREFSTEN=1		32 kHz		70	—	μA	
10	T		TPM PWM		100 Hz		12	—	μA	
11	T		SCI, SPI, or IIC		300 bps		15	—	μA	
12	T		RTC using LPO		1 kHz		200	—	nA	
13	T		RTC using ICSERCLK		32 kHz		1	—	μA	
14	T		LVD		n/a		100	—	μA	
15	T		ACMP		n/a		20	—	μA	

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				–40°C	**25**°C	**70**°C	**85**°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]	—	63	70	77	81	μA
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	μA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	22	23	μA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	μA

[1] Not available in stop2 mode.

3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits.

Table 10. XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	 C_1 C_2	 See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH} 	 — — — —	 200 400 5 15	 — — — —	 ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	40 40	MHz MHz

[1] Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.

[2] Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

[3] See crystal or resonator manufacturer's recommendation.

[4] Proper PC board layout procedures must be followed to achieve specifications.

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[3]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 12. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$) $V_{DD} \le 2.1V$ $2.1<V_{DD} \le 2.4V$ $V_{DD} > 2.4Vs$	f_{Bus}	DC	—	10 20 25.165	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns

Table 12. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[5]	t_{ILIH}, t_{IHIL}	 100 1.5 × t_{cyc}	 — —	 — —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 8 31	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 7 24	 — —	ns
10	C	Voltage regulator recovery time	t_{VRR}	—	4	—	µs

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 To enter BDM mode following a POR, BKGD/MS must be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

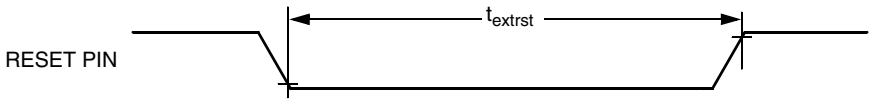


Figure 13. Reset Timing

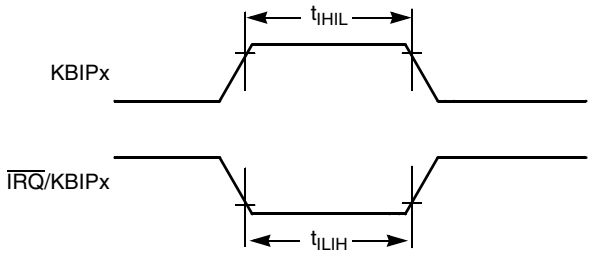


Figure 14. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 13. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

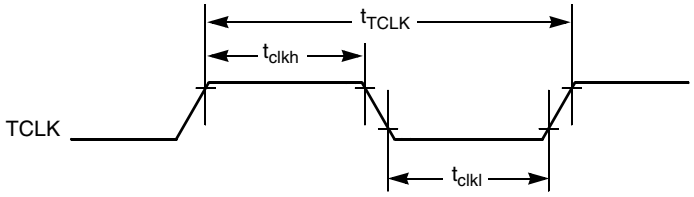


Figure 15. Timer External Clock

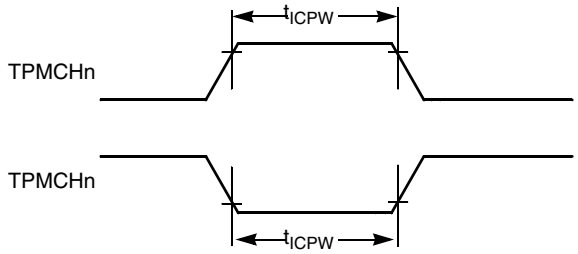


Figure 16. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 14 and Figure 17 through Figure 20 describe the timing requirements for the SPI system.

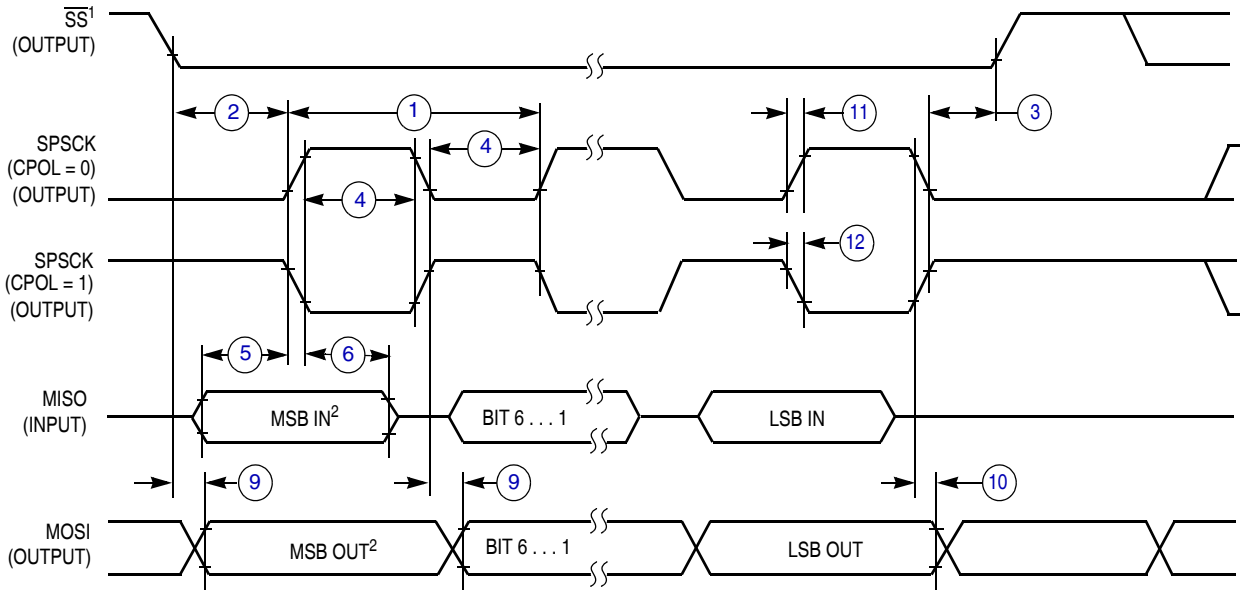
Table 14. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2^1$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}

Table 14. SPI Timing (continued)

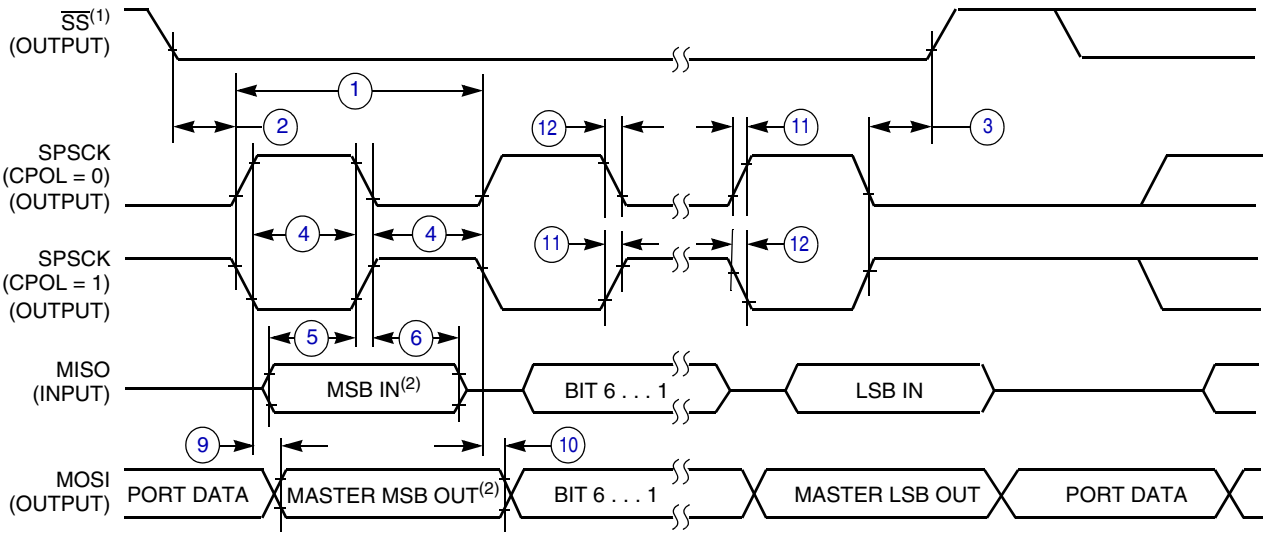
No.	C	Function	Symbol	Min	Max	Unit
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
11	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
12	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns

1 Max operating frequency limited to 8 MHz when input filter disabled and high output drive strength enabled. Max operating frequency limited to 5 MHz when input filter enabled and high output drive strength disabled.



NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI Master Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 15. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
P	Supply current (active)	I_{DDAC}	—	20	35	μA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}	—	20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.12 ADC Characteristics

Table 16. 12-Bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	—
		Delta to V_{DD} (V_{DD} – V_{DDAD})[2]	ΔV_{DDAD}	–100	0	100	mV	—
D	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSAD})[2]	ΔV_{SSAD}	–100	0	100	mV	—
D	Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
C	Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
C	Input resistance	—	R_{ADIN}	—	5	7	kΩ	—
C	Analog source resistance	12-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
		10-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz		 — —	 — —	 5 10		
		8-bit mode (all valid f_{ADCK})		—	—	10		
D	ADC conversion clock freq.	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
		Low power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 17. ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$) (continued)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long sample (ADLSMP = 1)		—	40	—		
P	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long sample (ADLSMP = 1)		—	23.5	—		
D	Temp sensor slope	–40 °C– 25 °C	m	—	1.646	—	mV/°C	
		25 °C– 85 °C		—	1.769	—		
D	Temp sensor voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	
T	Total unadjusted error	12-bit mode, 3.6> V_{DDAD} > 2.7	E_{TUE}	—	–1 to 3	–2.5 to 5.5	LSB[2]	Includes quantization
T		12-bit mode, 2.7> V_{DDAD} > 1.8V		—	–1 to 3	–3.0 to 6.5		
P		10-bit mode		—	±1	±2.5		
P		8-bit mode		—	±0.5	±1.0		
T	Differential non-linearity	12-bit mode	DNL	—	±1.0	–1.5 to 2.0	LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
P		8-bit mode[3]		—	±0.3	±0.5		
T	Integral non-linearity	12-bit mode	INL	—	±1.5	–2.5 to 2.75	LSB[2]	
T		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		
T	Zero-scale error	12-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSAD}$
P		10-bit mode		—	±0.5	±1.5		
P		8-bit mode		—	±0.5	±0.5		
T	Full-scale error	12-bit mode	E_{FS}	—	±1.0	–3.5 to 1.0	LSB[2]	$V_{ADIN} = V_{DDAD}$
P		10-bit mode		—	±0.5	±1		
P		8-bit mode		—	±0.5	±0.5		
D	Quantization error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	
		10-bit mode		—	—	±0.5		
		8-bit mode		—	—	±0.5		
D	Input leakage error	12-bit mode	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode		—	±0.2	±4		
		8-bit mode		—	±0.1	±1.2		

1 Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-missing-codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see MC9S08QE32 Series Reference Manual Chapter 4 Memory.

Table 18. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
P	Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
P	Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
P	Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
	Byte program current[3]	R_{IDDBP}	—	4	—	mA
	Page erase current[3]	R_{IDDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40 °C to 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information is supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

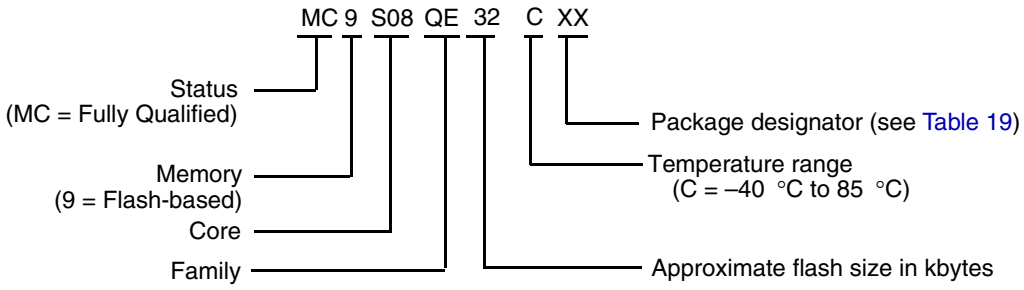
4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

4 Ordering Information

This section contains ordering information for the MC9S08QE32 series of MCUs.

Example of the device numbering system:



5 Package Information

Table 19. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
48	Quad Flat No-Leads	QFN	FT	1314	98ARH99048A
44	Low Quad Flat Package	LQFP	LD	824D	98ASS23225W
32	Low Quad Flat Package	LQFP	LC	873A	98ASH70029A
32	Quad Flat No-Leads	QFN	FM	1582	98ARE10566D
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B

5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 19. For the latest available drawings please visit our web site (http://www.freescale.com) and enter the package's document number into the keyword search box.

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