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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qe32cld">https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qe32cld</a>

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## Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

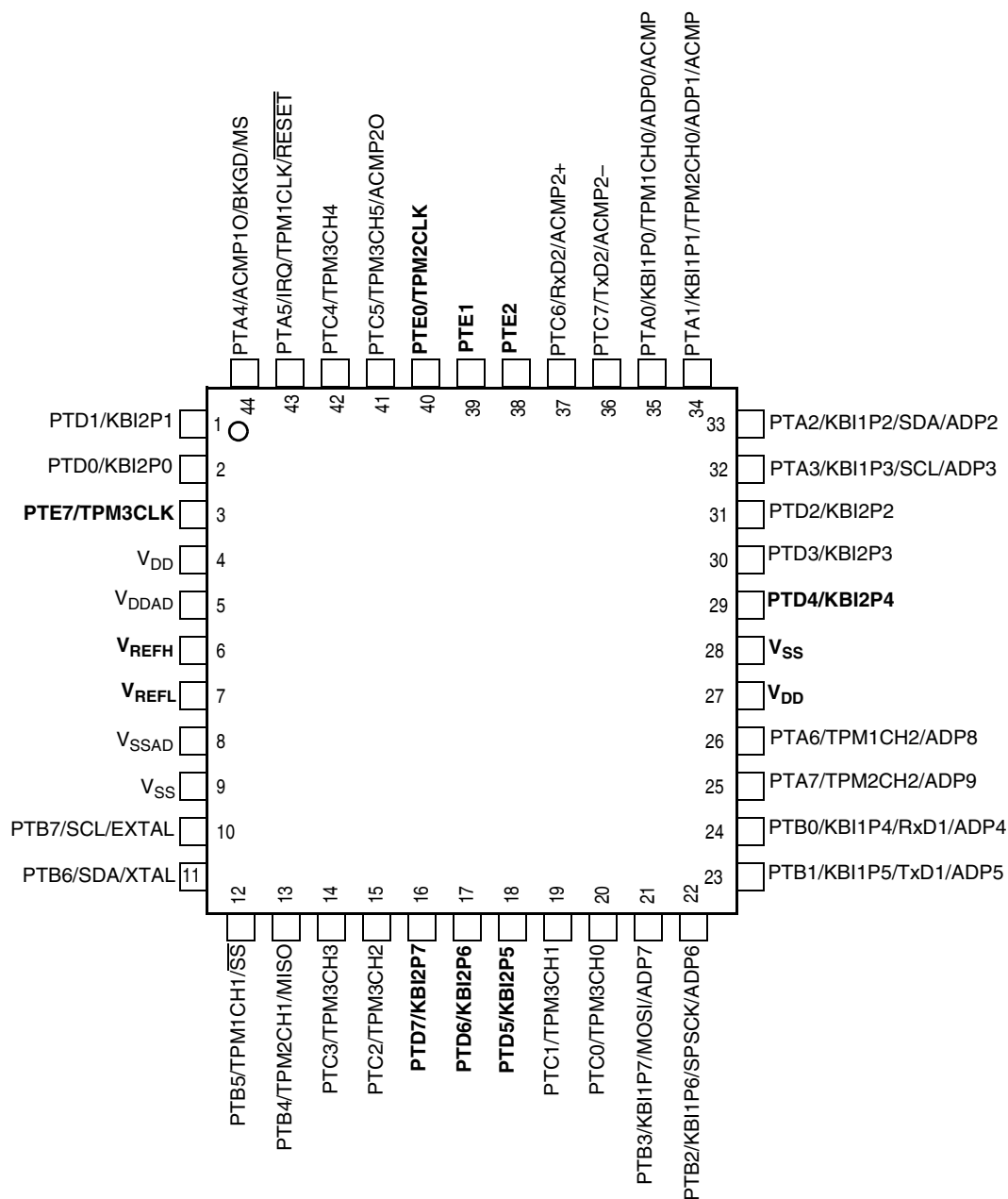
Revision	Date	Description of Changes
1	7/2/2008	Initial public released.
2	10/7/2008	Updated the Stop2 and Stop3 mode supply current, and $RI_{DD}$ in FEI mode with all modules on at 25.165 MHz in the <a href="#">Table 8</a> Supply Current Characteristics. Replaced the stop mode adders section from <a href="#">Table 8</a> with an individual <a href="#">Table 9</a> Stop Mode Adders with new specifications.
3	11/4/2008	Updated operating voltage in <a href="#">Table 7</a> .
4	5/4/2009	Added 10×10 mm information to 44 LQFP in the front page. In <a href="#">Table 7</a> , added $II_{OZTOT}$ . In <a href="#">Table 11</a> , updated typicals and Max. for $t_{IRST}$ . In <a href="#">Table 16</a> , removed the Rev. Voltage High item. Updated <a href="#">Table 17</a> .
5	8/27/2009	Updated $f_{int\_t}$ and $f_{int\_ut}$ in the <a href="#">Table 11</a> .
6	10/13/2009	Corrected the package size descriptions on the cover
7	9/16/2011	Added new package of 32-pin QFN.

## Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

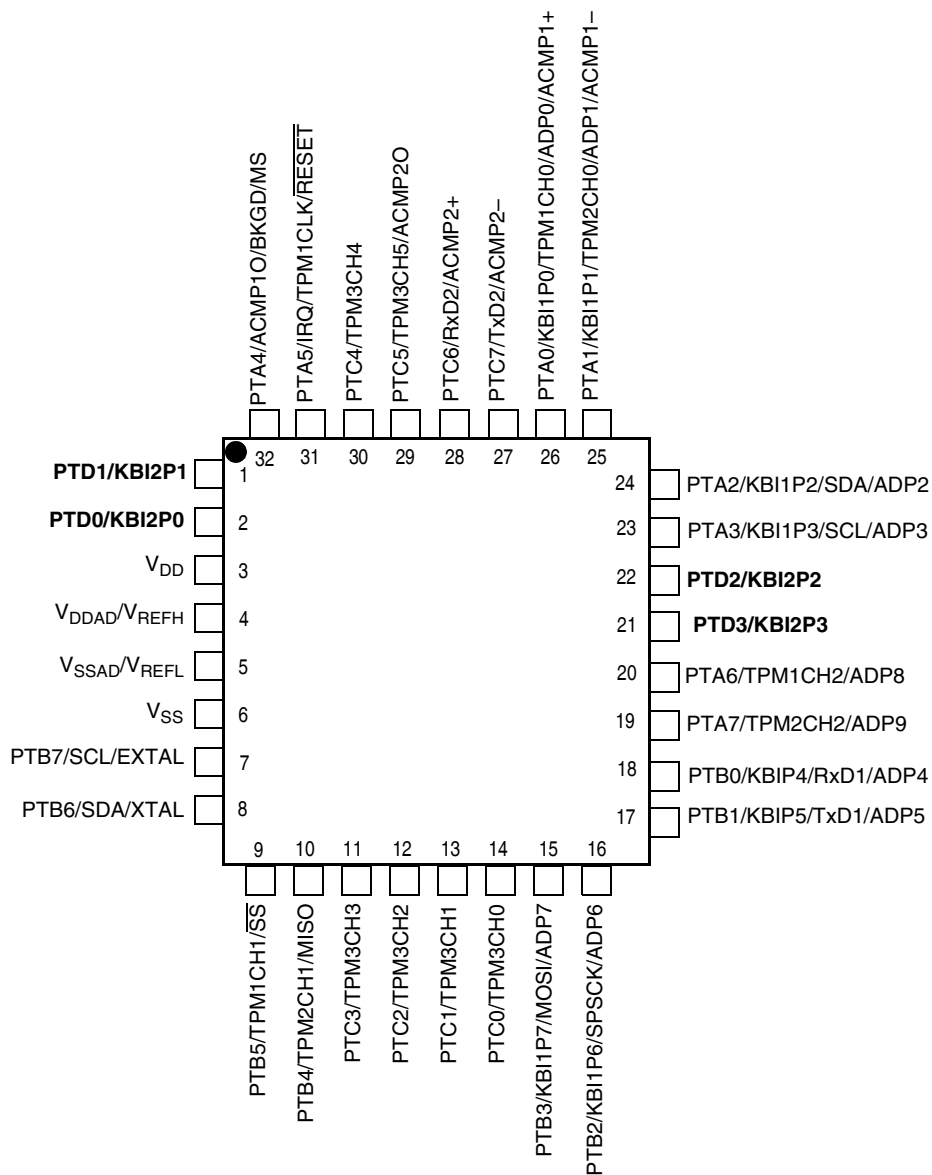
### Reference Manual (MC9S08QE32RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.



Pins in **bold** are lost in the next lower pin count package.

**Figure 3. 44-Pin LQFP**



Pins in **bold** are lost in the next lower pin count package.

**Figure 4. 32-Pin LQFP/QFN**

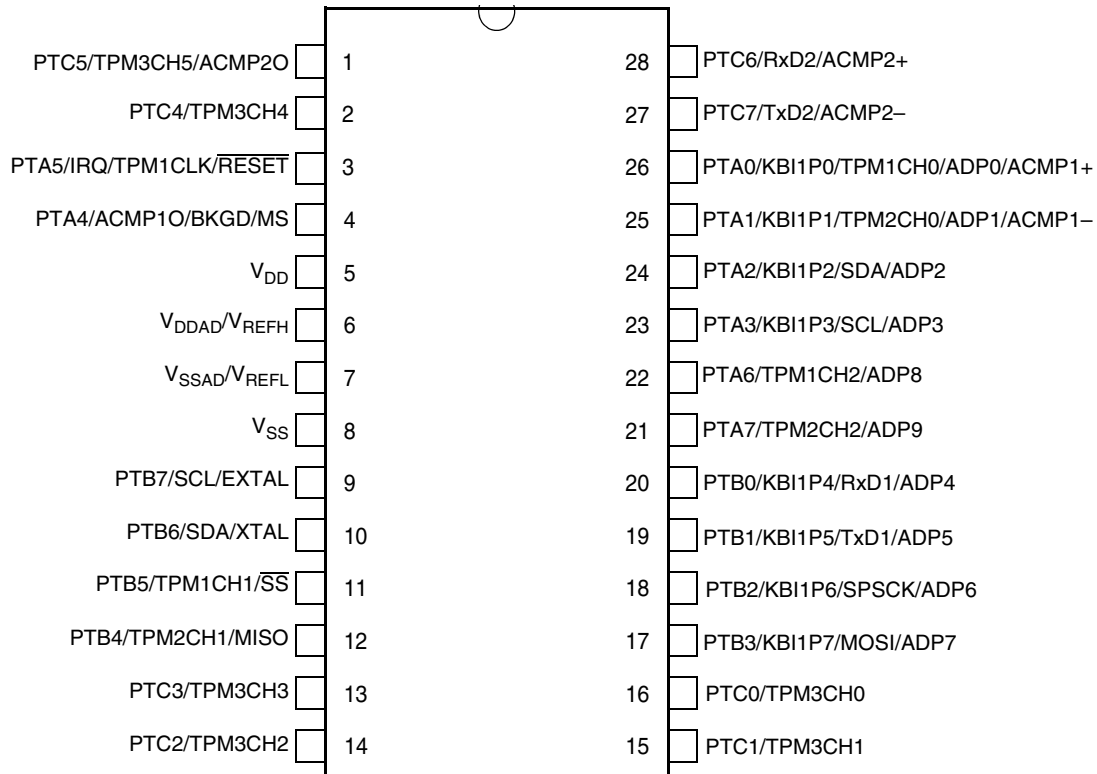


Figure 5. 28-Pin SOIC

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority

Pin Number				<-- Lowest Priority --> Highest				
48	44	32	28	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	—	PTD1	KBI2P1			
2	2	2	—	PTD0	KBI2P0			
3	3	—	—	PTE7	TPM3CLK			
4	4	3	5					V <sub>DD</sub>
5	5	4	6					V <sub>DDAD</sub>
6	6							V <sub>REFH</sub>
7	7	5	7					V <sub>REFL</sub>
8	8							V <sub>SSAD</sub>
9	9	6	8					V <sub>SS</sub>
10	10	7	9	PTB7	SCL <sup>1</sup>			EXTAL
11	11	8	10	PTB6	SDA <sup>1</sup>			XTAL
12	—	—	—	PTE6				
13	—	—	—	PTE5				
14	12	9	11	PTB5	TPM1CH1	SS <sup>2</sup>		
15	13	10	12	PTB4	TPM2CH1	MISO <sup>2</sup>		
16	14	11	13	PTC3	TPM3CH3			
17	15	12	14	PTC2	TPM3CH2			
18	16	—	—	PTD7	KBI2P7			

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority (continued)

Pin Number				<-- Lowest Priority --> Highest				
48	44	32	28	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
19	17	—	—	PTD6	KBI2P6			
20	18	—	—	PTD5	KBI2P5			
21	19	13	15	PTC1	TPM3CH1			
22	20	14	16	PTC0	TPM3CH0			
23	21	15	17	PTB3	KBI1P7	MOSI <sup>2</sup>		ADP7
24	22	16	18	PTB2	KBI1P6	SPSCK <sup>2</sup>		ADP6
25	23	17	19	PTB1	KBI1P5	TxD1		ADP5
26	24	18	20	PTB0	KBI1P4	RxD1		ADP4
27	25	19	21	PTA7	TPM2CH2			ADP9
28	26	20	22	PTA6	TPM1CH2			ADP8
29	—	—	—	PTE4				
30	27	—	—					V <sub>DD</sub>
31	28	—	—					V <sub>SS</sub>
32	29	—	—	PTD4	KBI2P4			
33	30	21	—	PTD3	KBI2P3			
34	31	22	—	PTD2	KBI2P2			
35	32	23	23	PTA3	KBI1P3	SCL <sup>1</sup>		ADP3
36	33	24	24	PTA2	KBI1P2	SDA <sup>1</sup>		ADP2
37	34	25	25	PTA1	KBI1P1	TPM2CH0	ADP1 <sup>3</sup>	ACMP1– <sup>3</sup>
38	35	26	26	PTA0	KBI1P0	TPM1CH0	ADP0 <sup>3</sup>	ACMP1+ <sup>3</sup>
39	36	27	27	PTC7	TxD2			ACMP2–
40	37	28	28	PTC6	RxD2			ACMP2+
41	—	—	—	PTE3	$\overline{SS}$ <sup>2</sup>			
42	38	—	—	PTE2	MISO <sup>2</sup>			
43	39	—	—	PTE1	MOSI <sup>2</sup>			
44	40	—	—	PTE0	TPM2CLK	SPSCK <sup>2</sup>		
45	41	29	1	PTC5	TPM3CH5			ACMP2O
46	42	30	2	PTC4	TPM3CH4			
47	43	31	3	PTA5	IRQ	TPM1CLK	$\overline{RESET}$	
48	44	32	4	PTA4	ACMP1O	BKGD	MS	

<sup>1</sup> IIC pins, SCL and SDA can be repositioned using IICPS in SOPT2; default reset locations are PTA3 and PTA2.

<sup>2</sup> SPI pins ( $\overline{SS}$ , MISO, MOSI, and SPSCK) can be repositioned using SPIPS in SOPT2. Default locations are PTB5, PTB4, PTB3, and PTB2.

<sup>3</sup> If ADC and ACMP1 are enabled, both modules will have access to the pin.

## 3 Electrical Characteristics

### 3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE32 series of microcontrollers available at the time of publication.

### 3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 2. Parameter Classifications**

<b>P</b>	Those parameters are guaranteed during production testing on each individual device.
<b>C</b>	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
<b>T</b>	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
<b>D</b>	Those parameters are derived mainly from simulations.

#### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

### 3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 3](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

**Table 3. Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	-0.3 to +3.8	V
Maximum current into $V_{DD}$	$I_{DD}$	120	mA
Digital input voltage	$V_{In}$	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	±25	mA
Storage temperature range	$T_{stg}$	-55 to 150	°C

<sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.

<sup>2</sup> All functional non-supply pins, except for PTA5 are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>3</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

### 3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.



Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T <sub>A</sub>	T <sub>L</sub> to T <sub>H</sub> −40 to 85	°C
Maximum junction temperature	T <sub>JM</sub>	95	°C
Thermal resistance Single-layer board			
48-pin QFN	θ <sub>JA</sub>	81	°C/W
44-pin LQFP		68	
32-pin LQFP		66	
32-pin QFN		92	
28-pin SOIC		57	
Thermal resistance Four-layer board			
48-pin QFN	θ <sub>JA</sub>	26	°C/W
44-pin LQFP		46	
32-pin LQFP		54	
32-pin QFN		33	
28-pin SOIC		42	

The average chip-junction temperature ( $T_J$ ) in  $^{\circ}\text{C}$  can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

$T_A$  = Ambient temperature,  $^{\circ}\text{C}$

$\theta_{JA}$  = Package thermal resistance, junction-to-ambient,  $^{\circ}\text{C/W}$

$P_D = P_{\text{int}} + P_{\text{I/O}}$

$P_{\text{int}} = I_{\text{DD}} \times V_{\text{DD}}$ , Watts — chip internal power

$P_{\text{I/O}}$  = Power dissipation on input and output pins — user determined

For most applications,  $P_{\text{I/O}} \ll P_{\text{int}}$  and can be neglected. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{\text{I/O}}$  is neglected) is:

$$P_D = K \div (T_J + 273^{\circ}\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^{\circ}\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving Equation 1 and Equation 2 iteratively for any value of  $T_A$ .

### 3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 5. ESD and Latch-up Test Conditions**

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	$\Omega$
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Machine	Series resistance	R1	0	$\Omega$
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

**Table 6. ESD and Latch-Up Protection Characteristics**

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{HBM}$	$\pm 2000$	—	V
2	Machine model (MM)	$V_{MM}$	$\pm 200$	—	V
3	Charge device model (CDM)	$V_{CDM}$	$\pm 500$	—	V
4	Latch-up current at $T_A = 85^\circ\text{C}$	$I_{LAT}$	$\pm 100$	—	mA

<sup>1</sup> Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

### 3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typical <sup>1</sup>	Max	Unit
1		Operating Voltage <div>V<sub>DD</sub> rising V<sub>DD</sub> falling</div>			2.0 1.8	—	3.6	V
2	C	Output high voltage <sup>2</sup> <div>All I/O pins, low-drive strength</div>	V <sub>OH</sub>	1.8 V, I <sub>Load</sub> = −2 mA	V <sub>DD</sub> − 0.5	—	—	V
	P	2.7 V, I <sub>Load</sub> = −10 mA		V <sub>DD</sub> − 0.5	—	—		
	T	2.3 V, I <sub>Load</sub> = −6 mA		V <sub>DD</sub> − 0.5	—	—		
	C	1.8V, I <sub>Load</sub> = −3 mA		V <sub>DD</sub> − 0.5	—	—		
3	D	Output high current Max total I <sub>OH</sub> for all ports	I <sub>OHT</sub>		—	—	100	mA
4	C	Output low voltage <div>All I/O pins, low-drive strength</div>	V <sub>OL</sub>	1.8 V, I <sub>Load</sub> = 2 mA	—	—	0.5	V
	P	2.7 V, I <sub>Load</sub> = 10 mA		—	—	0.5		
	T	2.3 V, I <sub>Load</sub> = 6 mA		—	—	0.5		
	C	1.8 V, I <sub>Load</sub> = 3 mA		—	—	0.5		
5	D	Output low current Max total I <sub>OL</sub> for all ports	I <sub>OLT</sub>		—	—	100	mA
6	P	Input high voltage all digital inputs	V <sub>IH</sub>	V <sub>DD</sub> > 2.3 V	0.70 x V <sub>DD</sub>	—	—	V
	C			V <sub>DD</sub> ≤ 1.8 V	0.85 x V <sub>DD</sub>	—	—	
7	P	Input low voltage all digital inputs	V <sub>IL</sub>	V <sub>DD</sub> > 2.7 V	—	—	0.35 x V <sub>DD</sub>	
	C			V <sub>DD</sub> ≤ 1.8 V	—	—	0.30 x V <sub>DD</sub>	
8	C	Input hysteresis all digital inputs	V <sub>hys</sub>		0.06 x V <sub>DD</sub>	—	—	mV
9	P	Input leakage current all input only pins (Per pin)	I <sub>In</sub>	V <sub>In</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	—	1	μA
10	P	Hi-Z (off-state) leakage current all input/output (per pin)	I <sub>OZ</sub>	V <sub>In</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	—	1	μA
11	C	Total leakage combined for all inputs and Hi-Z pins All input only and I/O	I <sub>OZTOT</sub>	V <sub>In</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	—	2	μA
11	P	Pullup, Pulldown resistors all digital inputs, when enabled	R <sub>PU</sub> , R <sub>PD</sub>		17.5	—	52.5	kΩ
12	D	DC injection current <sup>3, 4, 5</sup> Single pin limit	I <sub>IC</sub>	V <sub>IN</sub> < V <sub>SS</sub> , V <sub>IN</sub> > V <sub>DD</sub>	−0.2	—	0.2	mA
		Total MCU limit, includes sum of all stressed pins			−5	—	5	mA
13	C	Input Capacitance, all pins	C <sub>In</sub>		—	—	8	pF
14	C	RAM retention voltage	V <sub>RAM</sub>		—	0.6	1.0	V
15	C	POR re-arm voltage <sup>6</sup>	V <sub>POR</sub>		0.9	1.4	2.0	V

Table 7. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typical <sup>1</sup>	Max	Unit
16	D	POR re-arm time	$t_{POR}$		10	—	—	$\mu s$
17	P	Low-voltage detection threshold — high range	$V_{LVDH}$	$V_{DD}$ falling $V_{DD}$ rising	2.11 2.16	2.16 2.21	2.22 2.27	V
18	P	Low-voltage detection threshold — low range	$V_{LVDL}$	$V_{DD}$ falling $V_{DD}$ rising	1.80 1.88	1.82 1.90	1.91 1.99	V
19	P	Low-voltage warning threshold — high range	$V_{LVWH}$	$V_{DD}$ falling $V_{DD}$ rising	2.36 2.36	2.46 2.46	2.56 2.56	V
20	P	Low-voltage warning threshold — low range	$V_{LVWL}$	$V_{DD}$ falling $V_{DD}$ rising	2.11 2.16	2.16 2.21	2.22 2.27	V
21	C	Low-voltage inhibit reset/recover hysteresis	$V_{hys}$		—	80	—	mV
22	P	Bandgap Voltage Reference <sup>7</sup>	$V_{BG}$		1.15	1.17	1.18	V

<sup>1</sup> Typical values are measured at 25 °C. Characterized, not tested

<sup>2</sup> As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above  $V_{LVDL}$ .

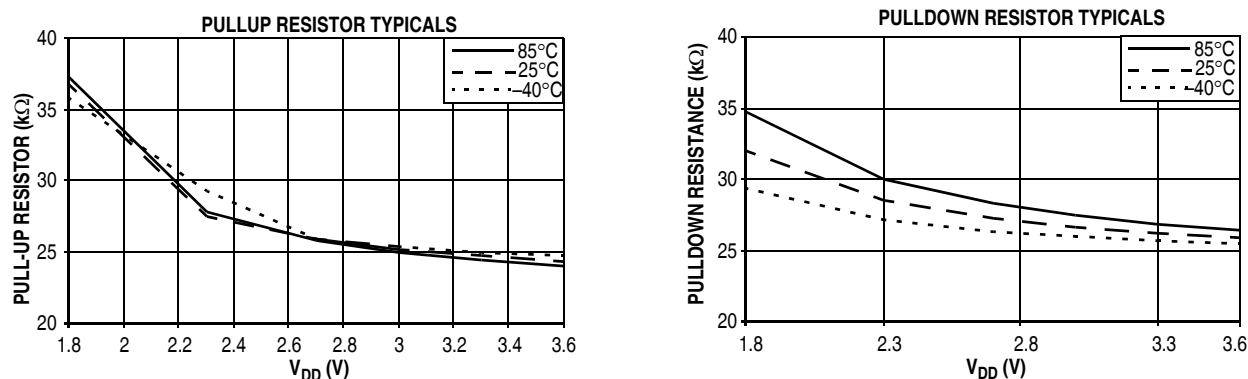
<sup>3</sup> All functional non-supply pins, except for PTA5 are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>4</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

<sup>5</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{in} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

<sup>6</sup> Maximum is highest voltage that POR is guaranteed.

<sup>7</sup> Factory trimmed at  $V_{DD} = 3.0$  V, Temp = 25 °C

Figure 6. Pullup and Pulldown Typical Resistor Values ( $V_{DD} = 3.0$  V)

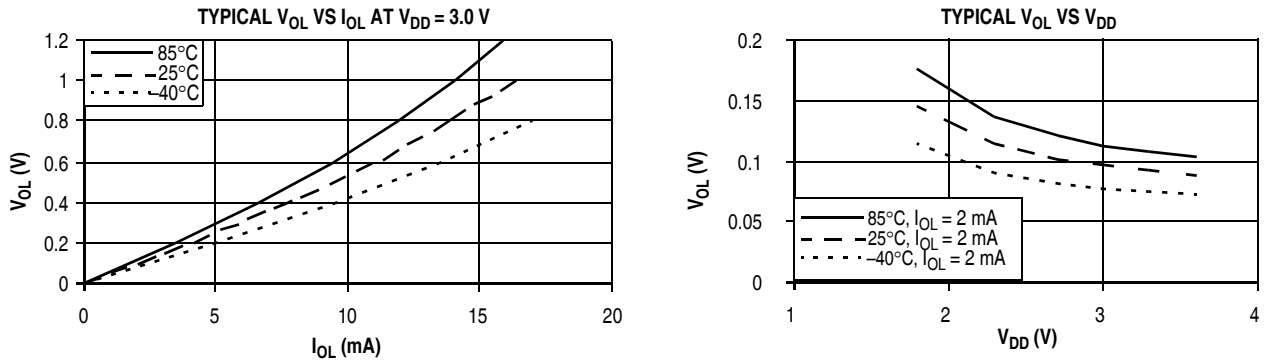


Figure 7. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

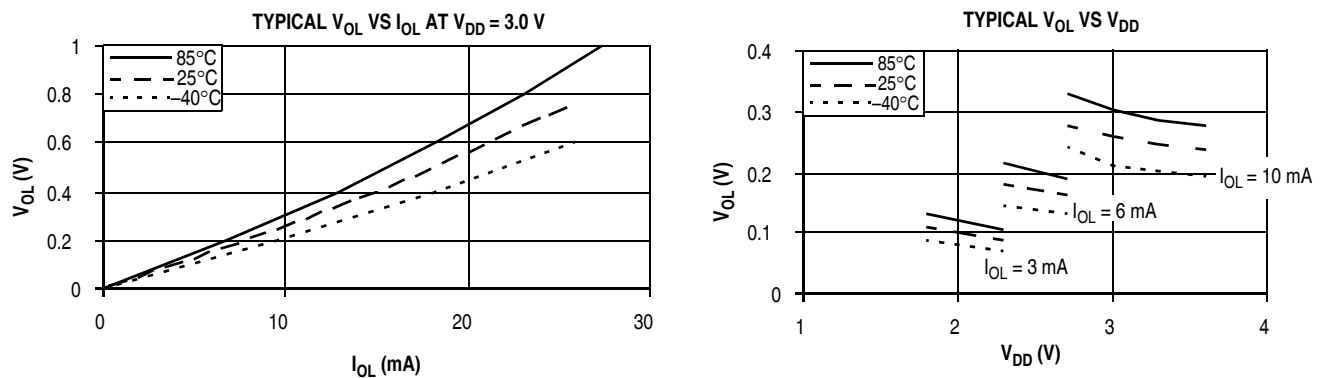


Figure 8. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

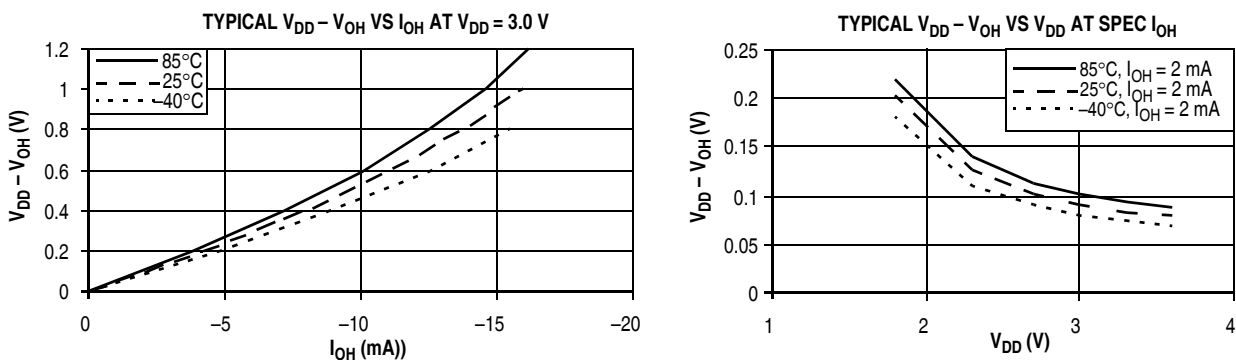


Figure 9. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V <sub>DD</sub> (V)	Typical <sup>1</sup>	Max	Unit	Temp (°C)
6	P	Stop2 mode supply current		S2I <sub>DD</sub>	—	3	0.35	0.65	μA	–40 to 25°C
	C				—		0.8	1.0		70
	P				—		2.0	4.5		85
	C				—	2	0.25	0.50		–40 to 25
	C				—		0.65	0.85		70
	C				—		1.5	3.5		85
7	P	Stop3 mode supply current no clocks active		S3I <sub>DD</sub>	—	3	0.45	1.00	μA	–40 to 25
	C				—		1.5	2.3		70
	P				—		4	8		85
	C				—	2	0.35	0.70		–40 to 25
	C				—		1	2		70
	C				—		3.5	6.0		85
8	T	Low power mode adders:	EREFSTEN=1		32 kHz	3	500	—	nA	–40 to 85
9	T		IREFSTEN=1		32 kHz		70	—	μA	
10	T		TPM PWM		100 Hz		12	—	μA	
11	T		SCI, SPI, or IIC		300 bps		15	—	μA	
12	T		RTC using LPO		1 kHz		200	—	nA	
13	T		RTC using IC SERCLK		32 kHz		1	—	μA	
14	T		LVD		n/a		100	—	μA	
15	T		ACMP		n/a		20	—	μA	

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				–40°C	25°C	70°C	85°C	
1	T	LPO	—	50	75	100	150	nA
2	T	EREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN <sup>1</sup>	—	63	70	77	81	μA
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD <sup>1</sup>	LVDSE = 1	90	100	110	115	μA
6	T	ACMP <sup>1</sup>	Not using the bandgap (BGBE = 0)	18	20	22	23	μA
7	T	ADC <sup>1</sup>	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	μA

<sup>1</sup> Not available in stop2 mode.

### 3.8 External Oscillator (XOSCVLP) Characteristics

Reference [Figure 11](#) and [Figure 12](#) for crystal or resonator circuits.

**Table 10. XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)**

Num	C	Characteristic	Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	$f_{lo}$ $f_{hi}$ $f_{hi}$	32 1 1	— — —	38.4 16 8	kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	$C_1$ $C_2$	See Note <sup>2</sup> See Note <sup>3</sup>			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0) <sup>2</sup> Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	$R_F$	— — —	— 10 1	— — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0) <sup>2</sup> Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	$R_S$	— — — — — — —	— 100 0 0 0 0 0	— — — 0 10 20	kΩ
5	C	Crystal start-up time <sup>4</sup> Low range, low power Low range, high power High range, low power High range, high power	$t_{CSTL}$ $t_{CSTH}$	— — — —	200 400 5 15	— — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	$f_{extal}$	0.03125 0	— —	40 40	MHz MHz

<sup>1</sup> Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.

<sup>2</sup> Load capacitors ( $C_1, C_2$ ), feedback resistor ( $R_F$ ) and series resistor ( $R_S$ ) are incorporated internally when RANGE=HGO=0.

<sup>3</sup> See crystal or resonator manufacturer's recommendation.

<sup>4</sup> Proper PC board layout procedures must be followed to achieve specifications.

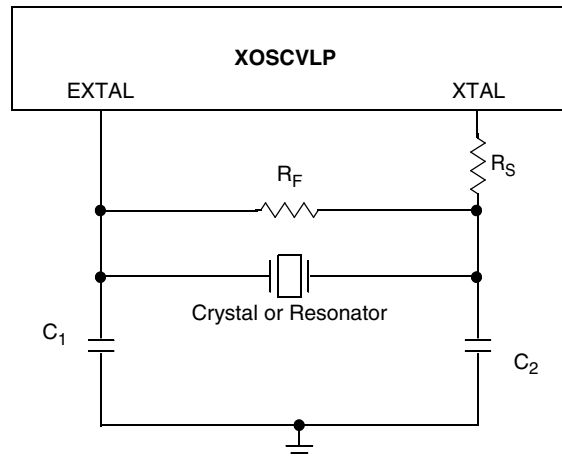


Figure 11. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

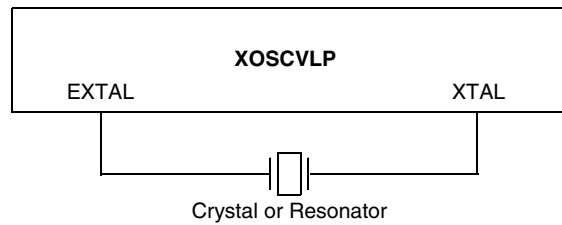


Figure 12. Typical Crystal or Resonator Circuit: Low Range/Low Power

### 3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range =  $-40$  to  $85^{\circ}\text{C}$  Ambient)

Num	C	Characteristic		Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	P	Average internal reference frequency — factory trimmed		$f_{\text{int}_t}$	—	32.768	—	kHz
2	C	Average internal reference frequency — untrimmed		$f_{\text{int}_{ut}}$	31.25	—	39.06	kHz
3	T	Internal reference start-up time		$t_{\text{IRST}}$	—	5	10	$\mu\text{s}$
4	P	DCO output frequency trimmed <sup>2</sup>	Low range (DFR = 00)	$f_{\text{dco}_u}$	16	—	20	MHz
	P		Mid range (DFR = 01)		32	—	40	
	P		High range (DFR = 10)		48	—	60	
5	P	DCO output frequency <sup>2</sup> reference = 32768 Hz and DMX32 = 1	Low range (DFR = 00)	$f_{\text{dco\_DMX32}}$	—	19.92	—	MHz
	P		Mid range (DFR = 01)		—	39.85	—	
	P		High range (DFR = 10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{\text{dco\_res}_t}$	—	$\pm 0.1$	$\pm 0.2$	$\%f_{\text{dco}}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{\text{dco\_res}_t}$	—	$\pm 0.2$	$\pm 0.4$	$\%f_{\text{dco}}$



Table 13. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	$f_{TCLK}$	0	$f_{Bus}/4$	Hz
2	D	External clock period	$t_{TCLK}$	4	—	$t_{cyc}$
3	D	External clock high time	$t_{clkh}$	1.5	—	$t_{cyc}$
4	D	External clock low time	$t_{clkl}$	1.5	—	$t_{cyc}$
5	D	Input capture pulse width	$t_{ICPW}$	1.5	—	$t_{cyc}$

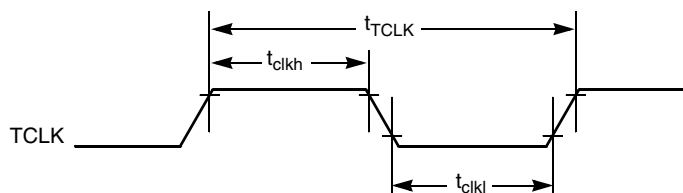


Figure 15. Timer External Clock

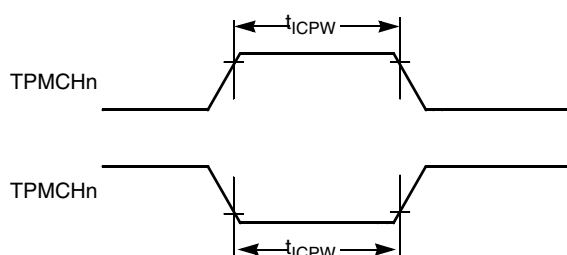


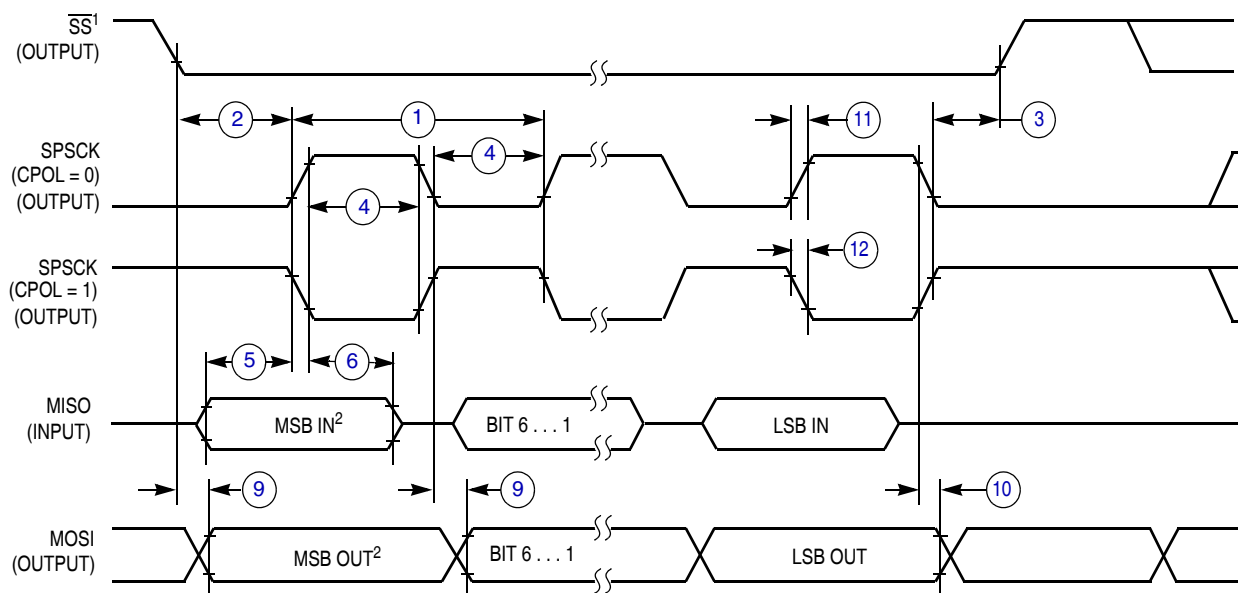
Figure 16. Timer Input Capture Pulse

### 3.10.3 SPI Timing

Table 14 and Figure 17 through Figure 20 describe the timing requirements for the SPI system.

Table 14. SPI Timing

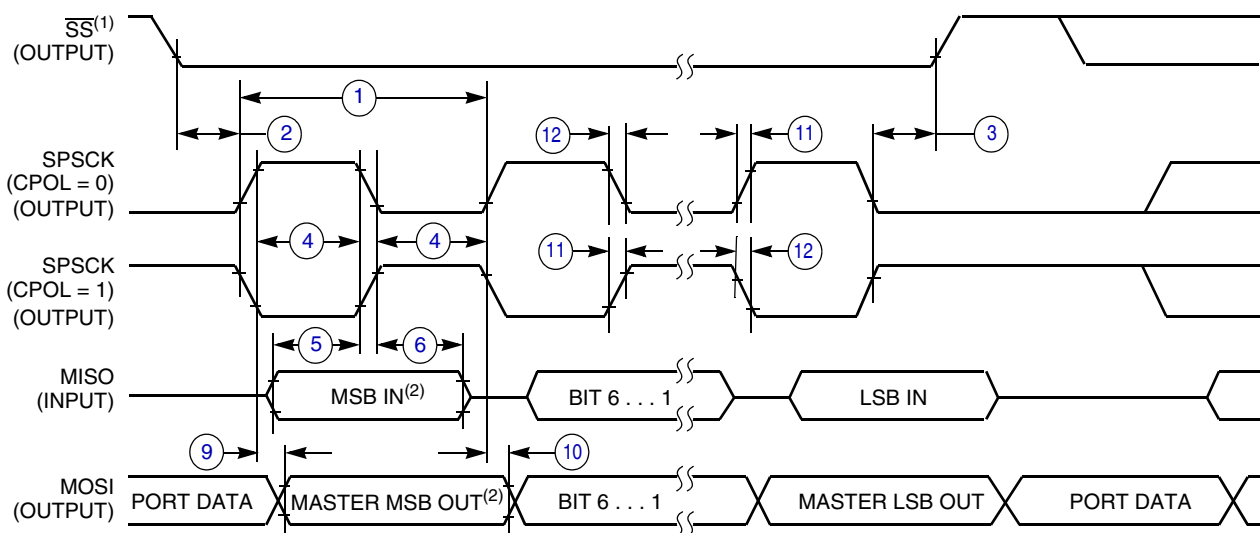
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	$f_{op}$	$f_{Bus}/2048$ 0	$f_{Bus}/2^1$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	$t_{SPSCK}$	2 4	2048 —	$t_{cyc}$ $t_{cyc}$
2	D	Enable lead time Master Slave	$t_{Lead}$	1/2 1	— —	$t_{SPSCK}$ $t_{cyc}$
3	D	Enable lag time Master Slave	$t_{Lag}$	1/2 1	— —	$t_{SPSCK}$ $t_{cyc}$



NOTES:

1.  $\overline{SS}$  output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI Master Timing (CPHA = 0)



NOTES:

1.  $\overline{SS}$  output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI Master Timing (CPHA = 1)

Table 17. ADC Characteristics ( $V_{REFH} = V_{DDAD}$ ,  $V_{REFL} = V_{SSAD}$ ) (continued)

C	Characteristic	Conditions	Symbol	Min	Typ <sup>1</sup>	Max	Unit	Comment
P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t <sub>ADC</sub>	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long sample (ADLSMP = 1)		—	40	—		
P	Sample time	Short sample (ADLSMP = 0)	t <sub>ADS</sub>	—	3.5	—	ADCK cycles	
		Long sample (ADLSMP = 1)		—	23.5	—		
D	Temp sensor slope	–40 °C– 25 °C	m	—	1.646	—	mV/°C	
		25 °C– 85 °C		—	1.769	—		
D	Temp sensor voltage	25 °C	V <sub>TEMP25</sub>	—	701.2	—	mV	
T	Total unadjusted error	12-bit mode, 3.6> V <sub>DDAD</sub> > 2.7	E <sub>TUE</sub>	—	–1 to 3	–2.5 to 5.5	LSB <sup>2</sup>	Includes quantization
T		12-bit mode, 2.7> V <sub>DDAD</sub> > 1.8V		—	–1 to 3	–3.0 to 6.5		
P		10-bit mode		—	±1	±2.5		
P		8-bit mode		—	±0.5	±1.0		
T	Differential non-linearity	12-bit mode	DNL	—	±1.0	–1.5 to 2.0	LSB <sup>2</sup>	
P		10-bit mode <sup>3</sup>		—	±0.5	±1.0		
P		8-bit mode <sup>3</sup>		—	±0.3	±0.5		
T	Integral non-linearity	12-bit mode	INL	—	±1.5	–2.5 to 2.75	LSB <sup>2</sup>	
T		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		
T	Zero-scale error	12-bit mode	E <sub>ZS</sub>	—	±1.5	±2.5	LSB <sup>2</sup>	V <sub>ADIN</sub> = V <sub>SSAD</sub>
P		10-bit mode		—	±0.5	±1.5		
P		8-bit mode		—	±0.5	±0.5		
T	Full-scale error	12-bit mode	E <sub>FS</sub>	—	±1.0	–3.5 to 1.0	LSB <sup>2</sup>	V <sub>ADIN</sub> = V <sub>DDAD</sub>
P		10-bit mode		—	±0.5	±1		
P		8-bit mode		—	±0.5	±0.5		
D	Quantization error	12-bit mode	E <sub>Q</sub>	—	–1 to 0	—	LSB <sup>2</sup>	
		10-bit mode		—	—	±0.5		
		8-bit mode		—	—	±0.5		
D	Input leakage error	12-bit mode	E <sub>IL</sub>	—	±2	—	LSB <sup>2</sup>	Pad leakage <sup>4</sup> * R <sub>AS</sub>
		10-bit mode		—	±0.2	±4		
		8-bit mode		—	±0.1	±1.2		

<sup>1</sup> Typical values assume  $V_{DDAD} = 3.0\text{ V}$ ,  $\text{Temp} = 25\text{ }^{\circ}\text{C}$ ,  $f_{ADCK} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup>  $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$

<sup>3</sup> Monotonicity and No-missing-codes guaranteed in 10-bit and 8-bit modes

<sup>4</sup> Based on input pad leakage current. Refer to pad electricals.

### 3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for flash memory.

Program and erase operations do not require any special power sources other than the normal  $V_{DD}$  supply. For more detailed information about program/erase operations, see MC9S08QE32 Series Reference Manual Chapter 4 Memory.

**Table 18. Flash Characteristics**

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{\text{prog/erase}}$	1.8	—	3.6	V
D	Supply voltage for read operation	$V_{\text{Read}}$	1.8	—	3.6	V
D	Internal FCLK frequency <sup>1</sup>	$f_{\text{FCLK}}$	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	$t_{\text{Fcyc}}$	5	—	6.67	μs
P	Byte program time (random location) <sup>(2)</sup>	$t_{\text{prog}}$	9			$t_{\text{Fcyc}}$
P	Byte program time (burst mode) <sup>(2)</sup>	$t_{\text{Burst}}$	4			$t_{\text{Fcyc}}$
P	Page erase time <sup>2</sup>	$t_{\text{Page}}$	4000			$t_{\text{Fcyc}}$
P	Mass erase time <sup>(2)</sup>	$t_{\text{Mass}}$	20,000			$t_{\text{Fcyc}}$
	Byte program current <sup>3</sup>	$R_{\text{IDDBP}}$	—	4	—	mA
	Page erase current <sup>3</sup>	$R_{\text{IDDEPE}}$	—	6	—	mA
C	Program/erase endurance <sup>4</sup> $T_L$ to $T_H = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ $T = 25\text{ }^{\circ}\text{C}$		10,000	— 100,000	— —	cycles
C	Data retention <sup>5</sup>	$t_{\text{D\_ret}}$	15	100	—	years

<sup>1</sup> The frequency of this clock is controlled by software setting.

<sup>2</sup> These values are hardware state machine controlled. User code does not need to count cycles. This information is supplied for calculating approximate time to program and erase.

<sup>3</sup> The program and erase currents are additional to the standard run  $I_{DD}$ . These values are measured at room temperatures with  $V_{DD} = 3.0\text{ V}$ , bus frequency = 4.0 MHz.

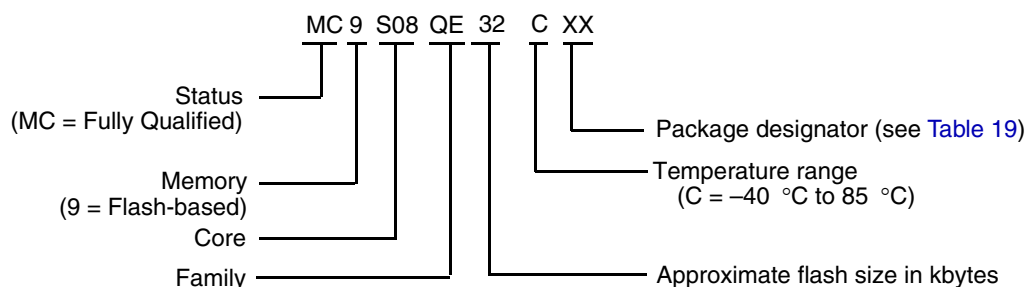
<sup>4</sup> **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

<sup>5</sup> **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

## 4 Ordering Information

This section contains ordering information for the MC9S08QE32 series of MCUs.

Example of the device numbering system:



## 5 Package Information

Table 19. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
48	Quad Flat No-Leads	QFN	FT	1314	<a href="#">98ARH99048A</a>
44	Low Quad Flat Package	LQFP	LD	824D	<a href="#">98ASS23225W</a>
32	Low Quad Flat Package	LQFP	LC	873A	<a href="#">98ASH70029A</a>
32	Quad Flat No-Leads	QFN	FM	1582	<a href="#">98ARE10566D</a>
28	Small Outline Integrated Circuit	SOIC	WL	751F	<a href="#">98ASB42345B</a>

### 5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 19. For the latest available drawings please visit our web site (<http://www.freescale.com>) and enter the package's document number into the keyword search box.