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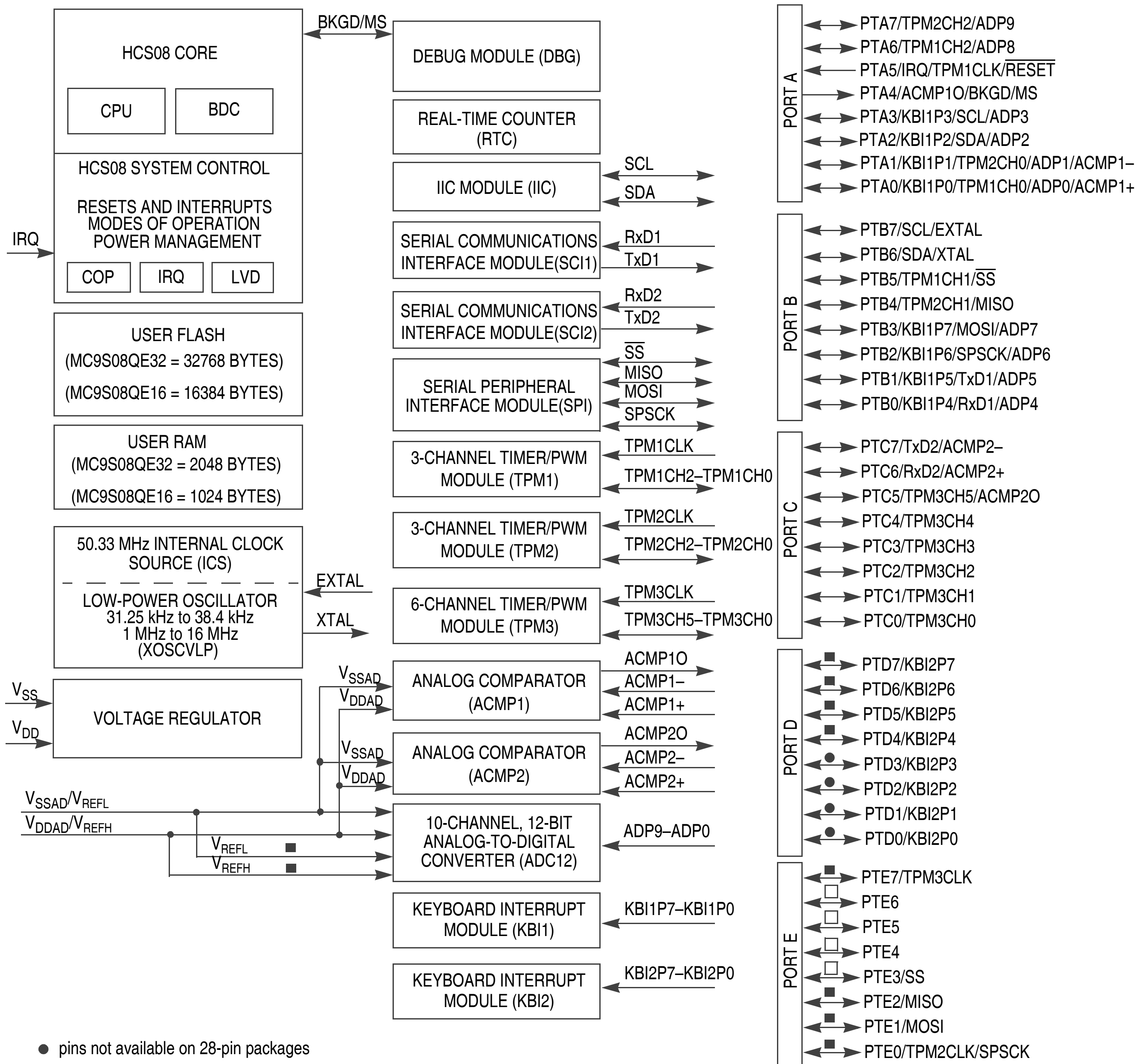
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qe32cwl

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08QE32 MCU.



● pins not available on 28-pin packages

■ pins not available on 28-pin or 32-pin packages

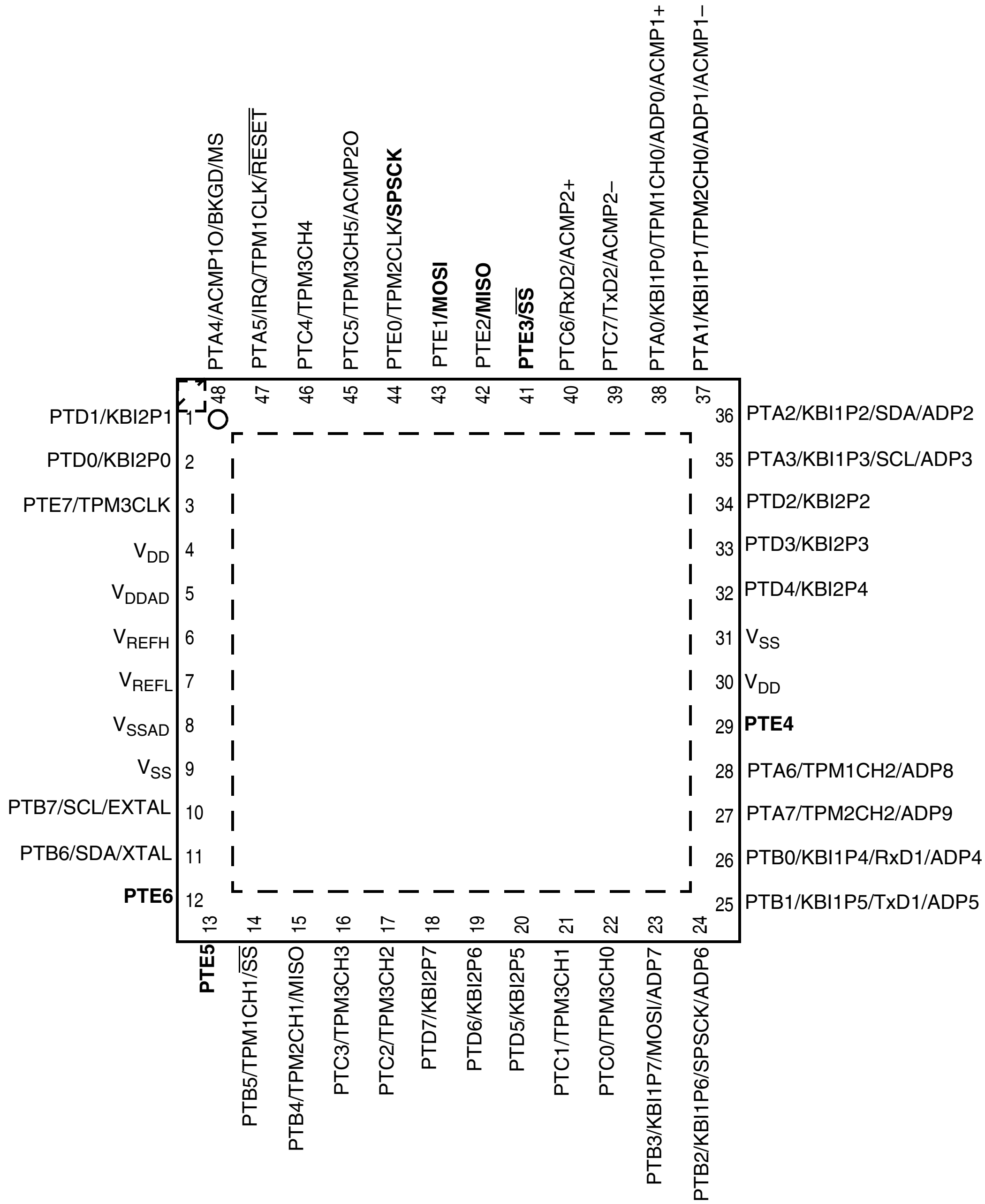
□ pins not available on 28-pin, 32-pin, or 44-pin packages

Notes: When PTA5 is configured as RESET, pin becomes bi-directional with output being open-drain drive containing an internal pullup device.
When PTA4 is configured as BKGD, pin becomes bi-directional.
For the 28-pin packages, V_{SSAD}/V_{REFL} and V_{DDAD}/V_{REFH} are double bonded to V_{SS} and V_{DD} respectively.
The 48-pin package is the only package with the option of having the SPI pins (SS, MISO, MOSI, and SPSCK) available on PTE3-0 pins.

Figure 1. MC9S08QE32 Series Block Diagram

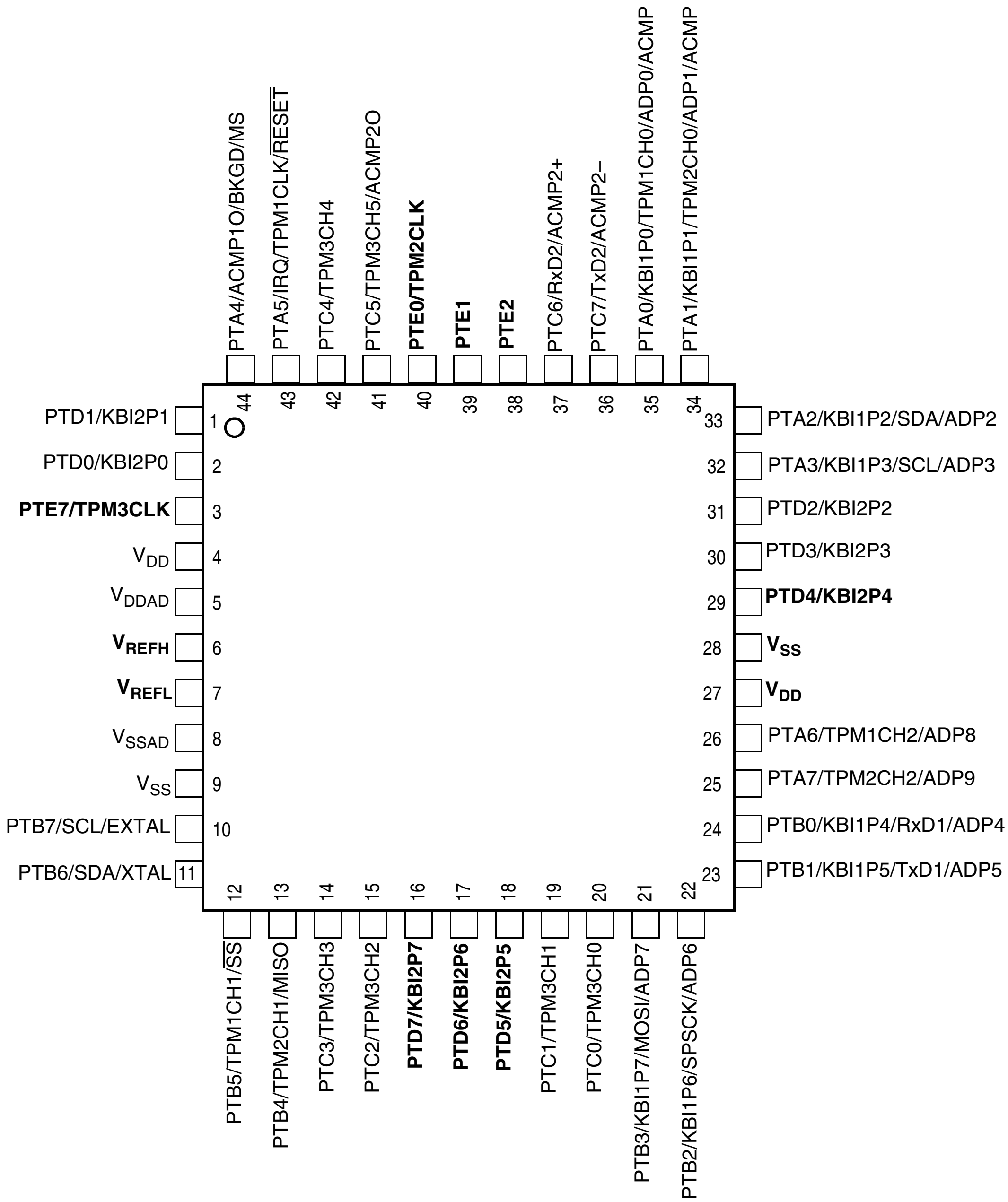
2 Pin Assignments

This section shows the pin assignments for the MC9S08QE32 series devices.



Pins in **bold** are lost in the next lower pin count package.

Figure 2. 48-Pin QFN



Pins in **bold** are lost in the next lower pin count package.

Figure 3. 44-Pin LQFP

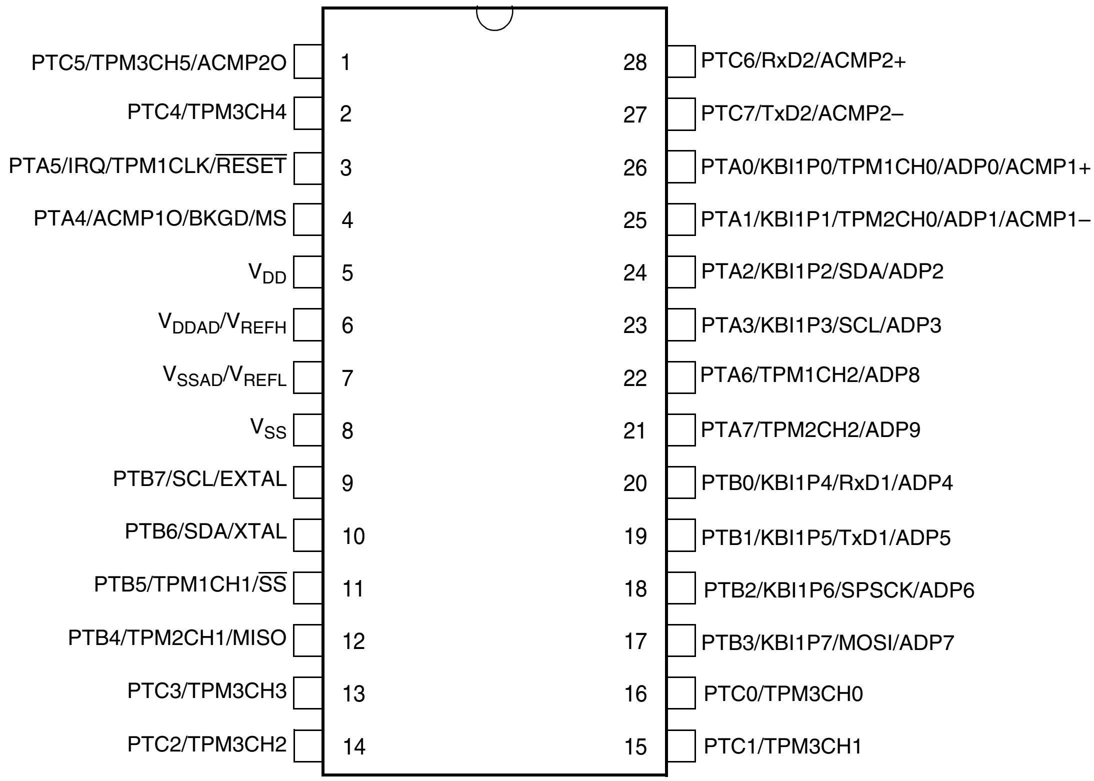


Figure 5. 28-Pin SOIC

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority

Pin Number				<-- Lowest	Priority	--> Highest		
48	**44**	**32**	**28**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	—	PTD1	KBI2P1			
2	2	2	—	PTD0	KBI2P0			
3	3	—	—	PTE7	TPM3CLK			
4	4	3	5					V_{DD}
5	5	4	6					V_{DDAD}
6	6							V_{REFH}
7	7	5	7					V_{REFL}
8	8							V_{SSAD}
9	9	6	8					V_{SS}
10	10	7	9	PTB7	SCL[1]			EXTAL
11	11	8	10	PTB6	SDA[1]			XTAL
12	—	—	—	PTE6				
13	—	—	—	PTE5				
14	12	9	11	PTB5	TPM1CH1	SS[2]		
15	13	10	12	PTB4	TPM2CH1	MISO[2]		
16	14	11	13	PTC3	TPM3CH3			
17	15	12	14	PTC2	TPM3CH2			
18	16	—	—	PTD7	KBI2P7			

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority (continued)

Pin Number				<-- Lowest **Priority** --> Highest				
48	**44**	**32**	**28**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
19	17	—	—	PTD6	KBI2P6			
20	18	—	—	PTD5	KBI2P5			
21	19	13	15	PTC1	TPM3CH1			
22	20	14	16	PTC0	TPM3CH0			
23	21	15	17	PTB3	KBI1P7	MOSI[2]		ADP7
24	22	16	18	PTB2	KBI1P6	SPSCK[2]		ADP6
25	23	17	19	PTB1	KBI1P5	TxD1		ADP5
26	24	18	20	PTB0	KBI1P4	RxD1		ADP4
27	25	19	21	PTA7	TPM2CH2			ADP9
28	26	20	22	PTA6	TPM1CH2			ADP8
29	—	—	—	PTE4				
30	27	—	—					V_{DD}
31	28	—	—					V_{SS}
32	29	—	—	PTD4	KBI2P4			
33	30	21	—	PTD3	KBI2P3			
34	31	22	—	PTD2	KBI2P2			
35	32	23	23	PTA3	KBI1P3	SCL[1]		ADP3
36	33	24	24	PTA2	KBI1P2	SDA[1]		ADP2
37	34	25	25	PTA1	KBI1P1	TPM2CH0	ADP1[3]	ACMP1–[3]
38	35	26	26	PTA0	KBI1P0	TPM1CH0	ADP0[3]	ACMP1+[3]
39	36	27	27	PTC7	TxD2			ACMP2–
40	37	28	28	PTC6	RxD2			ACMP2+
41	—	—	—	PTE3	$\overline{SS}$[2]			
42	38	—	—	PTE2	MISO[2]			
43	39	—	—	PTE1	MOSI[2]			
44	40	—	—	PTE0	TPM2CLK	SPSCK[2]		
45	41	29	1	PTC5	TPM3CH5			ACMP2O
46	42	30	2	PTC4	TPM3CH4			
47	43	31	3	PTA5	IRQ	TPM1CLK	$\overline{RESET}$	
48	44	32	4	PTA4	ACMP1O	BKGD	MS	

1 IIC pins, SCL and SDA can be repositioned using IICPS in SOPT2; default reset locations are PTA3 and PTA2.

2 SPI pins ($\overline{SS}$, MISO, MOSI, and SPSCK) can be repositioned using SPIPS in SOPT2. Default locations are PTB5, PTB4, PTB3, and PTB2.

3 If ADC and ACMP1 are enabled, both modules will have access to the pin.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE32 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 7. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typical[1]	Max	Unit
1		Operating Voltage	V_{DD} rising V_{DD} falling			2.0 1.8	—	3.6	V
2	C	Output high voltage[2]	All I/O pins, low-drive strength	V_{OH}	1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	T				2.3 V, I_{Load} = –6 mA	V_{DD} – 0.5	—	—	
	C				1.8V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	1.8 V, I_{Load} = 2 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		2.7 V, I_{Load} = 10 mA	—	—	0.5	
	T				2.3 V, I_{Load} = 6 mA	—	—	0.5	
	C				1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
6	P	Input high voltage	all digital inputs	V_{IH}	$V_{DD} > 2.3$ V	0.70 x V_{DD}	—	—	V
	C				$V_{DD} \le 1.8$ V	0.85 x V_{DD}	—	—	
7	P	Input low voltage	all digital inputs	V_{IL}	$V_{DD} > 2.7$ V	—	—	0.35 x V_{DD}	
	C				$V_{DD} \le 1.8$ V	—	—	0.30 x V_{DD}	
8	C	Input hysteresis	all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
9	P	Input leakage current	all input only pins (Per pin)	$\|I_{In}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
10	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$\|I_{OZ}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
11	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	$\|I_{OZTOT}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	2	μA
11	P	Pullup, Pulldown resistors	all digital inputs, when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
12	D	DC injection current[3, 4, 5]	Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
13	C	Input Capacitance, all pins		C_{In}		—	—	8	pF
14	C	RAM retention voltage		V_{RAM}		—	0.6	1.0	V
15	C	POR re-arm voltage[6]		V_{POR}		0.9	1.4	2.0	V

Table 7. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typical[1]	Max	Unit
16	D	POR re-arm time	t_{POR}		10	—	—	μs
17	P	Low-voltage detection threshold — high range	V_{LVDH}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
18	P	Low-voltage detection threshold — low range	V_{LVDL}	V_{DD} falling V_{DD} rising	1.80 1.88	1.82 1.90	1.91 1.99	V
19	P	Low-voltage warning threshold — high range	V_{LVWH}	V_{DD} falling V_{DD} rising	2.36 2.36	2.46 2.46	2.56 2.56	V
20	P	Low-voltage warning threshold — low range	V_{LVWL}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
21	C	Low-voltage inhibit reset/recover hysteresis	V_{hys}		—	80	—	mV
22	P	Bandgap Voltage Reference[7]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C

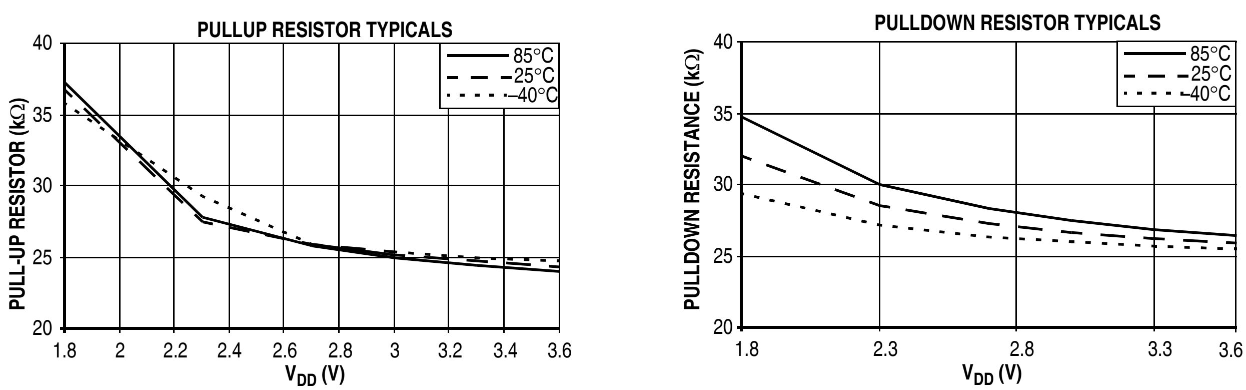


Figure 6. Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

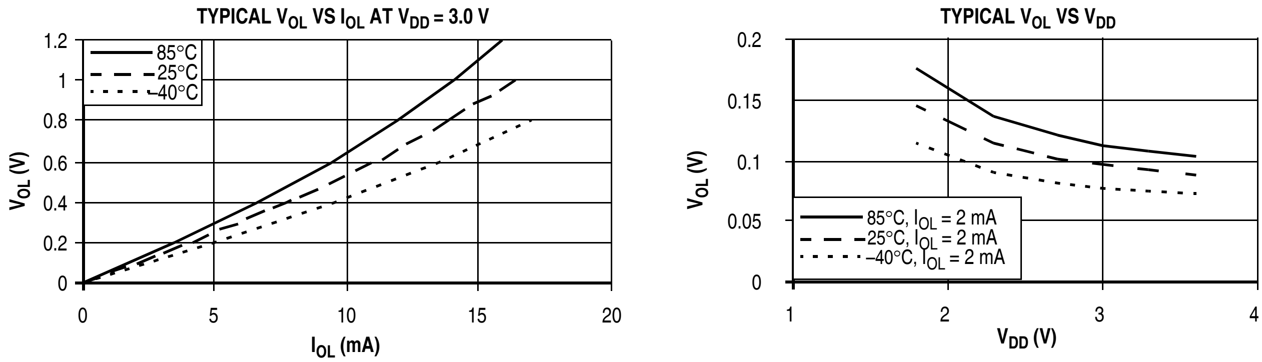


Figure 7. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

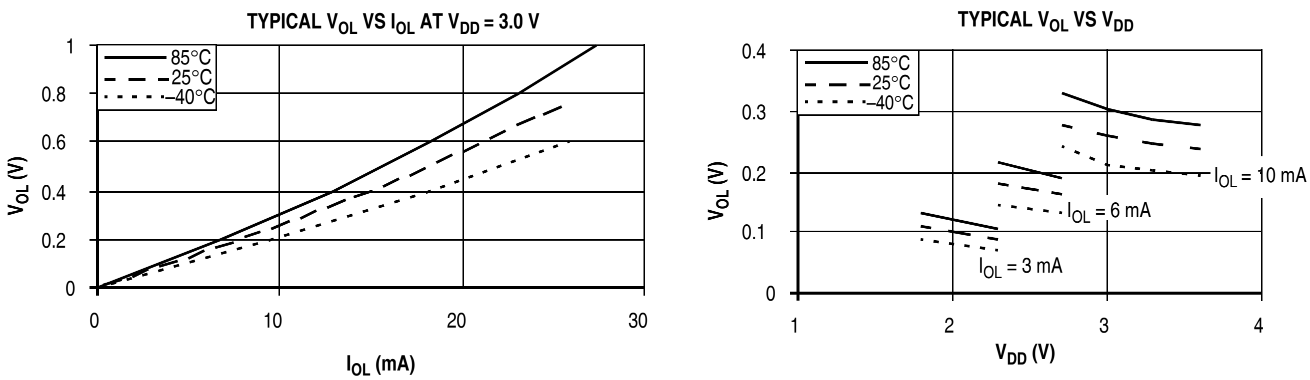


Figure 8. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

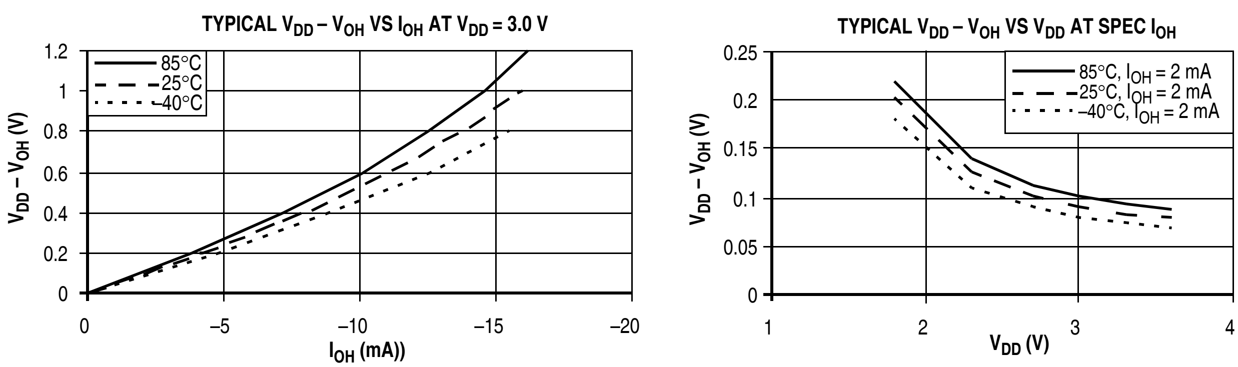


Figure 9. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

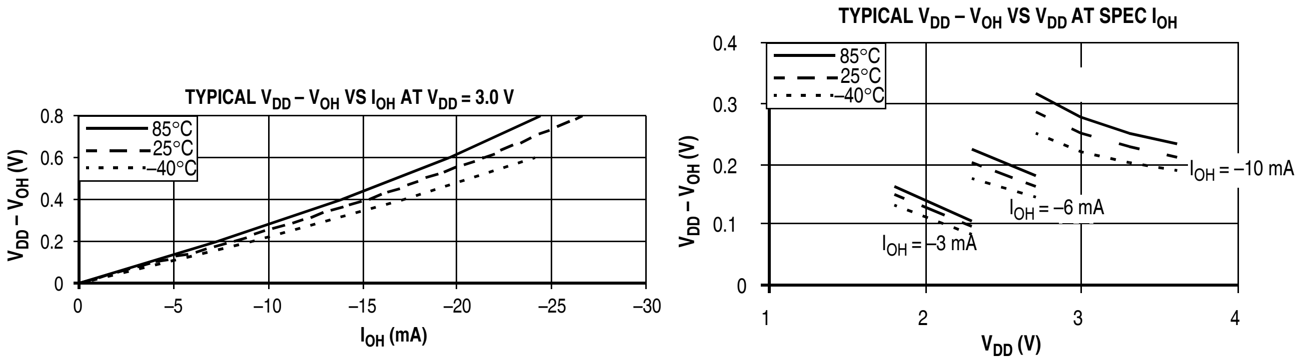


Figure 10. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25.165 MHz	3	13	14	mA	–40 to 25
	P					14	15		85
	T			20 MHz		13.75	—		–40 to 85
	T			8 MHz		5.59	—		
	T			1 MHz		1.03	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25.165 MHz	3	11.5	12.3	mA	–40 to 85
	T			20 MHz		9.5	—		
	T			8 MHz		4.6	—		
	T			1 MHz		1.0	—		
3	T	Run supply current LPRS = 0, all modules off	RI_{DD}	16 kHz FBILP	3	152	—	μA	–40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPRS = 1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	21.9	—	μA	–40 to 85
	T	Run supply current LPRS = 1, all modules off, running from RAM				7.3	—		
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25.165 MHz	3	5.74	6.00	mA	--40 to 85
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
6	P	Stop2 mode supply current		$S2I_{DD}$	—	3	0.35	0.65	μA	–40 to 25C
	C				—		0.8	1.0		70
	P				—		2.0	4.5		85
	C				—	2	0.25	0.50		–40 to 25
	C				—		0.65	0.85		70
	C				—		1.5	3.5		85
7	P	Stop3 mode supply current no clocks active		$S3I_{DD}$	—	3	0.45	1.00	μA	–40 to 25
	C				—		1.5	2.3		70
	P				—		4	8		85
	C				—	2	0.35	0.70		–40 to 25
	C				—		1	2		70
	C				—		3.5	6.0		85
8	T	Low power mode adders:	EREFSTEN=1		32 kHz	3	500	—	nA	–40 to 85
9	T		IREFSTEN=1		32 kHz		70	—	μA	
10	T		TPM PWM		100 Hz		12	—	μA	
11	T		SCI, SPI, or IIC		300 bps		15	—	μA	
12	T		RTC using LPO		1 kHz		200	—	nA	
13	T		RTC using ICSERCLK		32 kHz		1	—	μA	
14	T		LVD		n/a		100	—	μA	
15	T		ACMP		n/a		20	—	μA	

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				–40°C	**25**°C	**70**°C	**85**°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]	—	63	70	77	81	μA
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	μA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	22	23	μA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	μA

1 Not available in stop2 mode.

3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits.

Table 10. XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1 C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	t_{CSTL} t_{CSTH}	 — — — —	 200 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	 0.03125 0	 — —	 40 40	 MHz MHz

1 Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.
2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.
3 See crystal or resonator manufacturer's recommendation.
4 Proper PC board layout procedures must be followed to achieve specifications.

Table 13. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

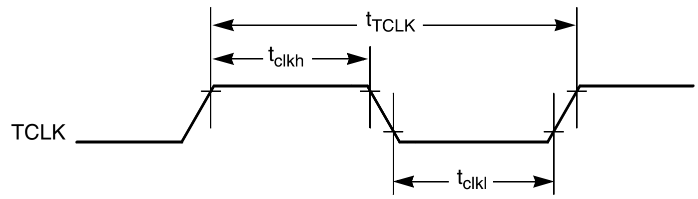


Figure 15. Timer External Clock

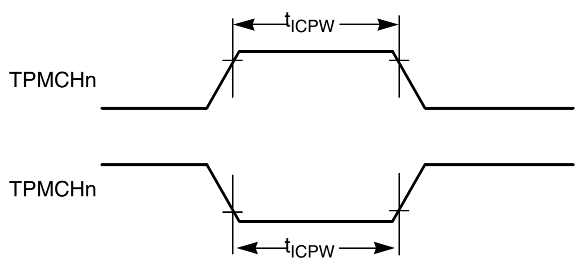


Figure 16. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 14 and Figure 17 through Figure 20 describe the timing requirements for the SPI system.

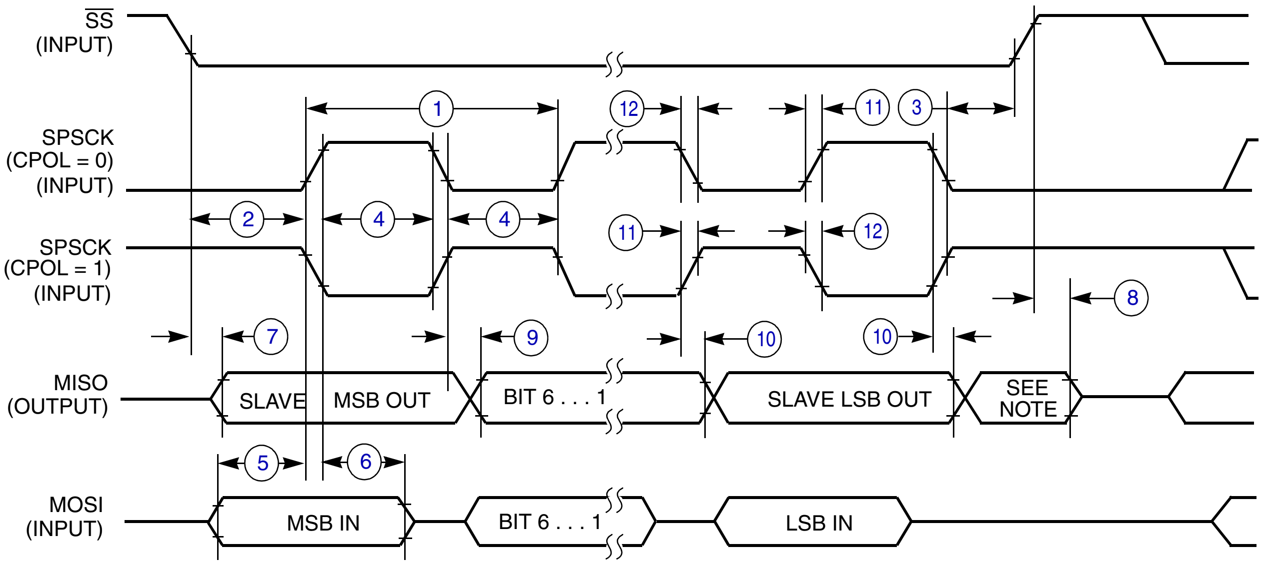
Table 14. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$[1] $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}

Table 14. SPI Timing (continued)

No.	C	Function	Symbol	Min	Max	Unit
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	t_{cyc} – 30 t_{cyc} – 30	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	t_{cyc} – 25 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	t_{cyc} – 25 25	ns ns

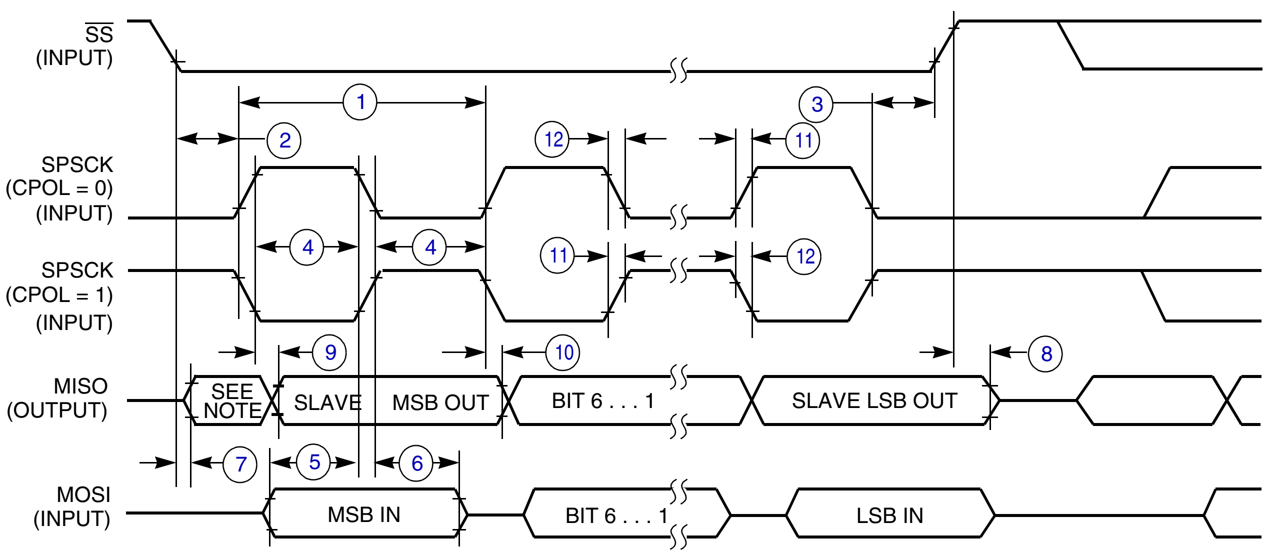
[1] Max operating frequency limited to 8 MHz when input filter disabled and high output drive strength enabled. Max operating frequency limited to 5 MHz when input filter enabled and high output drive strength disabled.



NOTE:

1. Not defined but normally MSB of character just received

Figure 19. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 20. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 15. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
P	Supply current (active)	I_{DDAC}	—	20	35	µA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}	—	20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs

3.12 ADC Characteristics

Table 16. 12-Bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	—
D	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDAD})[2]	ΔV_{DDAD}	–100	0	100	mV	—
D	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSAD})[2]	ΔV_{SSAD}	–100	0	100	mV	—
D	Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
C	Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
C	Input resistance	—	R_{ADIN}	—	5	7	kΩ	—
C	Analog source resistance	12-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
C	Analog source resistance	10-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	— —	— —	5 10	kΩ	External to MCU
C	Analog source resistance	8-bit mode (all valid f_{ADCK})	R_{AS}	—	—	10	kΩ	External to MCU
D	ADC conversion clock freq.	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
D	ADC conversion clock freq.	Low power (ADLPC = 1)	f_{ADCK}	0.4	—	4.0	MHz	—

1 Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

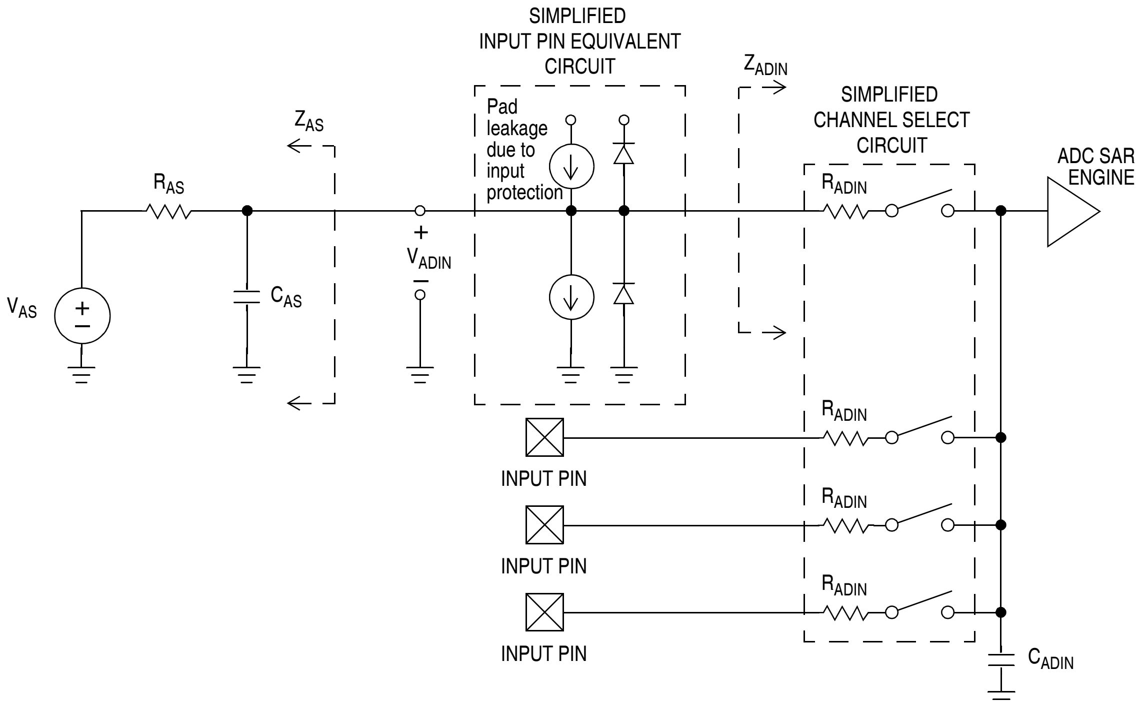


Figure 21. ADC Input Impedance Equivalency Diagram

Table 17. ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	120	—	µA	
T	Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	202	—	µA	
T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	288	—	µA	
P	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	0.532	1	mA	
P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low power (ADLPC = 1)		1.25	2	3.3		

[1] Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] 1 LSB = $(V_{REFH} – V_{REFL})/2^N$

[3] Monotonicity and No-missing-codes guaranteed in 10-bit and 8-bit modes

[4] Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see MC9S08QE32 Series Reference Manual Chapter 4 Memory.

Table 18. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
P	Byte program time (random location)(2)	t_{prog}		9		t_{Fcyc}
P	Byte program time (burst mode)(2)	t_{Burst}		4		t_{Fcyc}
P	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
P	Mass erase time(2)	t_{Mass}		20,000		t_{Fcyc}
	Byte program current[3]	R_{IDDBP}	—	4	—	mA
	Page erase current[3]	R_{IDDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40 °C to 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

[1] The frequency of this clock is controlled by software setting.

[2] These values are hardware state machine controlled. User code does not need to count cycles. This information is supplied for calculating approximate time to program and erase.

[3] The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

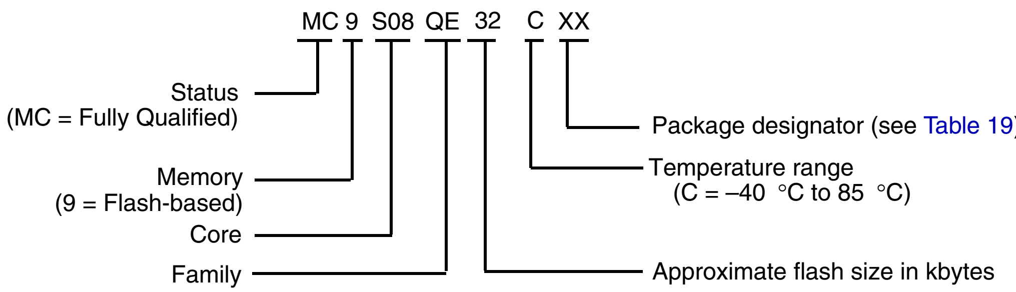
[4] **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

[5] **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

4 Ordering Information

This section contains ordering information for the MC9S08QE32 series of MCUs.

Example of the device numbering system:



5 Package Information

Table 19. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
48	Quad Flat No-Leads	QFN	FT	1314	98ARH99048A
44	Low Quad Flat Package	LQFP	LD	824D	98ASS23225W
32	Low Quad Flat Package	LQFP	LC	873A	98ASH70029A
32	Quad Flat No-Leads	QFN	FM	1582	98ARE10566D
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B

5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 19. For the latest available drawings please visit our web site (http://www.freescale.com) and enter the package's document number into the keyword search box.