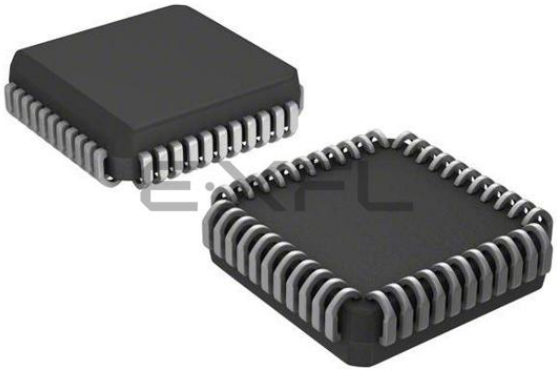


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp51-20ju

not accessible while DMEN = 0. FDATA can be accessed only by 16-bit (MOVX @DPTR) addresses. MOVX @Ri instructions to the FDATA address range will access external memory. Addresses above the FDATA range are mapped to XDATA.

3.3.2.1 *Write Protocol*

The FDATA address space accesses an internal nonvolatile data memory. This address space can be read just like EDATA by issuing a MOVX A,@DPTR; however, writes to FDATA require a more complex protocol and take several milliseconds to complete.

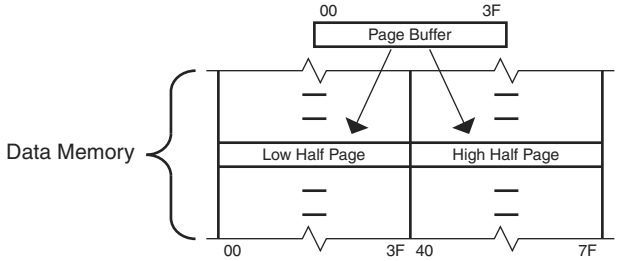
For internal execution the AT89LP51/52 uses an *idle-while-write* architecture where the CPU is placed in an idle state while the write occurs. When the write completes, the CPU will continue executing with the instruction after the MOVX @DPTR,A instruction that started the write. All peripherals will continue to function during the write cycle; however, interrupts will not be serviced until the write completes.

For external execution the AT89LP51/52 uses an *execute-while-write* architecture where the CPU continues to operate while the write occurs. The software should poll the state of the $\overline{\text{BUSY}}$ flag to determine when the write completes. Interrupts must be disabled during the write sequence as the CPU will not be able to vector to the internal interrupt table and care should be taken that the application does not jump to an internal address until the write completes.

To enable write access to the nonvolatile data memory, the MWEN bit (MEMCON.4) must be set to one. When MWEN = 1 and DMEN = 1, MOVX @DPTR,A may be used to write to FDATA. FDATA uses flash memory with a page-based programming model. Flash data memory differs from traditional EEPROM data memory in the method of writing data. EEPROM generally can update a single byte with any value. Flash memory splits programming into write and erase operations. A Flash write can only program zeroes, i.e change ones into zeroes ($1 \rightarrow 0$). Any ones in the write data are ignored. A Flash erase sets an entire page of data to ones so that all bytes become FFH. Therefore after an erase, each byte in the page can only be written once with any possible value. Bytes can be overwritten without an erase as long as only ones are changed into zeroes. However, if even a single bit needs updating from zero to one ($0 \rightarrow 1$); then the contents of the page must first be saved, the entire page must be erased and the zero bits in all bytes (old and new data combined) must be written. Avoiding unnecessary page erases greatly improves the endurance of the memory..

The AT89LP51/52 includes 2 data pages of 128 bytes each. One or more bytes in a page may be written at one time. The AT89LP51/52 includes a temporary page buffer of 64 bytes, or half of a page. Because the page buffer is 64 bytes long, the maximum number of bytes written at one time is 64. Therefore, two write cycles are required to fill the entire 128-byte page, one for the low half page (00H–3FH) and one for the high half page (40H–7FH) as shown in Figure 3-7.

Figure 3-7. Page Programming Structure



6.4 System Clock Divider

The CDV_{2-0} bits in CLKREG allow the system clock to be divided down from the selected clock source by powers of 2. The clock divider provides users with a greater frequency range when using the Internal Oscillator. For example, to achieve a 230.4 kHz system frequency when using the RC oscillator, CDV_{2-0} should be set to 011B for divide-by-8 operation. The divider can also be used to reduce power consumption by decreasing the operational frequency during non-critical periods. The resulting system frequency is given by the following equation:

$$f_{SYS} = \frac{f_{OSC}}{2^{CDV}}$$

where f_{OSC} is the frequency of the selected clock source. The clock divider will prescale the clock for the CPU and all peripherals. The value of CDV may be changed at any time without interrupting normal execution. Changes to CDV are synchronized such that the system clock will not pass through intermediate frequencies. When CDV is updated, the new frequency will take affect within a maximum period of 32 x t_{OSC}.

In Compatibility mode the divider defaults to divide-by-2 and and in Fast mode it defaults to no division.

Table 6-2. CLKREG – Clock Control Register

CLKREG = 8FH — Reset Value = 0?0? 00?0B

Not Bit Addressable

	TPS3	TPS2	TPS1	TPS0	CDV2	CDV1	CDV0	—
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TPS[3-0]	Timer Prescaler. The Timer Prescaler selects the time base for Timer 0, Timer 1, Timer 2 and the Watchdog Timer. The prescaler is implemented as a 4-bit binary down counter. When the counter reaches zero it is reloaded with the value stored in the TPS bits to give a division ratio between 1 and 16. By default the timers will count every clock cycle in Fast mode (TPS = 0000B) and every six cycles in Compatibility mode (TPS = 0101B).
CDV[2-0]	System Clock Division. Determines the frequency of the system clock relative to the oscillator clock source. CDIV2 CDIV1 CDIV0 System Clock Frequency 0 0 0 $f_{OSC}/1$ 0 0 1 $f_{OSC}/2$ 0 1 0 $f_{OSC}/4$ 0 1 1 $f_{OSC}/8$ 1 0 0 $f_{OSC}/16$ 1 0 1 $f_{OSC}/32$ 1 1 0 Reserved 1 1 1 Reserved

Note: The reset value of CLKREG is 0000000B in Fast mode and 01010010B in Compatibility mode.

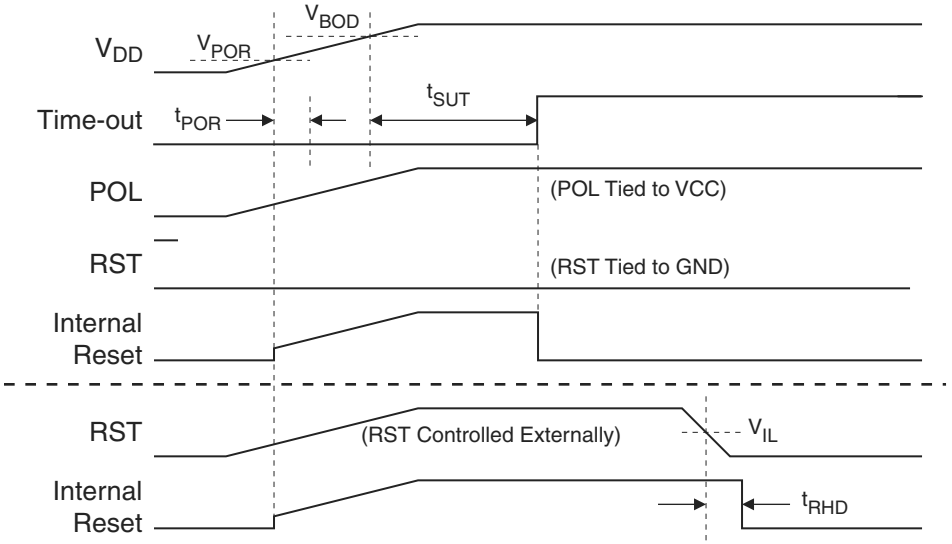
7. Reset

During reset, all I/O Registers are set to their initial values, the port pins are set to their default mode, and the program starts execution from the Reset Vector, 0000H. The AT89LP51/52 has five sources of reset: power-on reset, brown-out reset, external reset, watchdog reset, and software reset.

7.1 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level V_{POR} is nominally 1.4V. The POR is activated whenever V_{DD} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a major supply voltage failure. The POR circuit ensures that the device is reset from power-on. A power-on sequence is shown in Figure 7-1. When V_{DD} reaches the Power-on Reset threshold voltage V_{POR}, an initialization sequence lasting t_{POR} is started. When the initialization sequence completes, the start-up timer determines how long the device is kept in POR after V_{DD} rise. The start-up timer does not begin counting until after V_{DD} reaches the Brown-out Detector (BOD) threshold voltage V_{BOD}. The POR signal is activated again, without any delay, when V_{DD} falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON. The internally generated reset can be extended beyond the power-on period by holding the RST pin active longer than the time-out.

Figure 7-1. Power-on Reset Sequence



Note: t_{POR} is approximately 143 µs ± 5%.

The start-up timer delay is user-configurable with the Start-up Time User Fuses and depends on the clock source (Table 7-1). The Start-Up Time fuses also control the length of the start-up time after a Brown-out Reset or when waking up from Power-down during internally timed mode. The start-up delay should be selected to provide enough settling time for V_{DD} and the selected clock source. The device operating environment (supply voltage, frequency, temperature, etc.) must meet the minimum system requirements before the device exits reset and starts normal operation. The RST pin may be held active externally until these conditions are met.

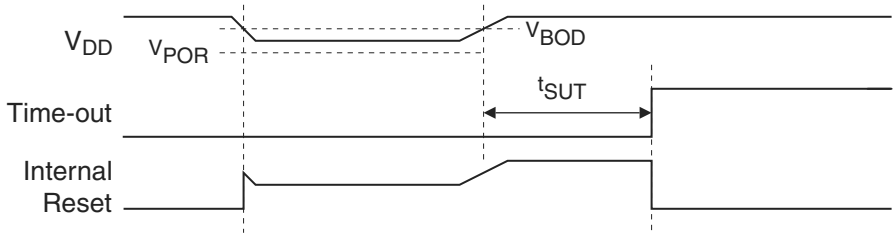
Table 7-1. Start-up Timer Settings

SUT Fuse 1	SUT Fuse 0	Clock Source	t_{SUT} (± 5%) µs
0	0	Internal RC/External Clock	16
		Crystal Oscillator	1024
0	1	Internal RC/External Clock	512
		Crystal Oscillator	2048
1	0	Internal RC/External Clock	1024
		Crystal Oscillator	4096
1	1	Internal RC/External Clock	4096
		Crystal Oscillator	16384

7.2 Brown-out Reset

The AT89LP51/52 has an on-chip Brown-out Detection (BOD) circuit for monitoring the V_{DD} level during operation by comparing it to a fixed trigger level. The trigger level V_{BOD} for the BOD is nominally 2.0V. The purpose of the BOD is to ensure that if V_{DD} fails or dips while executing at speed, the system will gracefully enter reset without the possibility of errors induced by incorrect execution. A BOD sequence is shown in Figure 7-2. When V_{DD} decreases to a value below the trigger level V_{BOD}, the internal reset is immediately activated. When V_{DD} increases above the trigger level plus about 200 mV of hysteresis, the start-up timer releases the internal reset after the specified time-out period has expired (Table 7-1).

Figure 7-2. Brown-out Detector Reset



The AT89LP51/52 allows for a wide V_{DD} operating range. The on-chip BOD may not be sufficient to prevent incorrect execution if V_{BOD} is lower than the minimum required V_{DD} range, such as when a 5.0V supply is coupled with high frequency operation. In such cases an external Brown-out Reset circuit connected to the RST pin may be required.

7.3 External Reset

The RST pin of the AT89LP51/52 can function as either an active-low reset input or as an active-high reset input. The polarity of the RST pin is selectable using the POL pin (formerly $\overline{EA}$). When POL is high the RST pin is active high with an on-chip pull-down resistor tied to GND. When POL is low the RST pin is active low with an on-chip pull-up resistor tied to V_{DD}. The RST pin structure is shown in Figure 7-3. In Compatibility mode the reset pin is sampled every six clock cycles and must be held active for at least twelve clock cycles to trigger the internal reset. In Fast mode the reset pin is sampled every clock cycle and must be held active for at least two clock cycles to trigger the internal reset.

Table 11-2. TCON – Timer/Counter Control Register

TCON = 88H — Reset Value = 0000 0000B

Bit Addressable

	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to interrupt routine.
TR1	Timer 1 run control bit. Set/cleared by software to turn Timer/Counter on/off.
TF0	Timer 0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to interrupt routine.
TR0	Timer 0 run control bit. Set/cleared by software to turn Timer/Counter on/off.
IE1	Interrupt 1 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT1	Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
IE0	Interrupt 0 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT0	Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

Table 11-3. TCONB – Timer/Counter Control Register B

TCONB = 91H — Reset Value = 0000 0000B

Not Bit Addressable

	T1OE	T0OE	SPEN	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0

Symbol	Function
T1OE	Timer 1 Output Enable. Configures Timer 1 to toggle T1 (P3.5) upon overflow.
T0OE	Timer 0 Output Enable. Configures Timer 0 to toggle T0 (P3.4) upon overflow.
SPEN	Enables SPI mode for UART mode 0

11.5 Clock Output (Pin Toggle Mode)

On the AT89LP51/52, Timer 0 and Timer 1 may be independently configured to toggle their respective counter pins, T0 and T1, on overflow by setting the T0OE or T1OE bits in TCONB. The C/$\overline{Tx}$ bits must be set to “0” when in toggle mode and the T0 (P3.4) and T1 (P3.5) pins must be configured in an output mode. The Timer Overflow Flags and Interrupts will continue to function while in toggle mode and Timer 1 may still generate the baud rate for the UART. The timer GATE function also works in toggle mode, allowing the output to be halted by an external input.

Toggle mode can be used with Timer Mode 2 to output a 50% duty cycle clock with 8-bit programmable frequency. T*x* is toggled at every Timer *x* overflow with the pulse width determined by the value of THx. An example waveform is given in Figure 11-5. The following formula gives the output frequency for Timer 0 in Mode 2.

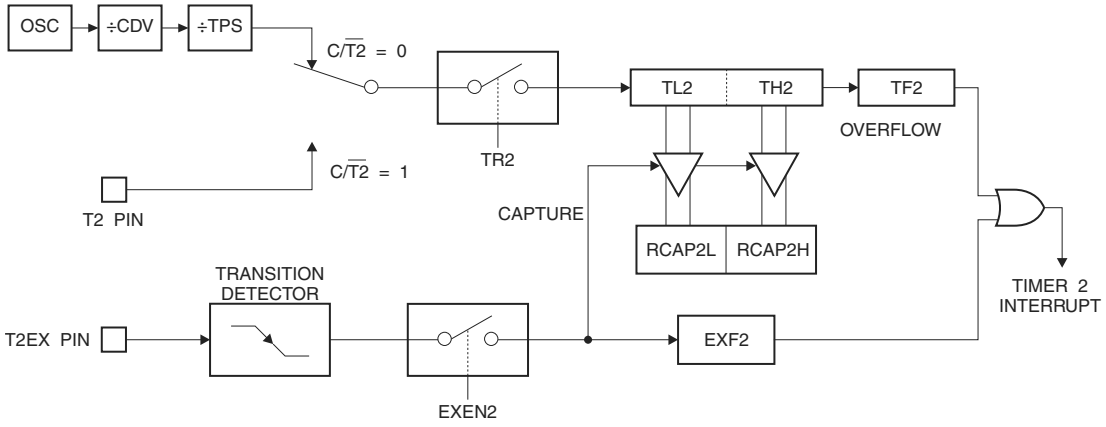
$$\text{Mode 2:} \qquad f_{out} = \frac{\text{System Frequency}}{2 \times (256 - \text{TH0})} \times \frac{1}{\text{TPS} + 1}$$

12.2 Capture Mode

In the Capture mode, Timer 2 is a fixed 16-bit timer or counter that counts up from MIN to MAX. An overflow from MAX to MIN sets bit TF2 in T2CON. If EXEN2 = 1, a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 and TF2 bits can generate an interrupt. Capture mode is illustrated in Figure 12-1. The Timer 2 overflow rate in Capture mode is given by the following equation:

$$\text{Capture Mode:} \qquad \text{Time-out Period} = \frac{65536}{\text{System Frequency}} \times (\text{TPS} + 1)$$

Figure 12-1. Timer 2 Diagram: Capture Mode



12.3 Auto-Reload Mode

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 12-4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin. A summary of the Auto-Reload behaviors is listed in Table 12-5.

Table 12-5. Summary of Auto-Reload Modes

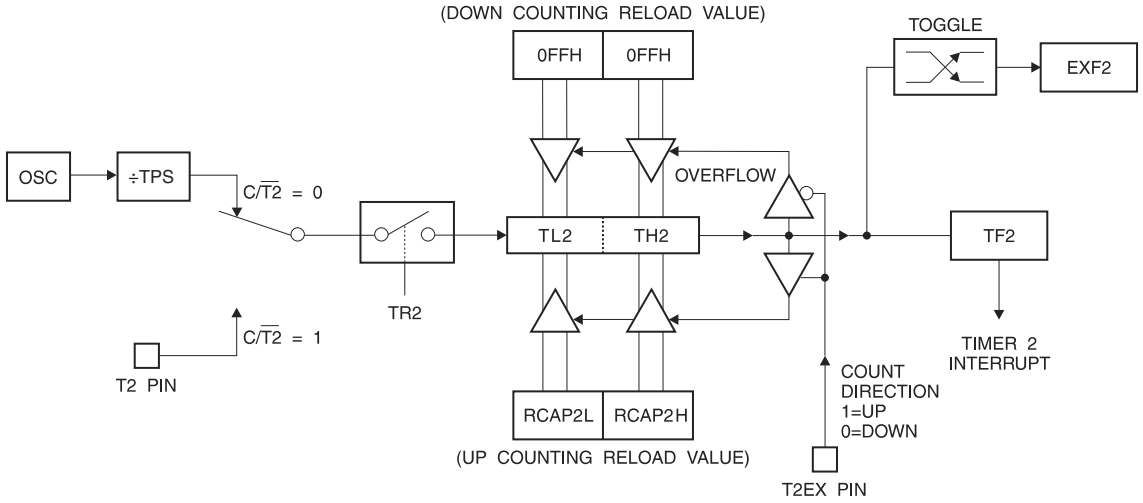
DCEN	T2EX	Direction	Behavior
0	X	Up	BOTTOM →MAX reload to BOTTOM
1	0	Down	MAX →BOTTOM underflow to MAX
1	1	Up	BOTTOM →MAX overflow to BOTTOM

12.3.1 Up Counter

Figure 12-2 shows Timer 2 automatically counting up when DCEN = 0. In this mode Timer 2 counts up to MAX and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with BOTTOM, the 16-bit value in RCAP2H and RCAP2L. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt. The Timer 2 overflow rate for this mode is given in the following equation:

$$\text{Auto-Reload Mode: DCEN = 0} \qquad \text{Time-out Period} = \frac{65536 - \{\text{RCAP2H}, \text{RCAP2L}\}}{\text{System Frequency}} \times (\text{TPS} + 1)$$

Figure 12-5. Timer 2 Diagram: Auto-Reload Mode (DCEN = 1)



The timer overflow/underflow rate for up-down counting mode is the same as for up counting mode, provided that the count direction does not change. Changes to the count direction may result in longer or shorter periods between time-outs.

12.4 Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 12-3). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 12-6.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in UART Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

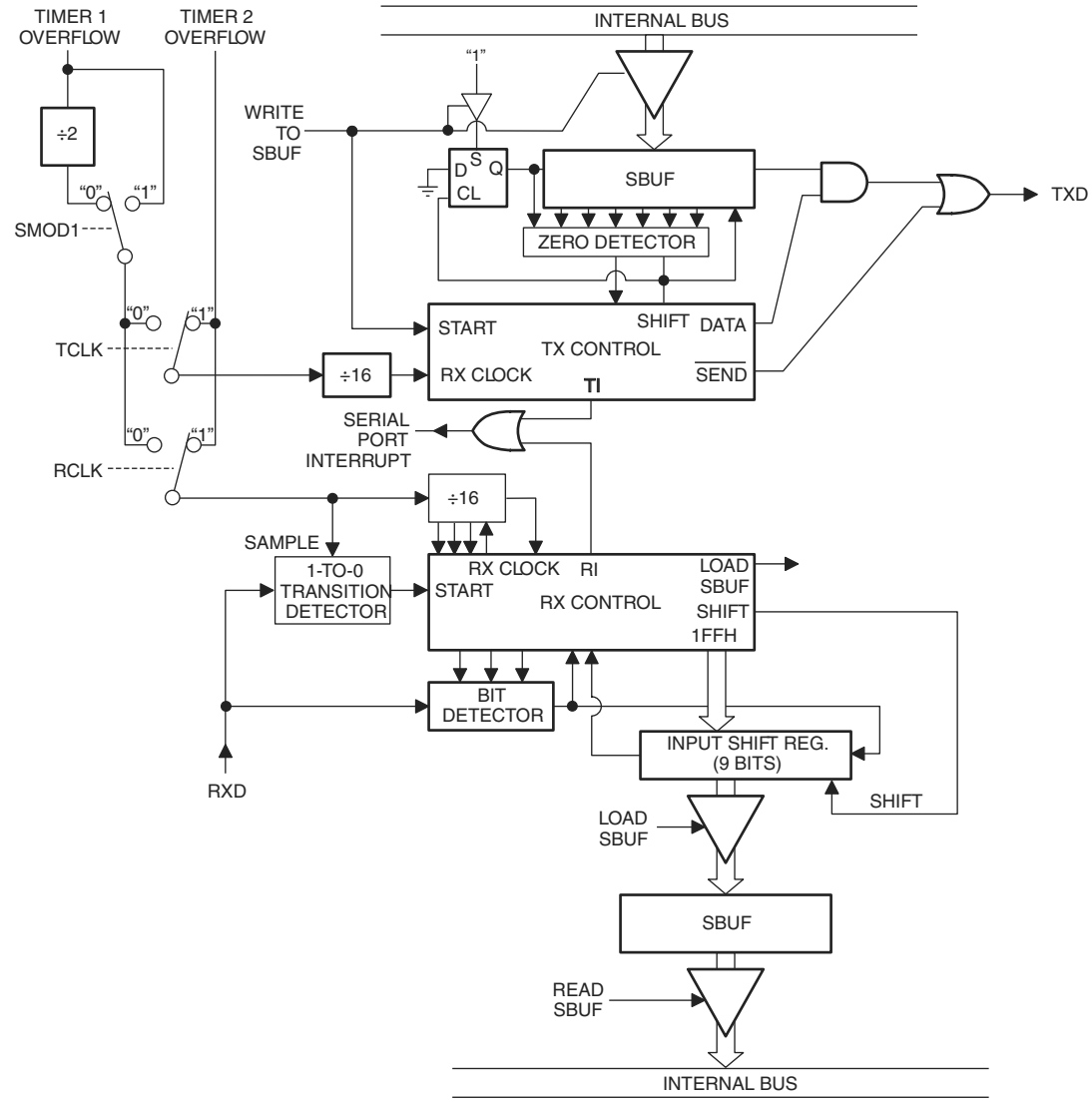
The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The baud rate formulas are given below.

$$\frac{\text{Modes 1, 3}}{\text{Baud Rate}} = \frac{\text{System Frequency}}{16 \times (\text{TPS} + 1) \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 12-6. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt. Also note that the Baud Rate and Frequency Generator modes may be used simultaneously.

Figure 14-6. Serial Port Mode 1



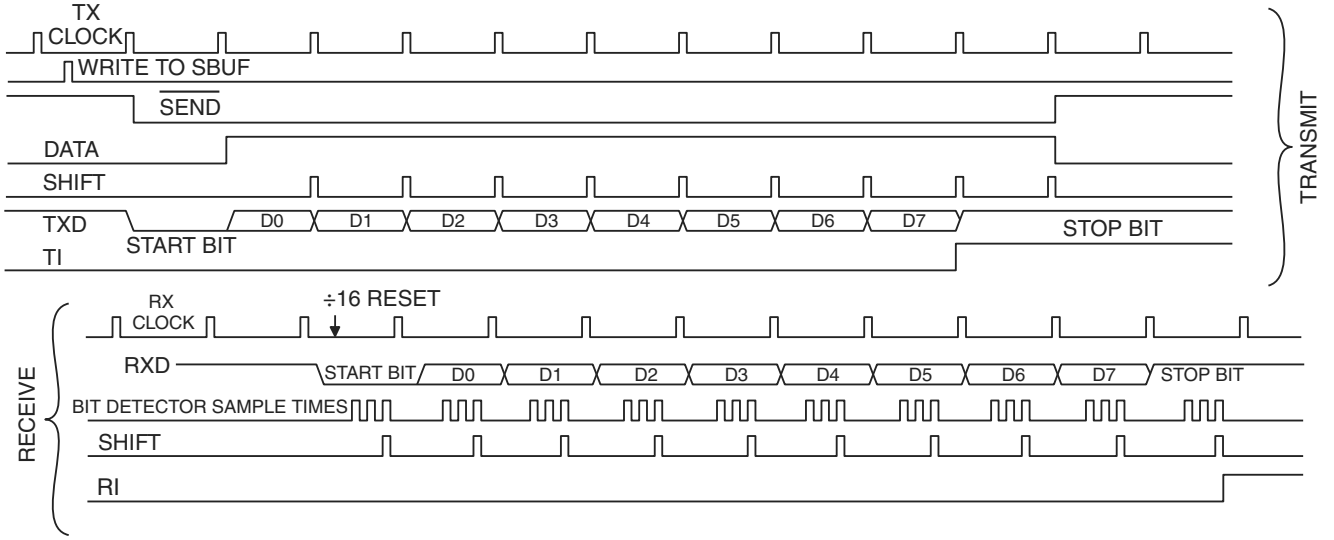
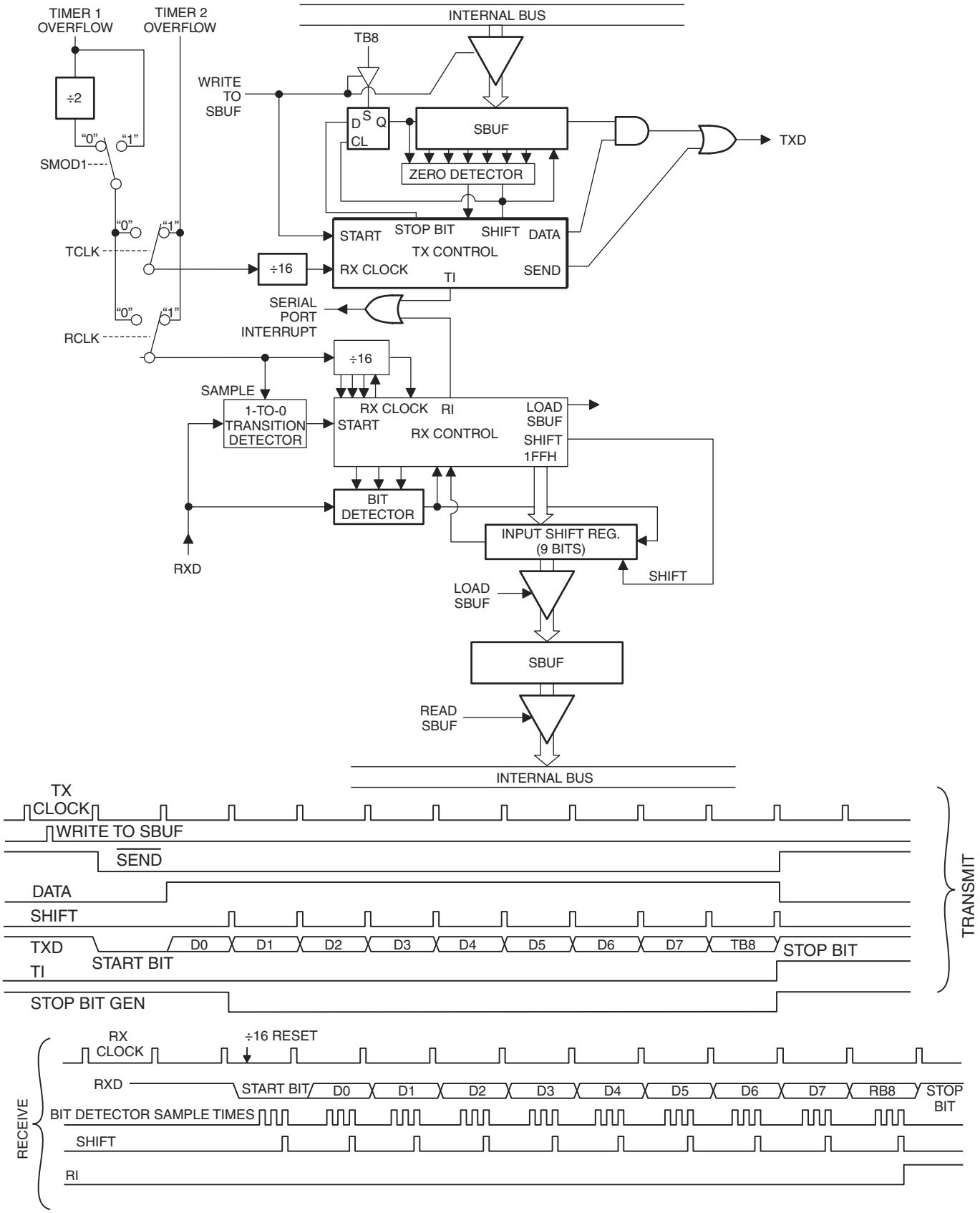


Figure 14-8. Serial Port Mode 3



15. Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) protects the system from incorrect execution by triggering a system reset when it times out after the software has failed to feed the timer prior to the timer overflow. By Default the WDT counts CPU clock cycles. The prescaler bits, PS0, PS1 and PS2 in SFR WDTCON are used to set the period of the Watchdog Timer from 16K to 2048K clock cycles. The Timer Prescaler can also be used to lengthen the time-out period (see Table 6-2 on page 31) The WDT is disabled by Reset and during Power-down mode. When the WDT times out without being serviced, an internal RST pulse is generated to reset the CPU. See Table 15-1 for the available WDT period selections.

Table 15-1. Watchdog Timer Time-out Period Selection

WDT Prescaler Bits			Period(1) (Clock Cycles)
PS2	PS1	PS0	
0	0	0	16K
0	0	1	32K
0	1	0	64K
0	1	1	128K
1	0	0	256K
1	0	1	512K
1	1	0	1024K
1	1	1	2048K

Note: 1. The WDT time-out period is dependent on the system clock frequency.

$$\text{Time-out Period} = \frac{2^{(PS+14)}}{\text{System Frequency}} \times (TPS+1)$$

The Watchdog Timer consists of a 14-bit timer with 7-bit programmable prescaler. Writing the sequence 1EH/E1H to the WDTRST register enables the timer. When the WDT is enabled, the WDTEN bit in WDTCON will be set to “1”. To prevent the WDT from generating a reset when if overflows, the watchdog feed sequence must be written to WDTRST before the end of the time-out period. To feed the watchdog, two write instructions must be sequentially executed successfully. Between the two write instructions, SFR reads are allowed, but writes are not allowed. The instructions should move 1EH to the WDTRST register and then 1EH to the WDTRST register. An incorrect feed or enable sequence will cause an immediate watchdog reset. The program sequence to feed or enable the watchdog timer is as follows:

```
MOV WDTRST, #01Eh
MOV WDTRST, #0E1h
```

15.1 Software Reset

A Software Reset of the AT89LP51/52 is accomplished by writing the software reset sequence 5AH/A5H to the WDTRST SFR. The WDT does not need to be enabled to generate the software reset. A normal software reset will set the SWRST flag in WDTCON. However, if at any time an incorrect sequence is written to WDTRST (i.e. anything other than 1EH/E1H or 5AH/A5H), a software reset will immediately be generated and both the SWRST and WDTOVF flags will be set. In this manner an intentional software reset may be distinguished from a software error-generated reset. The program sequence to generate a software reset is as follows:

16. Instruction Set Summary

The AT89LP51/52 is fully binary compatible with the 8051 instruction set. In Compatibility mode the AT89LP51/52 has identical execution time with AT89S51/52 and other standard 8051s. The difference between the AT89LP51/52 in Fast mode and the standard 8051 is the number of cycles required to execute an instruction. Fast mode instructions may take 1 to 5 clock cycles to complete. The execution times of most instructions may be computed using Table 16-1. Note that for the purposes of this table, a clock cycle is one period of the output of the system clock divider. For Fast mode the divider defaults to 1, so the clock cycle equals the oscillator period. For Compatibility mode the divider defaults to 2, so the clock cycle is twice the oscillator period, or conversely the clock count is half the number of oscillator periods.

Table 16-1. Instruction Execution Times and Exceptions[1]

Generic Instruction Types	Fast Mode Cycle Count Formula
Most arithmetic, logical, bit and transfer instructions	# bytes
Branches and Calls	# bytes + 1
Single Byte Indirect (i.e. ADD A, @Ri, etc.)	2
RET, RETI	4
MOVC	3
MOVX	4[3]
MUL	2
DIV	4
INC DPTR	2

		Clock Cycles		
Arithmetic	**Bytes**	**Compatibility**	**Fast**	**Hex Code**
ADD A, Rn	1	6	1	28-2F
ADD A, direct	2	6	2	25
ADD A, @Ri	1	6	2	26-27
ADD A, #data	2	6	2	24
ADDC A, Rn	1	6	1	38-3F
ADDC A, direct	2	6	2	35
ADDC A, @Ri	1	6	2	36-37
ADDC A, #data	2	6	2	34
SUBB A, Rn	1	6	1	98-9F
SUBB A, direct	2	6	2	95
SUBB A, @Ri	1	6	2	96-97
SUBB A, #data	2	6	2	94
INC Rn	1	6	1	08-0F
INC direct	2	6	2	05
INC @Ri	1	6	2	06-07
INC A	2	6	2	04
DEC Rn	1	6	1	18-1F
DEC direct	2	6	2	15

17. Programming the Flash Memory

The Atmel AT89LP51/52 microcontroller features 8K bytes of on-chip In-System Programmable Flash program memory and 256bytes of nonvolatile Flash data memory. In-System Programming allows programming and reprogramming of the microcontroller positioned inside the end system. Using a simple 3-wire SPI interface, the programmer communicates serially with the AT89LP51/52 microcontroller, reprogramming all nonvolatile memories on the chip. In-System Programming eliminates the need for physical removal of the chips from the system. This will save time and money, both during development in the lab, and when updating the software or parameters in the field. The programming interface of the AT89LP51/52 includes the following features:

- Three-wire serial SPI Programming Interface or 11-pin Parallel Interface
- Selectable Polarity Reset Entry into Programming
- User Signature Array
- Flexible Page Programming
- Row Erase Capability
- Page Write with Auto-Erase Commands
- Programming Status Register

For more detailed information on In-System Programming, refer to the Application Note entitled “AT89LP In-System Programming Specification”.

17.1 Physical Interface

The AT89LP51/52 provides a standard programming command set with two physical interfaces: a bit-serial and a byte-parallel interface. Normal Flash programming utilizes the Serial Peripheral Interface (SPI) pins of an AT89LP51/52 microcontroller. The SPI is a full-duplex synchronous serial interface consisting of three wires: Serial Clock (SCK), Master-In/Slave-out (MISO), and Master-out/Slave-in (MOSI)). When programming an AT89LP51/52 device, the programmer always operates as the SPI master, and the target system always operates as the SPI slave. To enter or remain in Programming mode the device’s reset line (RST) must be held active. With the addition of VDD and GND, an AT89LP51/52 microcontroller can be programmed with a minimum of seven connections as shown in Figure 17-1.

Figure 17-1. In-System Programming Device Connections

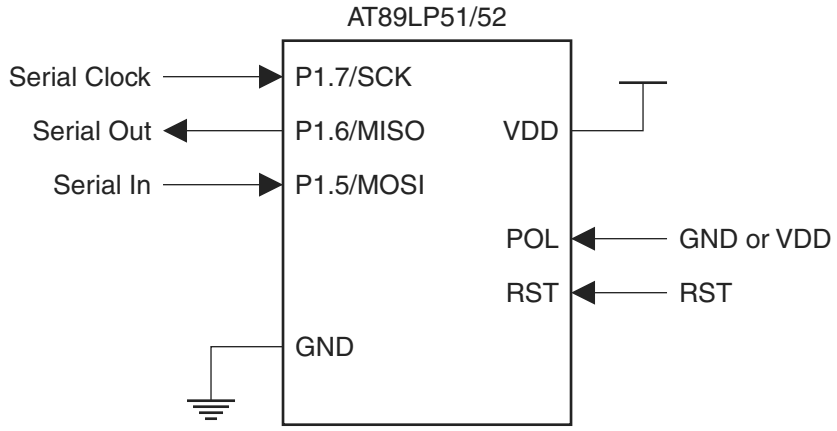
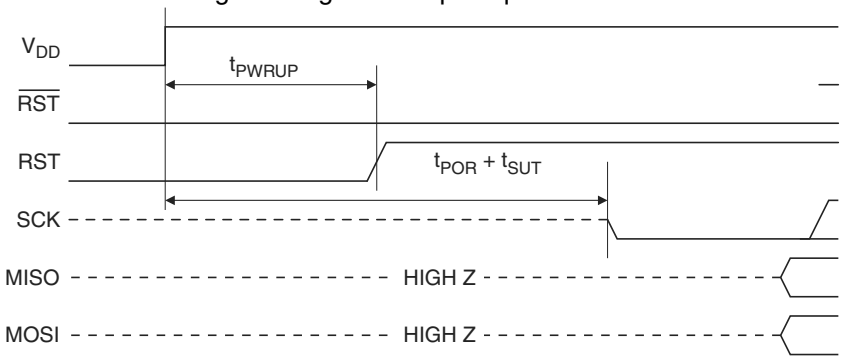


Table 17-2. Programming Command Summary

Command	Opcode	Addr High	Addr Low	Data 0	Data 1–63
Program Enable[1]	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx (0110 1001)[2]	–
Parallel Enable[3]	1010 1100	0011 0101	xxxx xxxx	xxxx xxxx	–
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	–
Read Status	0110 0000	xxxx xxxx	xxxx xxxx	Status Out	–
Write Code Byte	0100 0000	000a aaaa	asbb bbbb	Data In	–
Read Code Byte	0010 0000	000a aaaa	asbb bbbb	Data Out	–
Write Code Page	0101 0000	000a aaaa	as00 0000	Byte 0	Bytes 1–63
Write Code Page with Auto-Erase	0111 0000	000a aaaa	as00 0000	Byte 0	Bytes 1–63
Read Code Page	0011 0000	000a aaaa	as00 0000	Byte 0	Bytes 1–63
Write Data Byte	1100 0000	xxxx xxxx	asbb bbbb	Data In	–
Read Data Byte	1010 0000	xxxx xxxx	asbb bbbb	Data Out	–
Write Data Page	1101 0000	xxxx xxxx	as00 0000	Byte 0	Bytes 1–63
Write Data Page with Auto-Erase	1101 0010	xxxx xxxx	as00 0000	Byte 0	Bytes 1–63
Read Data Page	1011 0000	xxxx xxxx	as00 0000	Byte 0	Bytes 1–63
Write User Fuse[5]	0100 0001	xxxx xxxx	00bb bbbb	Fuse In[4]	–
Read User Fuse[5]	0010 0001	xxxx xxxx	00bb bbbb	Fuse Out[4]	–
Write User Fuses[5]	0101 0001	xxxx xxxx	0000 0000	Fuse 0[4]	Bytes 1–63
Write User Fuses with Auto-Erase[5]	0111 0001	xxxx xxxx	0000 0000	Fuse 0[4]	Fuses 1–63[4]
Read User Fuses[5]	0011 0001	xxxx xxxx	0000 0000	Fuse 0[4]	Fuses 1–63[4]
Write Lock Mode[6]	1010 1100	1110 00BB	xxxx xxxx	xxxx xxxx	–
Read Lock Mode[6]	0010 0100	xxxx xxxx	xxxx xxxx	xxxL LLxx	–
Write Lock Bit[6]	0100 0100	xxxx xxxx	00bb bbbb	Data In[4]	–
Write Lock Bits[6]	0101 0100	xxxx xxxx	0000 0000	Byte 0[4]	Bytes 1–63[4]
Read Lock Bits[6]	0011 0100	xxxx xxxx	0000 0000	Byte 0[4]	Bytes 1–63[4]
Write User Signature Byte	0100 0010	xxxx xxxx	asbb bbbb	Data In	–
Read User Signature Byte	0010 0010	xxxx xxxx	asbb bbbb	Data Out	–
Write User Signature Page	0101 0010	xxxx xxxx	as00 0000	Byte 0	Byte 1–63
Write User Signature Page with Auto-Erase	0111 0010	xxxx xxxx	as00 0000	Byte 0	Byte 1–63
Read User Signature Page	0011 0010	xxxx xxxx	as00 0000	Byte 0	Byte 1–63
Read Atmel Signature Byte[7]	0010 1000	xxxx xxxx	0sbb bbbb	Data Out	–
Read Atmel Signature Page[7]	0011 1000	xxxx xxxx	0s00 0000	Byte 0	Byte 1–63

Notes:
1. Program Enable must be the **first** command issued after entering into programming mode.
2. 0110 1001B is returned on MISO when Program Enable was successful.
3. Parallel Enable switches the interface from serial to parallel format until RST goes inactive.
4. Each byte address selects one fuse or lock bit. Data bytes must be 00h or FFh.
5. See Table 17-5 on page 86 for Fuse definitions.
6. See Table 17-4 on page 86 for Lock Bit definitions.

Figure 17-9. Serial Programming Power-up Sequence

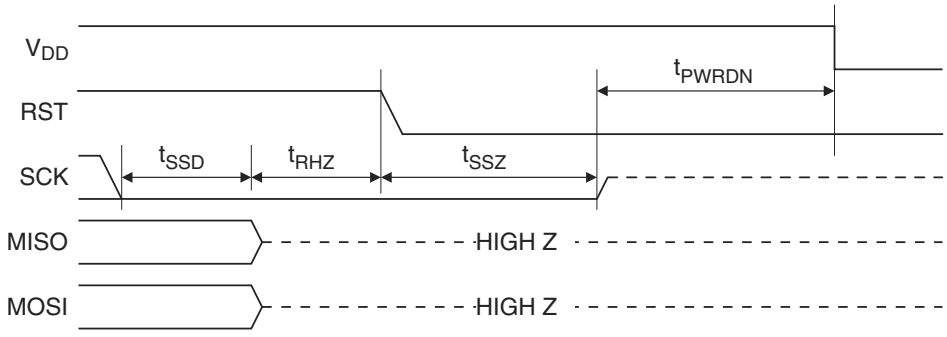


17.9.2 Power-down Sequence

Execute this sequence to power-down the device **after** programming.

1. Drive SCK low.
2. Wait at least t_{SSD} and Tristate MOSI.
3. Wait at least t_{RHZ} and drive RST low.
4. Wait at least t_{SSZ} and tristate SCK.
5. Wait no more than t_{PWRDN} and power off VDD.

Figure 17-10. Serial Programming Power-down Sequence

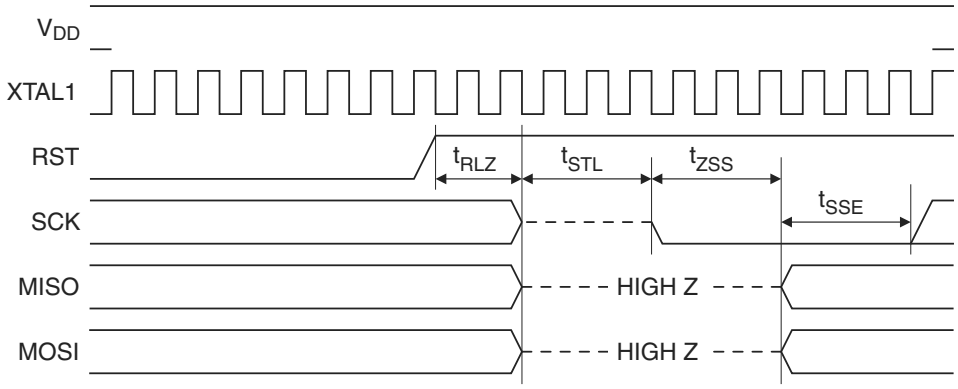


17.9.3 ISP Start Sequence

Execute this sequence to exit CPU execution mode and enter ISP mode when the device has passed Power-On Reset and is already operational.

1. Drive RST high.
2. Wait $t_{RLZ} + t_{STL}$.
3. Drive SCK low.
4. Start programming session.

Figure 17-11. In-System Programming (ISP) Start Sequence

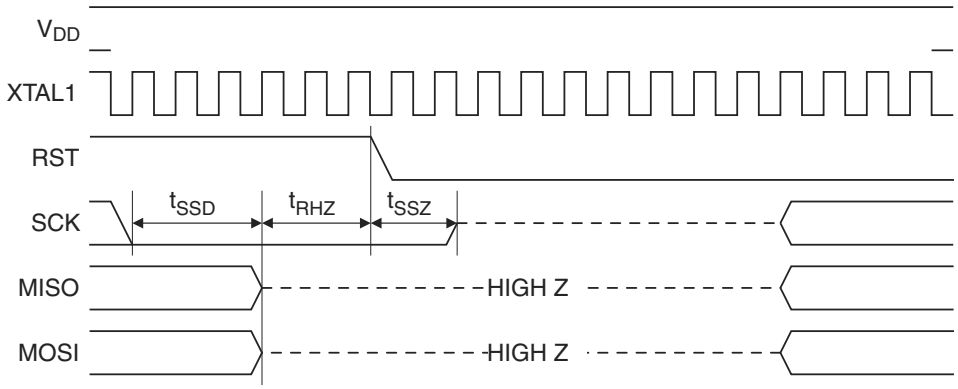


17.9.4 ISP Exit Sequence

Execute this sequence to exit ISP mode and resume CPU execution mode.

1. Drive SCK low.
1. Wait at least t_{SSD}.
2. Tristate MOSI.
3. Wait at least t_{RHZ} and bring RST low.
4. Wait t_{SSZ} and tristate SCK.

Figure 17-12. In-System Programming (ISP) Exit Sequence



Note: The waveforms on this page are not to scale.

17.9.5 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is a byte-oriented full-duplex synchronous serial communication channel. During In-System Programming, the programmer always acts as the SPI master and the target device always acts as the SPI slave. The target device receives serial data on MOSI and outputs serial data on MISO. The Programming Interface implements a standard SPI Port with a fixed data order and For In-System Programming, bytes are transferred MSB first as shown in Figure 17-13. The SCK phase and polarity follow SPI clock mode 0 (CPOL = 0, CPHA = 0) where bits are sampled on the rising edge of SCK and output on the falling edge of SCK. For more detailed timing information see Figure 17-14.

Table 18-1. External Clock Parameters

Symbol	Parameter	V_{DD} = 2.4V to 5.5V		V_{DD} = 4.5V to 5.5V		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency(1)	0	20	0	25	MHz
t_{CLCL}	Clock Period	50		40		ns
t_{CHCX}	External Clock High Time	15		12		ns
t_{CLCX}	External Clock Low Time	15		12		ns
t_{CLCH}	External Clock Rise Time		5		5	ns
t_{CHCL}	External Clock Fall Time		5		5	ns

Note: 1. No wait state (single-cycle) fetch speed for Fast Mode

Table 18-2. Clock Characteristics

Symbol	Parameter	Condition	Min	Max	Units
f_{XTAL}	Crystal Oscillator Frequency	Low Power Oscillator	0	12	MHz
		High Power Oscillator	0	24	MHz
f_{RC}	Internal Oscillator Frequency	T_A = 25°C; V_{DD} = 5.0V	1.824	1.862	MHz
		V_{DD} = 2.4 to 5.5V	1.751	1.935	MHz

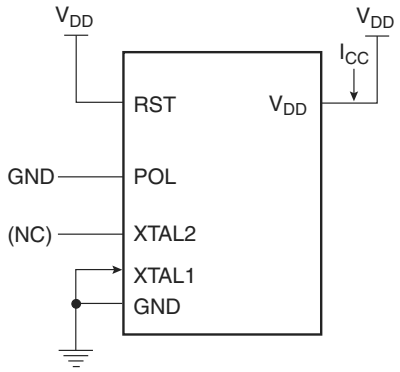
18.5 Reset Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{DD} = 2.4 to 5.5V, unless otherwise noted.

Table 18-3. Reset Characteristics

Symbol	Parameter	Condition	Min	Max	Units
R_{RST}	Reset Pull-up Resistor		150	300	kΩ
	Reset Pull-down Resistor		100	200	kΩ
V_{POR}	Power-On Reset Threshold		1.3	1.6	V
V_{BOD}	Brown-Out Detector Threshold		1.9	2.2	V
V_{BH}	Brown-Out Detector Hysteresis		200	300	mV
t_{POR}	Power-On Reset Delay		135	150	µs
t_{WDTRST}	Watchdog Reset Pulse Width		$49t_{CLCL}$		ns

18.8.6 I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{DD} = 2V to 5.5V



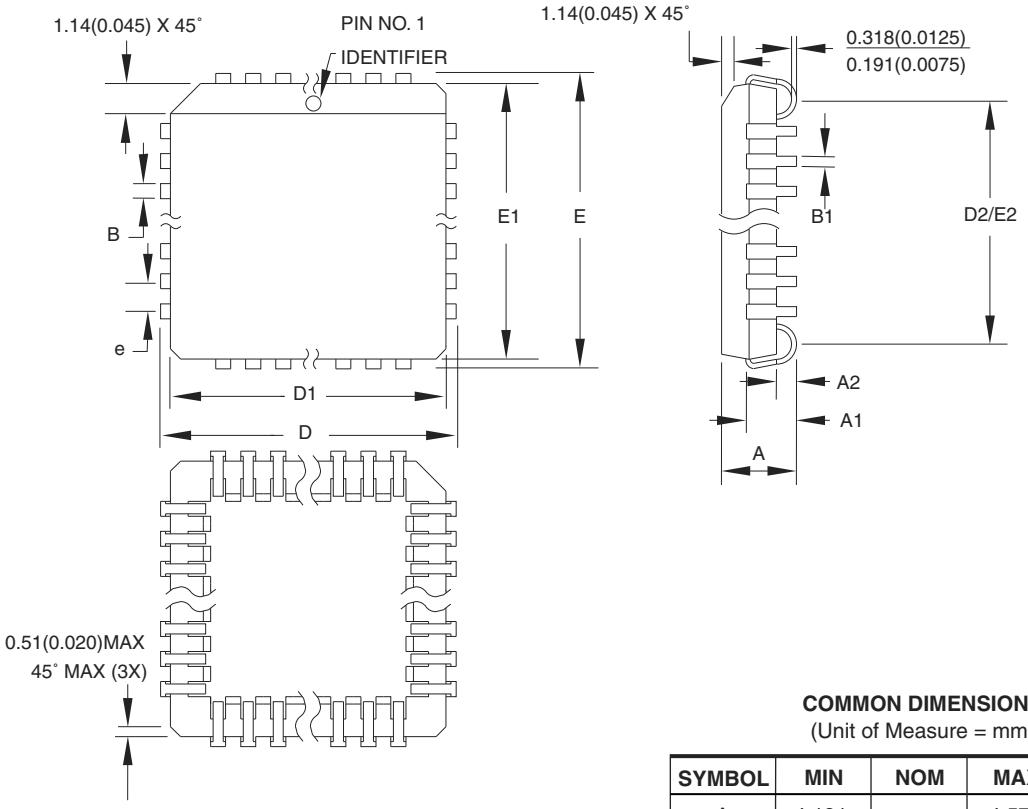
19. Ordering Information

19.1 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Code Memory	Ordering Code	Package	Operation Range
20	2.4V to 5.5V	4KB	AT89LP51-20AU AT89LP51-20PU AT89LP51-20JU AT89LP51-20MU	44A 40P6 44J 44M1	Industrial (-40° C to 85° C)
20	2.4V to 5.5V	8KB	AT89LP52-20AU AT89LP52-20PU AT89LP52-20JU AT89LP52-20MU	44A 40P6 44J 44M1	Industrial (-40° C to 85° C)

Package Types	
44A	44-lead, Thin Plastic Quad Flat Package (TQFP)
40P6	40-lead, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
44M1	44-pad, 7 x 7 x 1.0 mm Body, Plastic Very Thin Quad Flat No Lead Package (VQFN/MLF)

20.3 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

Table of Contents (Continued)