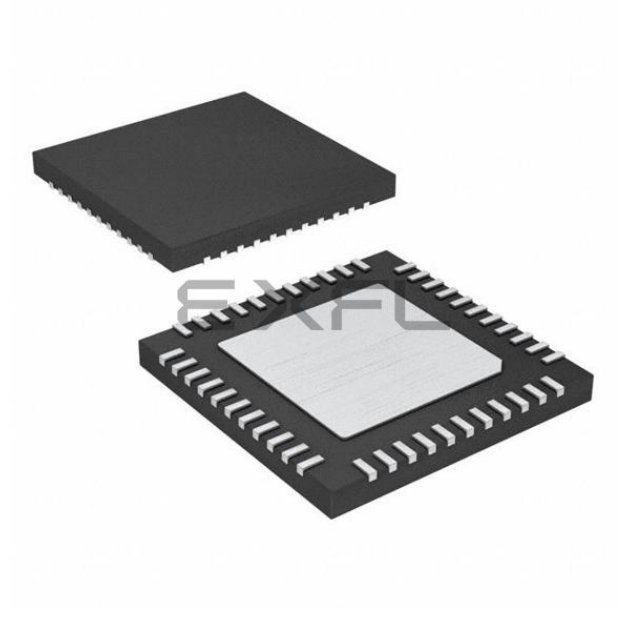

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp51-20mu

4. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 4-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

Table 4-1. AT89LP51/52 SFR Map and Reset Values

	8	9	A	B	C	D	E	F	
0F8H									0FFH
0F0H	B 0000 0000								0F7H
0E8H									0EFH
0E0H	ACC 0000 0000								0E7H
0D8H									0DFH
0D0H	PSW 0000 0000								0D7H
0C8H	T2CON 0000 0000	T2MOD 0000 0000	RCAP2L 0000 000	RCAP2H 0000 0000	TL2 0000 000	TH2 0000 0000			0CFH
0C0H	P4 1111 1111	PMOD (2)							0C7H
0B8H	IP xx00 0000	SADEN 0000 0000							0BFH
0B0H	P3 1111 1111							IPH xx00 0000	0B7H
0A8H	IE 0x00 0000	SADDR 0000 0000							0AFH
0A0H	P2 1111 1111		AUXR1 0000 00x0				WDTRST (write-only)	WDTCON 0000 0xx0	0A7H
98H	SCON 0000 0000	SBUF xxxx xxxx							9FH
90H	P1 1111 1111	TCONB 000x xxxx					MEMCON 0000 00xx		97H
88H	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 0000 0000	CLKREG (3)	8FH
80H	P0 1111 1111	SP 0000 0111	DP0L 0000 0000	DP0H 0000 0000	DP1L 0000 0000	DP1H 0000 0000		PCON 000x 0000	87H
	0	1	2	3	4	5	6	7	

Notes: 1. All SFRs in the left-most column are bit-addressable.

2. Reset value is 0101 0101B when Tristate-Port Fuse is enabled and 0000 0011B when disabled.

3. Reset value is 0101 0010B when Compatibility mode is enabled and 0000 0000B when disabled.

6. System Clock

The system clock is generated directly from one of three selectable clock sources. The three sources are the on-chip crystal oscillator, external clock source, and internal RC oscillator. A diagram of the clock subsystem is shown in Figure 6-1. The on-chip crystal oscillator may also be configured for low or high power operation. The clock source is selected by the Clock Source User Fuses as shown in Table 6-1. See “User Configuration Fuses” on page 86. By default, in Fast mode no internal clock division is used to generate the CPU clock from the system clock. In Compatibility mode the default is to divide the oscillator output by two. The system clock divider may be used to prescale the system clock with other values. The choice of clock source also affects the start-up time after a POR, BOD or Power-down event (See “Reset” on page 32 or “Power-down Mode” on page 35)

Figure 6-1. Clock Subsystem Diagram

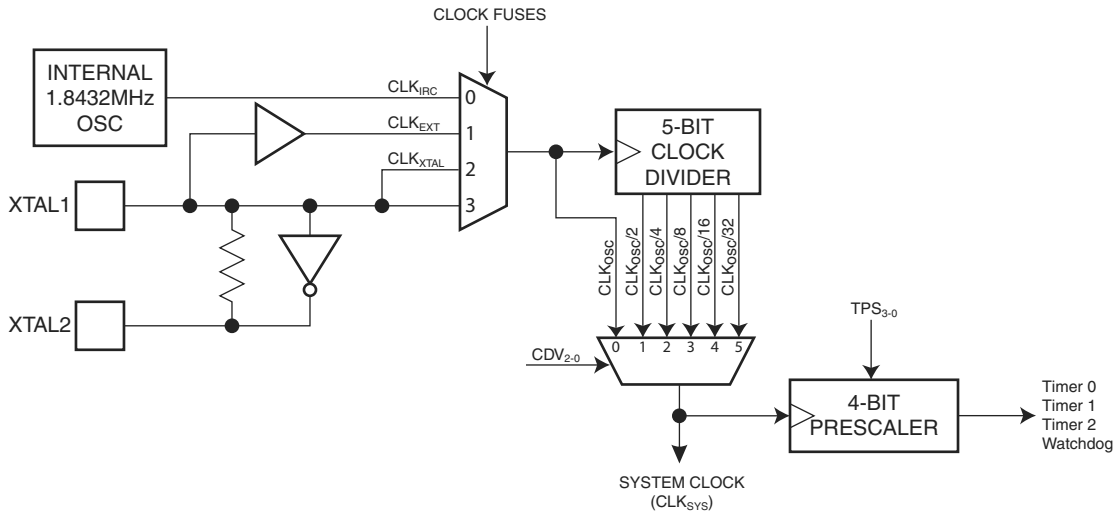


Table 6-1. Clock Source Settings

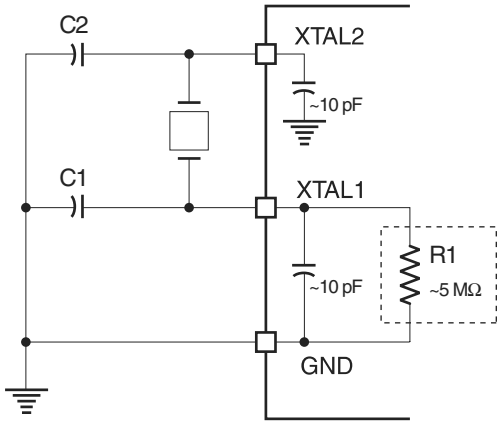
Clock Source Fuse 1	Clock Source Fuse 0	Selected Clock Source
1	1	High Power Crystal Oscillator (f > 12 MHz)
1	0	Low Power Crystal Oscillator (f ≤12 MHz)
0	1	External Clock on XTAL1
0	0	Internal 1.8432 MHz Auxiliary Oscillator

6.1 Crystal Oscillator

When enabled, the internal inverting oscillator amplifier is connected between XTAL1 and XTAL2 for connection to an external quartz crystal or ceramic resonator. The oscillator may operate in either high-power or low-power mode. Low-speed mode is intended for crystals of 12 MHz or less and consumes less power than the higher speed mode. The configuration as shown in Figure 6-2 applies for both high and low power oscillators. Note that in some cases, external capacitors C1 and C2 may **NOT** be required due to the on-chip capacitance of the XTAL1 and XTAL2 inputs (approximately 10 pF each). When using the crystal oscillator, P4.6 and P4.7 will have their inputs and outputs disabled. Also, XTAL2 in crystal oscillator mode should not be used to directly drive a board-level clock without a buffer.

An optional 5 MΩ on-chip resistor can be connected between XTAL1 and GND. This resistor can improve the startup characteristics of the oscillator especially at higher frequencies. The resistor can be enabled/disabled with the R1 User Fuse (See “User Configuration Fuses” on page 86.)

Figure 6-2. Crystal Oscillator Connections

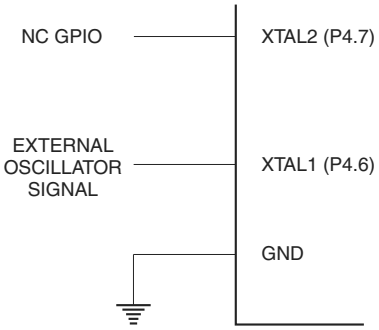


Note: 1. C1, C2 = 5 pF ±5pF for Crystals
= 5 pF ±5pF for Ceramic Resonators

6.2 External Clock Source

The external clock option disables the oscillator amplifier and allows XTAL1 to be driven directly by an external clock source as shown in Figure 6-3. XTAL2 may be left unconnected, used as general purpose I/O P4.7, or configured to output a divided version of the system clock.

Figure 6-3. External Clock Drive Configuration



6.3 Internal RC Oscillator

The AT89LP51/52 has an Internal Auxiliary oscillator tuned to 1.8432 MHz ±2.0%. When enabled as the clock source, XTAL1 and XTAL2 may be used as P4.6 and P4.7 respectively.

6.4 System Clock Divider

The CDV_{2-0} bits in CLKREG allow the system clock to be divided down from the selected clock source by powers of 2. The clock divider provides users with a greater frequency range when using the Internal Oscillator. For example, to achieve a 230.4 kHz system frequency when using the RC oscillator, CDV_{2-0} should be set to 011B for divide-by-8 operation. The divider can also be used to reduce power consumption by decreasing the operational frequency during non-critical periods. The resulting system frequency is given by the following equation:

$$f_{SYS} = \frac{f_{OSC}}{2^{CDV}}$$

where f_{OSC} is the frequency of the selected clock source. The clock divider will prescale the clock for the CPU and all peripherals. The value of CDV may be changed at any time without interrupting normal execution. Changes to CDV are synchronized such that the system clock will not pass through intermediate frequencies. When CDV is updated, the new frequency will take affect within a maximum period of 32 x t_{OSC}.

In Compatibility mode the divider defaults to divide-by-2 and and in Fast mode it defaults to no division.

Table 6-2. CLKREG – Clock Control Register

CLKREG = 8FH — Reset Value = 0?0? 00?0B

Not Bit Addressable

	TPS3	TPS2	TPS1	TPS0	CDV2	CDV1	CDV0	—
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TPS[3-0]	Timer Prescaler. The Timer Prescaler selects the time base for Timer 0, Timer 1, Timer 2 and the Watchdog Timer. The prescaler is implemented as a 4-bit binary down counter. When the counter reaches zero it is reloaded with the value stored in the TPS bits to give a division ratio between 1 and 16. By default the timers will count every clock cycle in Fast mode (TPS = 0000B) and every six cycles in Compatibility mode (TPS = 0101B).
CDV[2-0]	System Clock Division. Determines the frequency of the system clock relative to the oscillator clock source. CDIV2 CDIV1 CDIV0 System Clock Frequency 0 0 0 $f_{OSC}/1$ 0 0 1 $f_{OSC}/2$ 0 1 0 $f_{OSC}/4$ 0 1 1 $f_{OSC}/8$ 1 0 0 $f_{OSC}/16$ 1 0 1 $f_{OSC}/32$ 1 1 0 Reserved 1 1 1 Reserved

Note: The reset value of CLKREG is 0000000B in Fast mode and 01010010B in Compatibility mode.

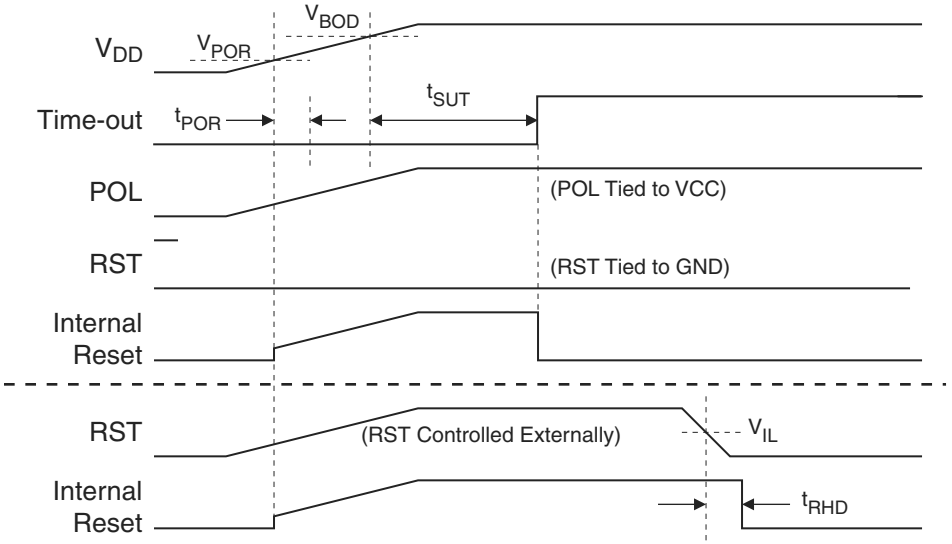
7. Reset

During reset, all I/O Registers are set to their initial values, the port pins are set to their default mode, and the program starts execution from the Reset Vector, 0000H. The AT89LP51/52 has five sources of reset: power-on reset, brown-out reset, external reset, watchdog reset, and software reset.

7.1 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level V_{POR} is nominally 1.4V. The POR is activated whenever V_{DD} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a major supply voltage failure. The POR circuit ensures that the device is reset from power-on. A power-on sequence is shown in Figure 7-1. When V_{DD} reaches the Power-on Reset threshold voltage V_{POR}, an initialization sequence lasting t_{POR} is started. When the initialization sequence completes, the start-up timer determines how long the device is kept in POR after V_{DD} rise. The start-up timer does not begin counting until after V_{DD} reaches the Brown-out Detector (BOD) threshold voltage V_{BOD}. The POR signal is activated again, without any delay, when V_{DD} falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON. The internally generated reset can be extended beyond the power-on period by holding the RST pin active longer than the time-out.

Figure 7-1. Power-on Reset Sequence



Note: t_{POR} is approximately 143 µs ± 5%.

The start-up timer delay is user-configurable with the Start-up Time User Fuses and depends on the clock source (Table 7-1). The Start-Up Time fuses also control the length of the start-up time after a Brown-out Reset or when waking up from Power-down during internally timed mode. The start-up delay should be selected to provide enough settling time for V_{DD} and the selected clock source. The device operating environment (supply voltage, frequency, temperature, etc.) must meet the minimum system requirements before the device exits reset and starts normal operation. The RST pin may be held active externally until these conditions are met.

CPU when an interrupt is generated. The timer and UART peripherals continue to function during Idle. If these functions are not needed during idle, they should be explicitly disabled by clearing the appropriate control bits in their respective SFRs. The watchdog may be selectively enabled or disabled during Idle by setting/clearing the WDIDLE bit. The Brown-out Detector is always active during Idle. Any enabled interrupt source or reset may terminate Idle mode. When exiting Idle mode with an interrupt, the interrupt will immediately be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into Idle.

The power consumption during Idle mode can be further reduced by prescaling down the system clock using the System Clock Divider (Section 6.4 on page 31). Be aware that the clock divider will affect all peripheral functions and baud rates may need to be adjusted to maintain their rate with the new clock frequency.

Table 8-1. PCON – Power Control Register

PCON = 87H — Reset Value = 000X 0000B

Not Bit Addressable

	SMOD1	SMOD0	PWDEX	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud Rate bit. Doubles the baud rate of the UART in Modes 1, 2, or 3.
SMOD0	Frame Error Select. When SMOD0 = 1, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0.
PWDEX	Power-down Exit Mode. When PWDEX = 0, wake up from Power-down is externally controlled. When PWDEX = 1, wake up from Power-down is internally timed.
POF	Power Off Flag. POF is set to “1” during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets).
GF1, GF0	General-purpose Flags
PD	Power-down bit. Setting this bit activates power-down operation. The PD bit is cleared automatically by hardware when waking up from power-down.
IDL	Idle Mode bit. Setting this bit activates Idle mode operation. The IDL bit is cleared automatically by hardware when waking up from idle

8.2 Power-down Mode

Setting the Power-down (PD) bit in PCON enters Power-down mode. Power-down mode stops the oscillator, disables the BOD and powers down the Flash memory in order to minimize power consumption. Only the power-on circuitry will continue to draw power during Power-down. During Power-down, the power supply voltage may be reduced to the RAM keep-alive voltage. The RAM contents will be retained, but the SFR contents are not guaranteed once V_{DD} has been reduced. Power-down may be exited by external reset, power-on reset, or certain enabled interrupts.

Table 11-2. TCON – Timer/Counter Control Register

TCON = 88H — Reset Value = 0000 0000B

Bit Addressable

	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to interrupt routine.
TR1	Timer 1 run control bit. Set/cleared by software to turn Timer/Counter on/off.
TF0	Timer 0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to interrupt routine.
TR0	Timer 0 run control bit. Set/cleared by software to turn Timer/Counter on/off.
IE1	Interrupt 1 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT1	Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
IE0	Interrupt 0 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT0	Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

Table 11-3. TCONB – Timer/Counter Control Register B

TCONB = 91H — Reset Value = 0000 0000B

Not Bit Addressable

	T1OE	T0OE	SPEN	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0

Symbol	Function
T1OE	Timer 1 Output Enable. Configures Timer 1 to toggle T1 (P3.5) upon overflow.
T0OE	Timer 0 Output Enable. Configures Timer 0 to toggle T0 (P3.4) upon overflow.
SPEN	Enables SPI mode for UART mode 0

11.5 Clock Output (Pin Toggle Mode)

On the AT89LP51/52, Timer 0 and Timer 1 may be independently configured to toggle their respective counter pins, T0 and T1, on overflow by setting the T0OE or T1OE bits in TCONB. The C/$\overline{Tx}$ bits must be set to “0” when in toggle mode and the T0 (P3.4) and T1 (P3.5) pins must be configured in an output mode. The Timer Overflow Flags and Interrupts will continue to function while in toggle mode and Timer 1 may still generate the baud rate for the UART. The timer GATE function also works in toggle mode, allowing the output to be halted by an external input.

Toggle mode can be used with Timer Mode 2 to output a 50% duty cycle clock with 8-bit programmable frequency. T*x* is toggled at every Timer *x* overflow with the pulse width determined by the value of THx. An example waveform is given in Figure 11-5. The following formula gives the output frequency for Timer 0 in Mode 2.

$$\text{Mode 2:} \qquad f_{out} = \frac{\text{System Frequency}}{2 \times (256 - \text{TH0})} \times \frac{1}{\text{TPS} + 1}$$

Figure 11-5. Timer 0/1 Toggle Mode 2 Waveform

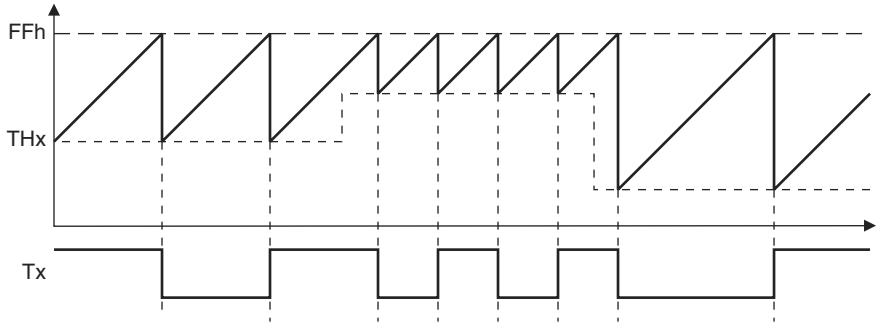


Table 11-4. TMOD – Timer/Counter Mode Control Register

TMOD Address = 089H — Reset Value = 0000 0000B

Not Bit Addressable

	GATE1	C/$\overline{T1}$	T1M1	T1M0	GATE0	C/$\overline{T0}$	T0M0	T0M1
Bit	7	6	5	4	3	2	1	0

Symbol	Function
GATE1	Timer 1 Gating Control. When set, Timer/Counter 1 is enabled only while $\overline{INT1}$ pin is high and TR1 control pin is set. When cleared, Timer 1 is enabled whenever TR1 control bit is set.
C/$\overline{T1}$	Timer or Counter Selector 1. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from T1 input pin). C/$\overline{T1}$ must be zero when using Timer 1 in Clock Out mode.
T1M1 T1M0	Timer 1 Operating Mode **Mode** / **T1M1** / **T1M0** / **Operation** 0 / 0 / 0 / 13-bit Timer Mode. 8-bit Timer/Counter TH1 with TL1 as 5-bit prescaler. 1 / 0 / 1 / 16-bit Timer Mode. TH1 and TL1 are cascaded to form a 16-bit Timer/Counter. 2 / 1 / 0 / 8-bit Auto Reload Mode. TH1 holds a value which is reloaded into 8-bit Timer/Counter TL1 each time it overflows. 3 / 1 / 1 / Timer/Counter 1 is stopped
GATE0	Timer 0 Gating Control. When set, Timer/Counter 0 is enabled only while $\overline{INT0}$ pin is high and TR0 control pin is set. When cleared, Timer 0 is enabled whenever TR0 control bit is set.
C/$\overline{T0}$	Timer or Counter Selector 0. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from T0 input pin). C/$\overline{T0}$ must be zero when using Timer 0 in Clock Out mode.
T0M1 T0M0	Timer 0 Operating Mode **Mode** / **T0M1** / **T0M0** / **Operation** 0 / 0 / 0 / 13-bit Timer Mode. 8-bit Timer/Counter TH0 with TL0 as 5-bit prescaler. 1 / 0 / 1 / 16-bit Timer Mode. TH0 and TL0 are cascaded to form a 16-bit Timer/Counter. 2 / 1 / 0 / 8-bit Auto Reload Mode. TH0 holds a value which is reloaded into 8-bit Timer/Counter TL0 each time it overflows. 3 / 1 / 1 / Split Timer Mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.

12.1 Timer 2 Registers

Control and status bits for Timer 2 are contained in registers T2CON (see Table 12-3) and T2MOD (see Table 12-4). The register pair {TH2, TL2} at addresses 0CDH and 0CCH are the 16-bit timer register for Timer 2. The register pair {RCAP2H, RCAP2L} at addresses 0CBH and 0CAH are the 16-bit Capture/Reload register for Timer 2 in capture and auto-reload modes.

Table 12-3. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1) or dual-slope mode.
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 12-4. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = 0000 0000B

Not Bit Addressable

	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
T2OE	Timer 2 Output Enable. When T2OE = 1 and C/$\overline{T2}$ = 0, the T2 pin will toggle after every Timer 2 overflow.
DCEN	Timer 2 Down Count Enable. When Timer 2 operates in Auto-Reload mode and EXEN2 = 1, setting DCEN = 1 will cause Timer 2 to count up or down depending on the state of T2EX.

Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9-bit mode requires that the 9th information bit be a “1” to indicate that the received information is an address and not data.

In Mode 1 (8-bit) the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8th address bits and the information is either a Given or Broadcast address. Automatic Address Recognition is not available during Mode 0.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples show the versatility of this scheme:

Slave 0
SADDR = 1100 0000
SADEN = 1111 1101
Given = 1100 00X0

Slave 1
SADDR = 1100 0000
SADEN = 1111 1110
Given = 1100 000X

In the previous example, SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a “0” in bit 0 and it ignores bit 1. Slave 1 requires a “0” in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a “0” in bit 1. A unique address for slave 1 would be 1100 0001 since a “1” in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system, the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0
SADDR = 1100 0000
SADEN = 1111 1001
Given = 1100 0XX0

Slave 1
SADDR = 1110 0000
SADEN = 1111 1010
Given = 1110 0X0X

Slave 2
SADDR = 1110 0000
SADEN = 1111 1100
Given = 1110 00XX

In the above example, the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2, use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logic OR of SADDR and SADEN. Zeros in this result are trended as don't cares. In most cases, interpreting the don't cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with "0"s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

14.5 More About Mode 0

In Mode 0, the UART is configured as either a two wire half-duplex or three wire full-duplex synchronous serial interface. In two-wire mode serial data enters and exits through RXD and TXD outputs the shift clock. In three-wire mode serial data enters through MISO, exits through MOSI and SCK outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. Figure 14-3 and Figure 14-5 on page 67 show simplified functional diagrams of the serial port in Mode 0 and associated timing. The baud rate is programmable to 1/2 or 1/4 the system frequency by setting/clearing the SMOD1 bit in Fast mode, or 1/3 or 1/6 the system frequency in Compatibility mode. However, changing SMOD1 has an effect on the relationship between the clock and data as described below. The baud rate can also be generated by Timer 1 by setting TB8. Table 14-4 lists the baud rate options for Mode 0.

Table 14-4. Mode 0 Baud Rates

TB8	SMOD1	Baud Rate (Fast)	Baud Rate (Compatibility)
0	0	$f_{SYS}/4$	$f_{SYS}/6$
0	1	$f_{SYS}/2$	$f_{SYS}/3$
1	0	(Timer 1 Overflow) / 4	(Timer 1 Overflow) / 4
1	1	(Timer 1 Overflow) / 2	(Timer 1 Overflow) / 2

14.5.1 Two-Wire (Half-Duplex) Mode

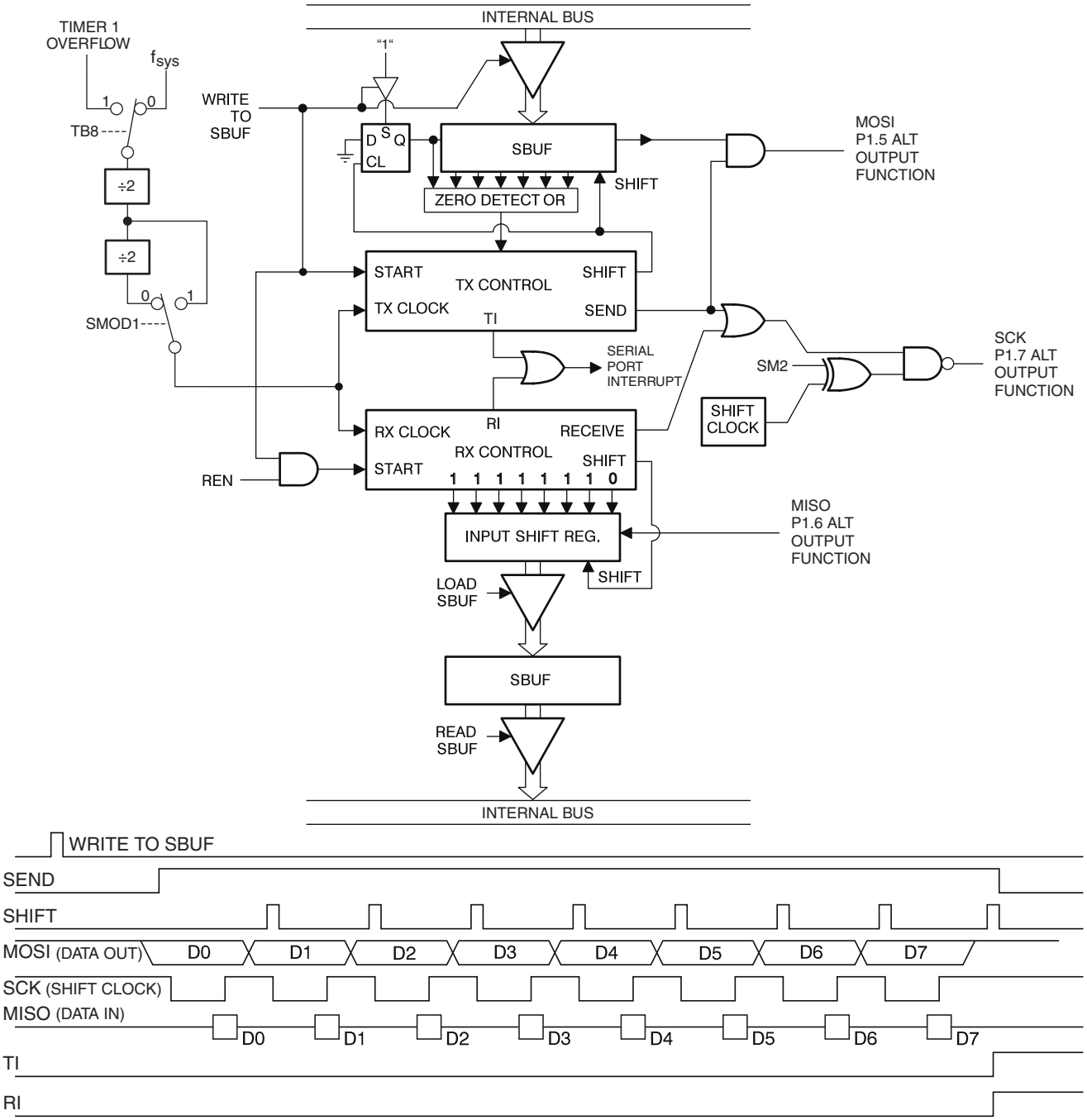
Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a "1" into the 9th position of the transmit shift register and tells the TX Control Block to begin a transmission. The internal timing is such that one full bit slot may elapse between "write to SBUF" and activation of SEND.

SEND transfers the output of the shift register to the alternate output function line of P3.0, and also transfers Shift Clock to the alternate output function line of P3.1. As data bits shift out to the right, "0"s come in from the left. When the MSB of the data byte is at the output position of the shift register, the "1" that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain "0"s. This condition flags the TX Control block to do one last shift, then deactivate SEND and set TI.

Reception is initiated by the condition REN = 1 and RI = 0. At the next clock cycle, the RX Control unit writes the bits 11111110B to the receive shift register and activates RECEIVE in the next clock phase. RECEIVE enables Shift Clock to the alternate output function line of P3.1. As data bits come in from the right, "1"s shift out to the left. When the "0" that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set.

The relationship between the shift clock and data is determined by the combination of the SM2 and SMOD1 bits as listed in Table 14-5 and shown in Figure . The SM2 bit determines the idle

Figure 14-5. Serial Port Mode 0 (Three-Wire)



15. Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) protects the system from incorrect execution by triggering a system reset when it times out after the software has failed to feed the timer prior to the timer overflow. By Default the WDT counts CPU clock cycles. The prescaler bits, PS0, PS1 and PS2 in SFR WDTCON are used to set the period of the Watchdog Timer from 16K to 2048K clock cycles. The Timer Prescaler can also be used to lengthen the time-out period (see Table 6-2 on page 31) The WDT is disabled by Reset and during Power-down mode. When the WDT times out without being serviced, an internal RST pulse is generated to reset the CPU. See Table 15-1 for the available WDT period selections.

Table 15-1. Watchdog Timer Time-out Period Selection

WDT Prescaler Bits			Period(1) (Clock Cycles)
PS2	PS1	PS0	
0	0	0	16K
0	0	1	32K
0	1	0	64K
0	1	1	128K
1	0	0	256K
1	0	1	512K
1	1	0	1024K
1	1	1	2048K

Note: 1. The WDT time-out period is dependent on the system clock frequency.

$$\text{Time-out Period} = \frac{2^{(PS+14)}}{\text{System Frequency}} \times (TPS+1)$$

The Watchdog Timer consists of a 14-bit timer with 7-bit programmable prescaler. Writing the sequence 1EH/E1H to the WDTRST register enables the timer. When the WDT is enabled, the WDTEN bit in WDTCON will be set to “1”. To prevent the WDT from generating a reset when if overflows, the watchdog feed sequence must be written to WDTRST before the end of the time-out period. To feed the watchdog, two write instructions must be sequentially executed successfully. Between the two write instructions, SFR reads are allowed, but writes are not allowed. The instructions should move 1EH to the WDTRST register and then 1EH to the WDTRST register. An incorrect feed or enable sequence will cause an immediate watchdog reset. The program sequence to feed or enable the watchdog timer is as follows:

```
MOV WDTRST, #01Eh
MOV WDTRST, #0E1h
```

15.1 Software Reset

A Software Reset of the AT89LP51/52 is accomplished by writing the software reset sequence 5AH/A5H to the WDTRST SFR. The WDT does not need to be enabled to generate the software reset. A normal software reset will set the SWRST flag in WDTCON. However, if at any time an incorrect sequence is written to WDTRST (i.e. anything other than 1EH/E1H or 5AH/A5H), a software reset will immediately be generated and both the SWRST and WDTOVF flags will be set. In this manner an intentional software reset may be distinguished from a software error-generated reset. The program sequence to generate a software reset is as follows:

17.2 Memory Organization

The AT89LP51/52 offers 8K bytes of In-System Programmable (ISP) nonvolatile Flash code memory and 256 bytes of nonvolatile Flash data memory. In addition, the device contains a 256-byte User Signature Array and a 128-byte read-only Atmel Signature Array. The memory organization is shown in Table 17-1 and Figure 17-3. The memory is divided into pages of 128 bytes each. A single read or write command may only access half a page (64 bytes) in the memory; however, write with auto-erase commands will erase an entire 128-byte page even though they can only write one half page. Each memory type resides in its own address space and is accessed by commands specific to that memory. However, all memory types share the same page size.

User configuration fuses are mapped as a row in the memory, with each byte representing one fuse. From a programming standpoint, fuses are treated the same as normal code bytes except they are not affected by Chip Erase. Fuses can be enabled at any time by writing 00h to the appropriate locations in the fuse row. However, to disable a fuse, i.e. set it to FFh, the **entire** fuse row must be erased and then reprogrammed. The programmer should read the state of all the fuses into a temporary location, modify those fuses which need to be disabled, then issue a Fuse Write with Auto-Erase command using the temporary data. Lock bits are treated in a similar manner to fuses except they may only be erased (unlocked) by Chip Erase.

Table 17-1. AT89LP51/52 Memory Organization

Memory	Capacity	Page Size	# Pages	Address Range
CODE	4096 bytes 8192 bytes	128 bytes	32 64	0000H – 0FFFH 0000H – 1FFFH
DATA	256 bytes	128 bytes	2	0000H – 00FFH
User Signature	256 bytes	128 bytes	2	0000H – 00FFH
Atmel Signature	128 bytes	128 bytes	1	0000H – 007FH

Figure 17-3. AT89LP52 Memory Organization

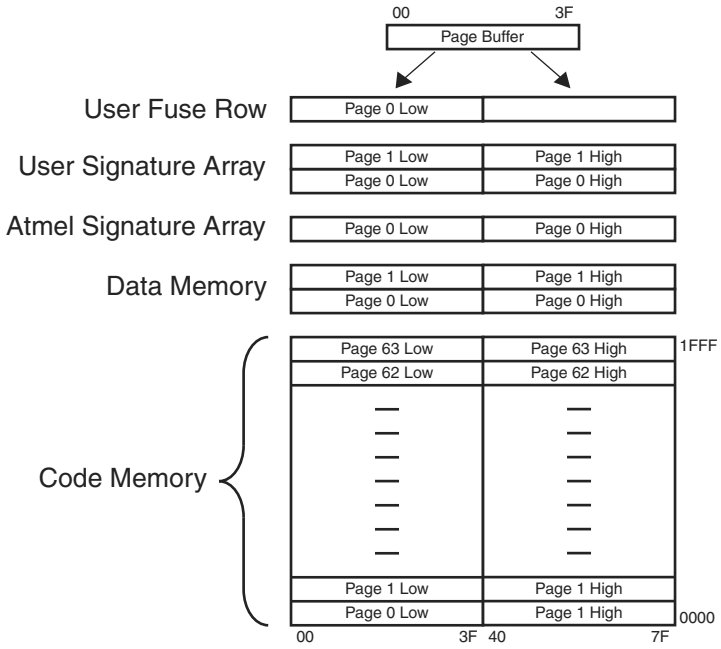


Table 17-5. User Configuration Fuse Definitions

Address	Fuse Name	Description
07H	Tristate Ports	FFh: I/O Ports start in input-only mode (tristated) after reset 00h: I/O Ports start in quasi-bidirectional mode after reset
08H	In-Application Programming	FFh: In-Application Programming Disabled 00h: In-Application Programming Enabled
09H	R1 Enable	FFh: 5 MΩ resistor on XTAL1 Disabled 00h: 5 MΩ resistor on XTAL1 Enabled

Notes: 1. The default state for Tristate Ports is 00h. All other fuses default to FFh.
2. Changes to these fuses will only take effect after a device POR.
3. Changes to these fuses will only take effect after the ISP session terminates by bringing RST inactive.

17.8 User Signature

The User Signature Array contains 256 bytes of non-volatile memory in two 128-byte pages. The User Signature is available for serial numbers, firmware revision information, date codes or other user parameters. The User Signature Array may only be written by an external device when the User Signature Programming Fuse is enabled. When the fuse is enabled, Chip Erase will also erase the first page of the array. When the fuse is disabled, the array is not affected by write or erase commands. Programming of the Signature Array can also be disabled by the Lock Bits. However, reading the signature is always allowed and the array should not be used to store security sensitive information. The User Signature Array may be modified during execution through the In-Application Programming interface, regardless of the state of the User Signature Programming fuse or Lock Bits, provided that the IAP Fuse is enabled. Note that the address of the User Signature Array, as seen by the IAP interface, equals the User Signature address plus 256 (0100H–01FFH instead of 0000H–00FFH).

17.9 Programming Interface Timing

This section details general system timing sequences and constraints for entering or exiting In-System Programming as well as parameters related to the Serial Peripheral Interface during ISP. The general timing parameters for the following waveform figures are listed in section “Timing Parameters” on page 91.

17.9.1 Power-up Sequence

Execute this sequence to enter programming mode immediately after power-up. In the RST pin is disabled or if the ISP Fuse is disabled, this is the only method to enter programming (see “External Reset” on page 33).

1. Apply power between VDD and GND pins. RST should remain low.
2. Wait at least t_{PWRUP} and drive RST high if active-high otherwise keep low.
3. Wait at least t_{SUT} for the internal Power-on Reset to complete. The value of t_{SUT} will depend on the current settings of the device.
4. Start programming session.

18.3.5 Push-Pull Output

Figure 18-9. Push-Pull Output I-V Source Characteristic at 5V

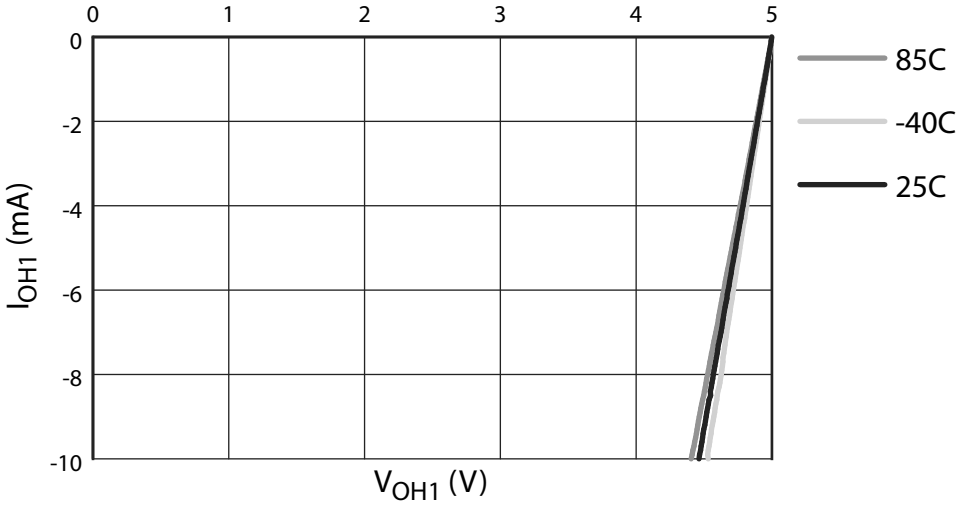


Figure 18-10. Push-Pull Output I-V Source Characteristic at 3V

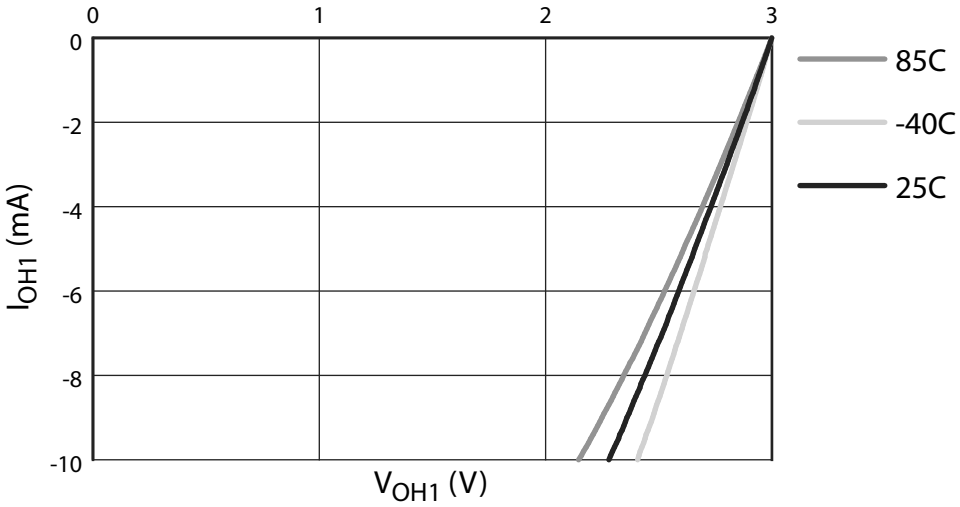


Figure 18-11. Push-Pull Output I-V Sink Characteristic at 5V

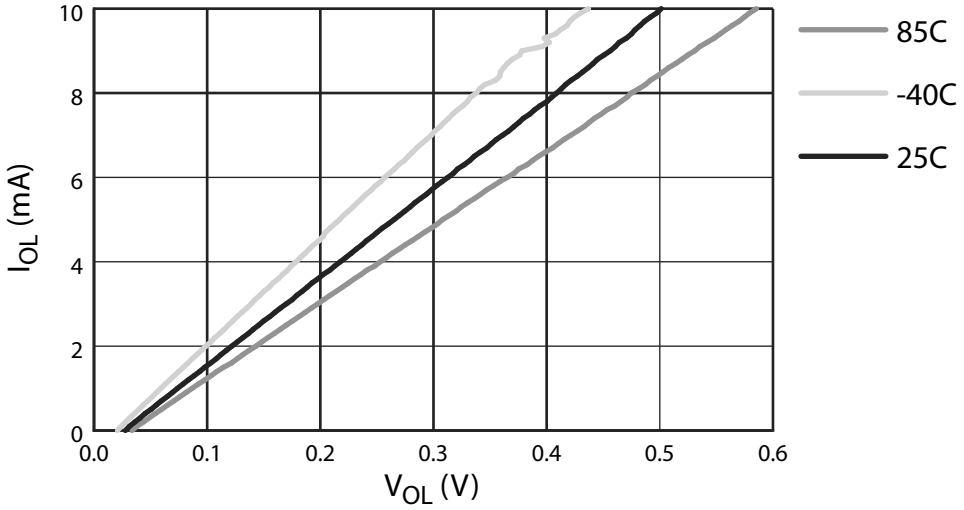
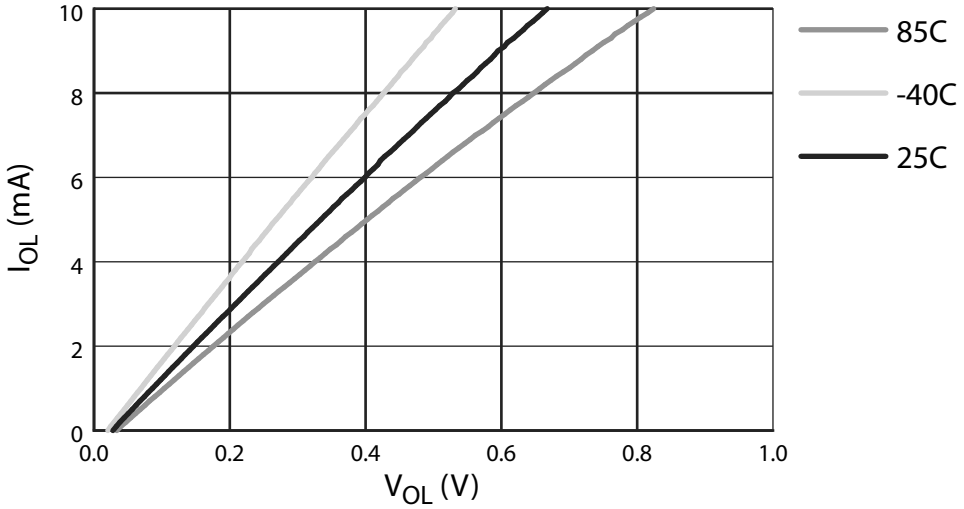


Figure 18-12. Push-Pull Output I-V Sink Characteristic at 3V



Note: The I_{OL}/V_{OL} characteristic applies to Push-Pull, Quasi-Bidirectional and Open-Drain modes.

18.4 Clock Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{DD} = 2.4 to 5.5V, unless otherwise noted.

Figure 18-13. External Clock Drive Waveform

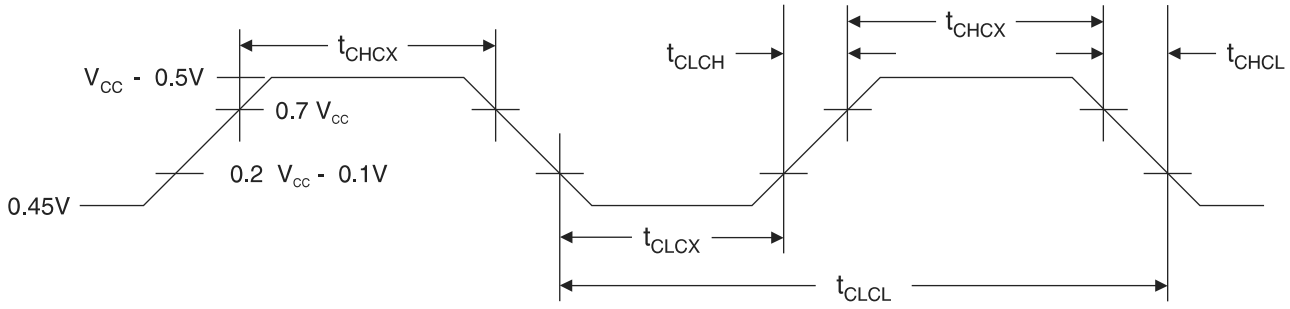


Table 18-1. External Clock Parameters

Symbol	Parameter	V_{DD} = 2.4V to 5.5V		V_{DD} = 4.5V to 5.5V		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency(1)	0	20	0	25	MHz
t_{CLCL}	Clock Period	50		40		ns
t_{CHCX}	External Clock High Time	15		12		ns
t_{CLCX}	External Clock Low Time	15		12		ns
t_{CLCH}	External Clock Rise Time		5		5	ns
t_{CHCL}	External Clock Fall Time		5		5	ns

Note: 1. No wait state (single-cycle) fetch speed for Fast Mode

Table 18-2. Clock Characteristics

Symbol	Parameter	Condition	Min	Max	Units
f_{XTAL}	Crystal Oscillator Frequency	Low Power Oscillator	0	12	MHz
		High Power Oscillator	0	24	MHz
f_{RC}	Internal Oscillator Frequency	T_A = 25°C; V_{DD} = 5.0V	1.824	1.862	MHz
		V_{DD} = 2.4 to 5.5V	1.751	1.935	MHz

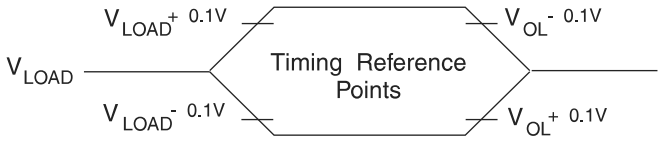
18.5 Reset Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{DD} = 2.4 to 5.5V, unless otherwise noted.

Table 18-3. Reset Characteristics

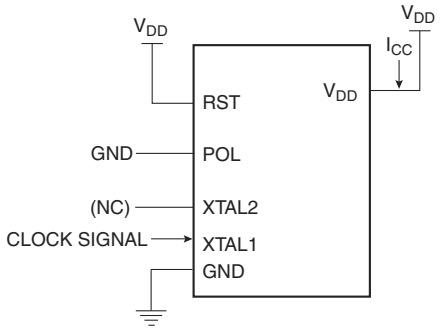
Symbol	Parameter	Condition	Min	Max	Units
R_{RST}	Reset Pull-up Resistor		150	300	kΩ
	Reset Pull-down Resistor		100	200	kΩ
V_{POR}	Power-On Reset Threshold		1.3	1.6	V
V_{BOD}	Brown-Out Detector Threshold		1.9	2.2	V
V_{BH}	Brown-Out Detector Hysteresis		200	300	mV
t_{POR}	Power-On Reset Delay		135	150	µs
t_{WDTRST}	Watchdog Reset Pulse Width		$49t_{CLCL}$		ns

18.8.2 Float Waveform(1)



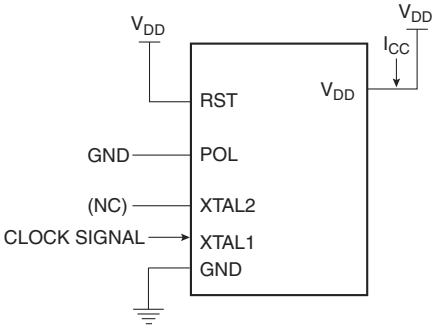
Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

18.8.3 I_{CC} Test Condition, Active Mode, All Other Pins are Disconnected(1)

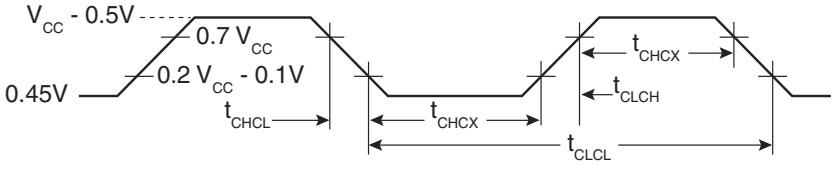


Notes: 1. For active supply current measurements all ports are configured in quasi-bidirectional mode. Timers 0, 1 and 2 are configured to be free running in their default timer modes. The CPU executes a simple random number generator that accesses RAM and SFR bus, and exercises the ALU and hardware multiplier.

18.8.4 I_{CC} Test Condition, Idle Mode, All Other Pins are Disconnected



18.8.5 Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns



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