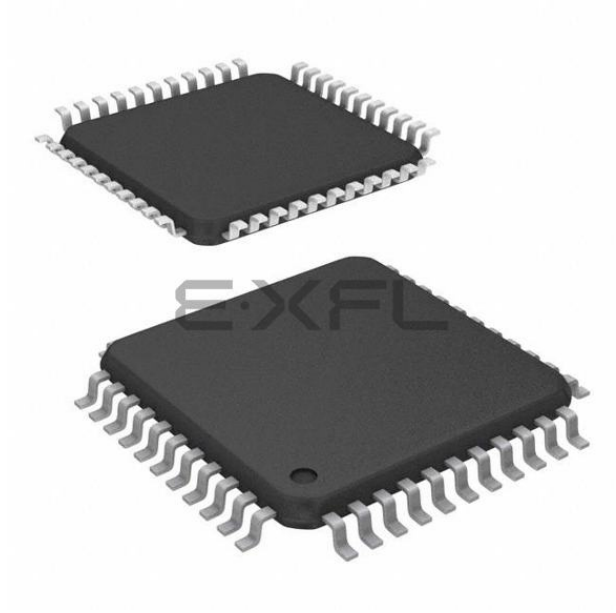

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp52-20au

Table 1-1. AT89LP51/52 Pin Description

Pin Number				Symbol	Type	Description
TQFP	PLCC	PDIP	VQFN			
21	27	24	21	P2.3	I/O O	**P2.3**: I/O Port 2 bit 3. **A11**: External memory interface Address bit 11.
22	28	25	22	P2.4	I/O O	**P2.4**: I/O Port 2 bit 5. **A12**: External memory interface Address bit 12.
23	29	26	23	P2.5	I/O O	**P2.5**: I/O Port 2 bit 5. **A13**: External memory interface Address bit 13.
24	30	27	24	P2.6	I/O O	**P2.6**: I/O Port 2 bit 6. **A14**: External memory interface Address bit 14.
25	31	28	25	P2.7	I/O O	**P2.7**: I/O Port 2 bit 7. **A15**: External memory interface Address bit 15.
26	32	29	26	P4.5	I/O O	**P4.5**: I/O Port 4 bit 5. **$\overline{\text{PSEN}}$**: External memory interface Program Store Enable (active-low).
27	33	30	27	P4.4	I/O O	**P4.4**: I/O Port 4 bit 4. **ALE**: External memory interface Address Latch Enable.
28	34		28		NC	Not internally connected
29	35	31	29	POL	I	**POL**: Reset polarity (See “External Reset” on page 33.)
30	36	32	30	P0.7	I/O I/O	**P0.7**: I/O Port 0 bit 7. **AD7**: External memory interface Address/Data bit 7.
31	37	33	31	P0.6	I/O I/O	**P0.6**: I/O Port 0 bit 6. **AD6**: External memory interface Address/Data bit 6.
32	38	34	32	P0.5	I/O I/O	**P0.5**: I/O Port 0 bit 5. **AD5**: External memory interface Address/Data bit 5.
33	39	35	33	P0.4	I/O I/O	**P0.4**: I/O Port 0 bit 4. **AD4**: External memory interface Address/Data bit 4.
34	40	36	34	P0.3	I/O I/O	**P0.3**: I/O Port 0 bit 3. **AD3**: External memory interface Address/Data bit 3.
35	41	37	35	P0.2	I/O I/O	**P0.2**: I/O Port 0 bit 2. **AD2**: External memory interface Address/Data bit 2.
36	42	38	36	P0.1	I/O I/O	**P0.1**: I/O Port 0 bit 1. **AD1**: External memory interface Address/Data bit 1.
37	43	39	37	P0.0	I/O I/O	**P0.0**: I/O Port 0 bit 0. **AD0**: External memory interface Address/Data bit 0.
38	44	40	38	VDD	I	Supply Voltage
39	1		39		NC	Not internally connected
40	2	1	40	P1.0	I/O I/O	**P1.0**: I/O Port 1 bit 0. **T2**: Timer 2 External Input or Clock Output.
41	3	2	41	P1.1	I/O I	**P1.1**: I/O Port 1 bit 1. **T2EX**: Timer 2 External Capture/Reload Input.
42	4	3	42	P1.2	I/O	**P1.2**: I/O Port 1 bit 2.
43	5	4	43	P1.3	I/O	**P1.3**: I/O Port 1 bit 3.
44	6	5	44	P1.4	I/O	**P1.4**: I/O Port 1 bit 4.

2.3.1 Instruction Execution

In Compatibility mode the AT89LP51/52 CPU uses the six-state machine cycle of the standard 8051 where instruction bytes are fetched every three system clock cycles. Execution times in this mode are identical to AT89S51/52. For greater performance the user can enable Fast mode by disabling the Compatibility fuse. In Fast mode the CPU fetches one code byte from memory every clock cycle instead of every three clock cycles. This greatly increases the throughput of the CPU. Each standard instruction executes in only 1 to 4 clock cycles. See “Instruction Set Summary” on page 75 for more details. Any software delay loops or instruction-based timing operations may need to be retuned to achieve the desired results in Fast mode.

2.3.2 System Clock

By default in Compatibility mode the system clock frequency is divided by 2 from the externally supplied XTAL1 frequency for compatibility with standard 8051s (12 clocks per machine cycle). The System Clock Divider can scale the system clock versus the oscillator source (See Section 6.4 on page 31). The divide-by-2 can be disabled to operate in X2 mode (6 clocks per machine cycle) or the clock may be further divided to reduce the operating frequency. In Fast mode the clock divider defaults to divide by 1.

The system clock source is selectable between the crystal oscillator, an externally driven clock and an internal 1.8432 MHz auxiliary oscillator. See “System Clock” on page 29 and “User Configuration Fuses” on page 86.

2.3.3 Reset

The RST pin of the AT89LP51/52 has selectable polarity using the POL pin (formerly $\overline{EA}$). When POL is high the RST pin is active high with a pull-down resistor and when POL is low the RST pin is active low with a pull-up resistor. For existing AT89S51/52 sockets where $\overline{EA}$ is tied to VDD, replacing AT89S51/52 with AT89LP51/52 will maintain the active high reset. Note that forcing external execution by tying $\overline{EA}$ low is not supported.

The AT89LP51/52 includes an on-chip Power-On Reset and Brown-out Detector circuit that ensures that the device is reset from system power up. In most cases a RC startup circuit is not required on the RST pin, reducing system cost, and the RST pin may be left unconnected if a board-level reset is not present.

2.3.4 Timer/Counters

A common prescaler is available to divide the time base for Timer 0, Timer 1, Timer 2 and the WDT. The TPS_{3-0} bits in the CLKREG SFR control the prescaler (Table 6-2 on page 31). In Compatibility mode TPS_{3-0} defaults to 0101B, which causes the timers to count once every machine cycle. The counting rate can be adjusted linearly from the system clock rate to 1/16 of the system clock rate by changing TPS_{3-0}. In Fast mode TPS_{3-0} defaults to 0000B, or the system clock rate. TPS does not affect Timer 2 in Clock Out or Baud Generator modes.

In Compatibility mode the sampling of the external Timer/Counter pins: T0, T1, T2 and T2EX; and the external interrupt pins, $\overline{INT0}$ and $\overline{INT1}$, is also controlled by the prescaler. In Fast mode these pins are always sampled at the system clock rate.

Both Timer 0 and Timer 1 can toggle their respective counter pins, T0 and T1, when they overflow by setting the output enable bits in TCONB.

The Watchdog Timer includes a 7-bit prescaler for longer timeout periods than the AT89S51/52. Note that in Fast Mode the WDIDLE and DISRTO bits are located in WDTCON and not in AUXR.

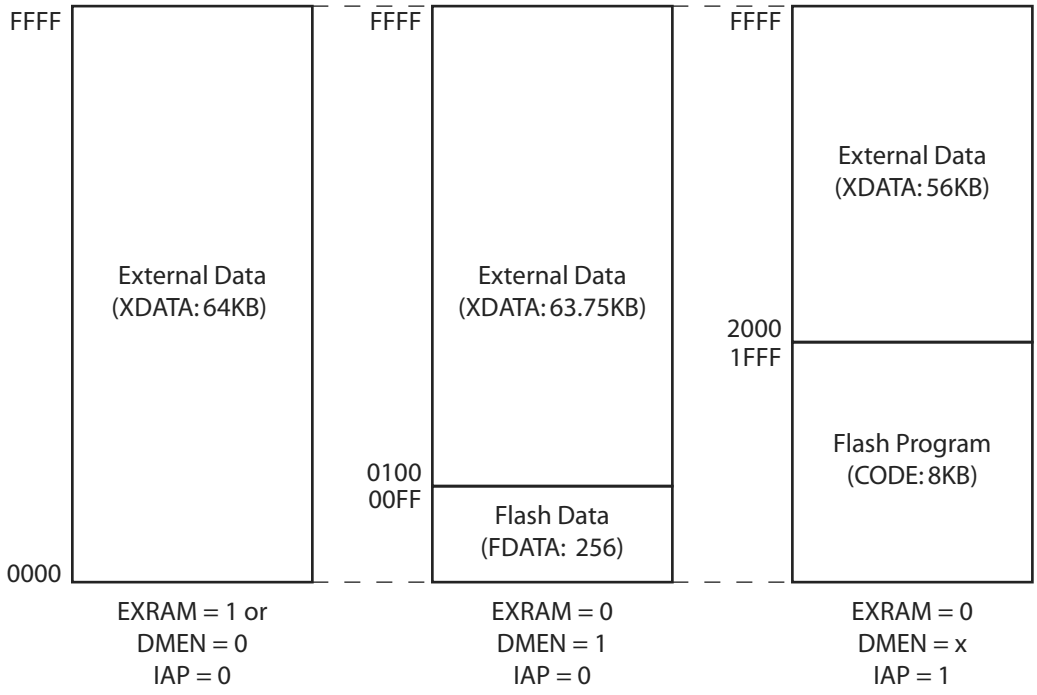
address space as shown in Figure 3-6. These memory spaces may require configuration before the CPU can access them. The AT89LP51/52 includes 256 bytes of nonvolatile Flash data memory (FDATA).

3.3.1 XDATA

The external data memory space can accommodate up to 64KB of external memory. The AT89LP51/52 uses the standard 8051 external data memory interface with the upper address byte on Port 2, the lower address byte and data in/out multiplexed on Port 0, and the ALE, $\overline{RD}$ and $\overline{WR}$ strobes. XDATA can be accessed with both 16-bit (MOVX @DPTR) and 8-bit (MOVX @Ri) addresses. See Section 3.3.3 on page 18 for more details of the external memory interface.

Some internal data memory spaces are mapped into portions of the XDATA address space. In this case the lower address ranges will access internal resources instead of external memory. Addresses above the range implemented internally will default to XDATA. The AT89LP51/52 supports up to 63.75K or 56K bytes of external memory when using the internally mapped memories. Setting the EXRAM bit (AUXR.1) to one will force all MOVX instructions to access the entire 64KB XDATA regardless of their address (See “AUXR – Auxiliary Control Register” on page 20).

Figure 3-6. External Data Memory Map



3.3.2 FDATA

The Flash Data Memory is a portion of the external memory space implemented as an internal nonvolatile data memory. Flash Data Memory is enabled by setting the DMEN bit (MEMCON.3) to one. When IAP = 0 and DMEN = 1, the Flash Data Memory is mapped into the FDATA space, at the bottom of the external memory address space, from 0000H to 00FFH. (See Figure 3-6). MOVX instructions to this address range will access the internal nonvolatile memory. FDATA is

Table 3-3. AUXR – Auxiliary Control Register

AUXR = 8EH — Reset Value = xxx0 0000B

Not Bit Addressable

	–	–	–	WDIDLE(1)	DISRTO(1) WS1(2)	WS0	EXRAM	DISALE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
WDIDLE	WDT Disable during Idle(1). When WDIDLE = 0 the WDT continues to count in Idle mode. When WDIDLE = 1 the WDT halts counting in Idle mode.
DISRTO	Disable Reset Output(1). When DISTRO = 0 the reset pin is driven to the same level as POL when the WDT resets. When DISRTO = 1 the reset pin is input only.
WS[1-0]	Wait State Select. Determines the number of wait states inserted into external memory accesses.

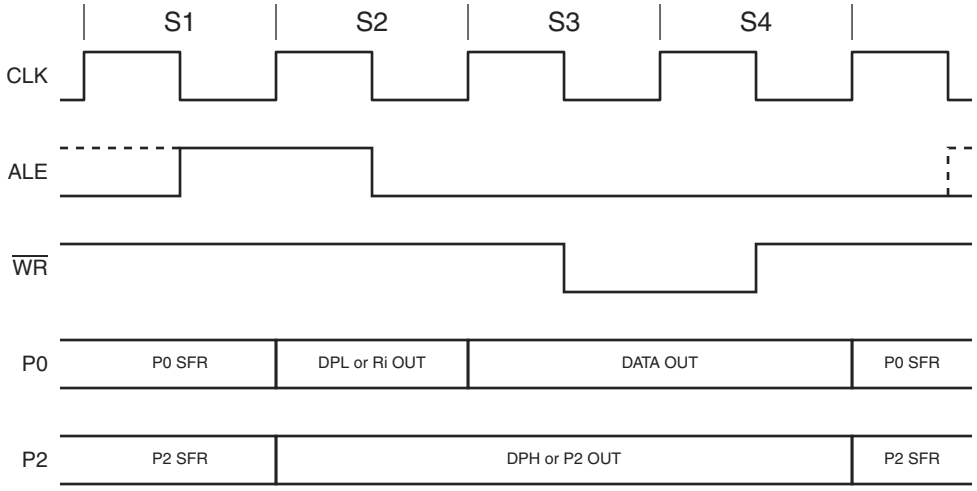
WS1(2)	WS0	Wait States	$\overline{RD}$ / $\overline{WR}$ Strobe Width	ALE to $\overline{RD}$ / $\overline{WR}$ Setup
0	0	0	1 x t_{CYC} (Fast); 3 x t_{CYC} (Compatibility)	1 x t_{CYC} (Fast); 1.5 x t_{CYC} (Compatibility)
0	1	1	2 x t_{CYC} (Fast); 15 x t_{CYC} (Compatibility)	1 x t_{CYC} (Fast); 1.5 x t_{CYC} (Compatibility)
1	0	2	2 x t_{CYC} (Fast)	2 x t_{CYC} (Fast)
1	1	3	3 x t_{CYC} (Fast)	2 x t_{CYC} (Fast)

EXRAM	External RAM Enable. When EXRAM = 0, MOVX instructions can access the internally mapped portions of the address space. Accesses to addresses above internally mapped memory will access external memory. Set EXRAM = 1 to bypass the internal memory and map the entire address space to external memory.
DISALE	ALE Disable. When DISALE = 0 the ALE pulse is active at 1/3 of the system clock frequency in Compatibility mode and 1/2 of the system clock frequency in Fast mode. When DISALES = 1 the ALE is inactive (high) unless an external memory access occurs. DISALE must be set to use P4.4 as a general I/O.

Notes: 1. AUXR.4 and AUXR.3 function as WDIDLE and DISRTO only in Compatibility mode. In Fast mode these bits are located in WDTCON.

2. WS1 is only available in Fast mode. WS1 is forced to 0 in Compatibility mode.

Figure 3-12. Fast Mode External Data Memory Write Cycle (WS = 00B)



6. System Clock

The system clock is generated directly from one of three selectable clock sources. The three sources are the on-chip crystal oscillator, external clock source, and internal RC oscillator. A diagram of the clock subsystem is shown in Figure 6-1. The on-chip crystal oscillator may also be configured for low or high power operation. The clock source is selected by the Clock Source User Fuses as shown in Table 6-1. See “User Configuration Fuses” on page 86. By default, in Fast mode no internal clock division is used to generate the CPU clock from the system clock. In Compatibility mode the default is to divide the oscillator output by two. The system clock divider may be used to prescale the system clock with other values. The choice of clock source also affects the start-up time after a POR, BOD or Power-down event (See “Reset” on page 32 or “Power-down Mode” on page 35)

Figure 6-1. Clock Subsystem Diagram

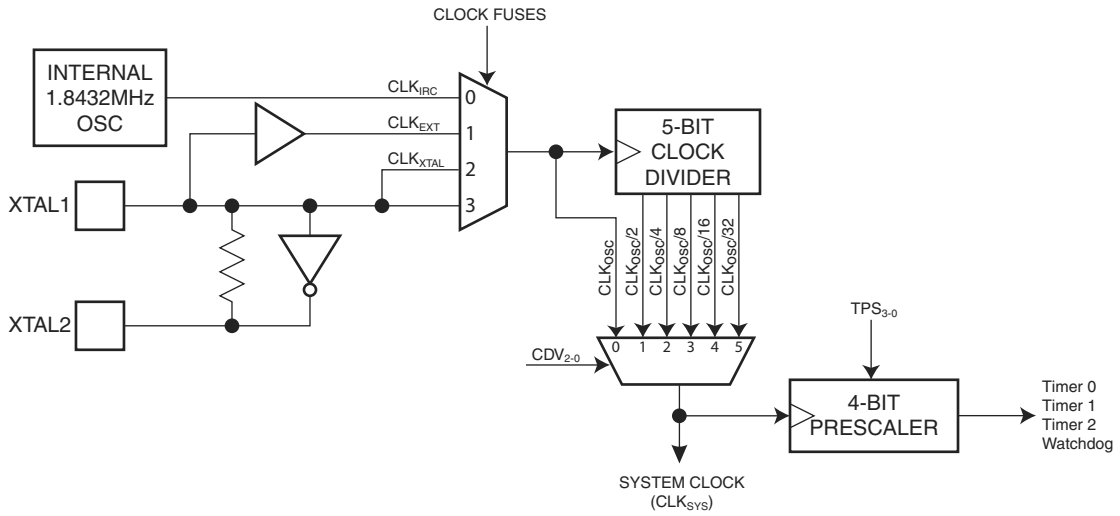


Table 6-1. Clock Source Settings

Clock Source Fuse 1	Clock Source Fuse 0	Selected Clock Source
1	1	High Power Crystal Oscillator (f > 12 MHz)
1	0	Low Power Crystal Oscillator (f ≤12 MHz)
0	1	External Clock on XTAL1
0	0	Internal 1.8432 MHz Auxiliary Oscillator

6.1 Crystal Oscillator

When enabled, the internal inverting oscillator amplifier is connected between XTAL1 and XTAL2 for connection to an external quartz crystal or ceramic resonator. The oscillator may operate in either high-power or low-power mode. Low-speed mode is intended for crystals of 12 MHz or less and consumes less power than the higher speed mode. The configuration as shown in Figure 6-2 applies for both high and low power oscillators. Note that in some cases, external capacitors C1 and C2 may **NOT** be required due to the on-chip capacitance of the XTAL1 and XTAL2 inputs (approximately 10 pF each). When using the crystal oscillator, P4.6 and P4.7 will have their inputs and outputs disabled. Also, XTAL2 in crystal oscillator mode should not be used to directly drive a board-level clock without a buffer.

instruction is 5 cycles long. If the instruction in progress is RETI, the additional wait time cannot be more than 9 cycles (a maximum of 4 more cycles to complete the instruction in progress, plus a maximum of 5 cycles to complete the next instruction). Thus, in a single-interrupt system, the response time is always more than 5 clock cycles and less than 14 clock cycles. See Figure 9-1 and Figure 9-2.

Figure 9-1. Minimum Interrupt Response Time (Fast Mode)

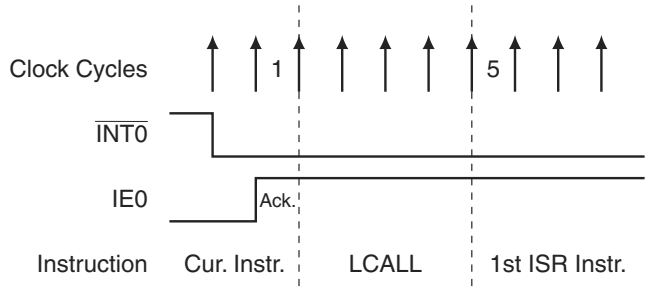


Figure 9-2. Maximum Interrupt Response Time (Fast Mode)

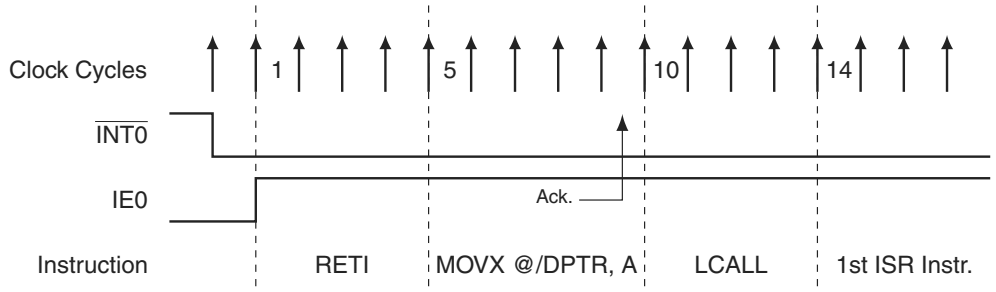


Figure 9-3. Minimum Interrupt Response Time (Compatibility Mode)

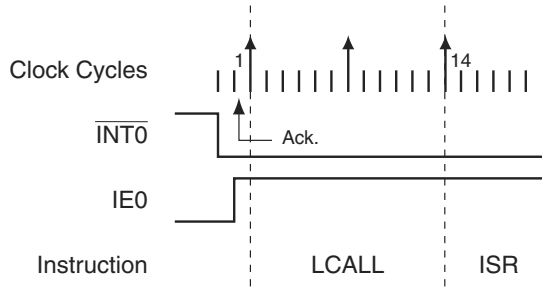
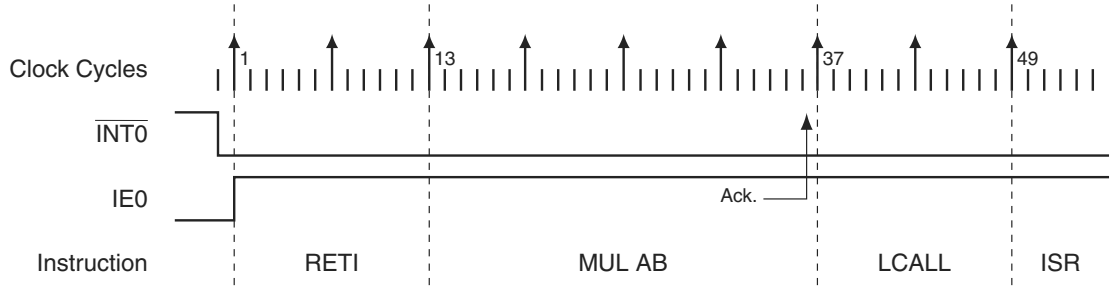


Figure 9-4. Maximum Interrupt Response Time (Compatibility Mode)



10. I/O Ports

The AT89LP51/52 can be configured for between 32 and 36 I/O pins. The exact number of I/O pins available depends on the clock, external memory and package type as shown in Table 10-1.

Table 10-1. I/O Pin Configurations

Clock Source	External Program Access	External Data Access	Number of I/O Pins
External Crystal or Resonator	Yes (PSEN+ALE+P0+P2)	Yes (RD+WR)	14
		No	16
	No	Yes (ALE+RD+WR+P0)	31
		No	34
External Clock	Yes (PSEN+ALE+P0+P2)	Yes (RD+WR)	15
		No	17
	No	Yes (ALE+RD+WR+P0)	32
		No	35
Internal RC Oscillator	Yes (PSEN+ALE+P0+P2)	Yes (RD+WR)	16
		No	18
	No	Yes (ALE+RD+WR+P0)	33
		No	36

10.1 Port Configuration

Each 8-bit port on the AT89LP51/52 may be configured in one of four modes: quasi-bidirectional (standard 8051 port outputs), push-pull output, open-drain output, or input-only. Port modes may be assigned in software on a port-by-port basis as shown in Table 10-2 using the PMOD register listed in Table 10-3. The Tristate-Port User Fuse determines the default state of the port pins (See “User Configuration Fuses” on page 86). When the fuse is enabled, all port pins default to input-only mode after reset. When the fuse is disabled, all port pins on P1, P2 and P3 default to quasi-bidirectional mode after reset and are weakly pulled high. P0 is set to Open-drain mode. P4 always operates in quasi-bidirectional mode.

Each port pin also has a Schmitt-triggered input for improved input noise rejection. During Power-down all the Schmitt-triggered inputs are disabled with the exception of P3.2 ($\overline{\text{INT0}}$), P3.3 ($\overline{\text{INT1}}$), RST, P4.6 (XTAL1) and P4.7 (XTAL2). Therefore, P3.2, P3.3, P4.6 and P4.7 should not be left floating during Power-down.

Table 10-2. Configuration Modes for Port x

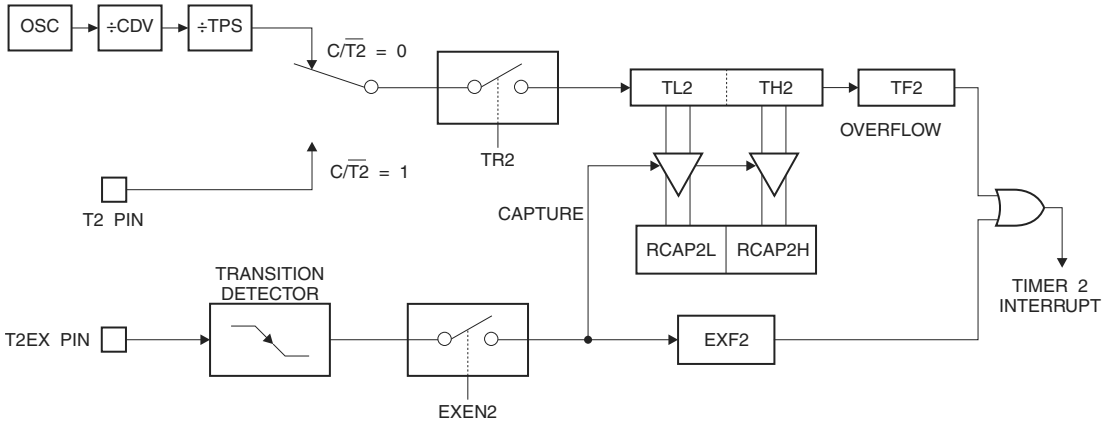
PxM0	PxM1	Port Mode
0	0	Quasi-bidirectional
0	1	Push-pull Output
1	0	Input Only (High Impedance)
1	1	Open-Drain Output

12.2 Capture Mode

In the Capture mode, Timer 2 is a fixed 16-bit timer or counter that counts up from MIN to MAX. An overflow from MAX to MIN sets bit TF2 in T2CON. If EXEN2 = 1, a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 and TF2 bits can generate an interrupt. Capture mode is illustrated in Figure 12-1. The Timer 2 overflow rate in Capture mode is given by the following equation:

$$\text{Capture Mode:} \qquad \text{Time-out Period} = \frac{65536}{\text{System Frequency}} \times (\text{TPS} + 1)$$

Figure 12-1. Timer 2 Diagram: Capture Mode



12.3 Auto-Reload Mode

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 12-4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin. A summary of the Auto-Reload behaviors is listed in Table 12-5.

Table 12-5. Summary of Auto-Reload Modes

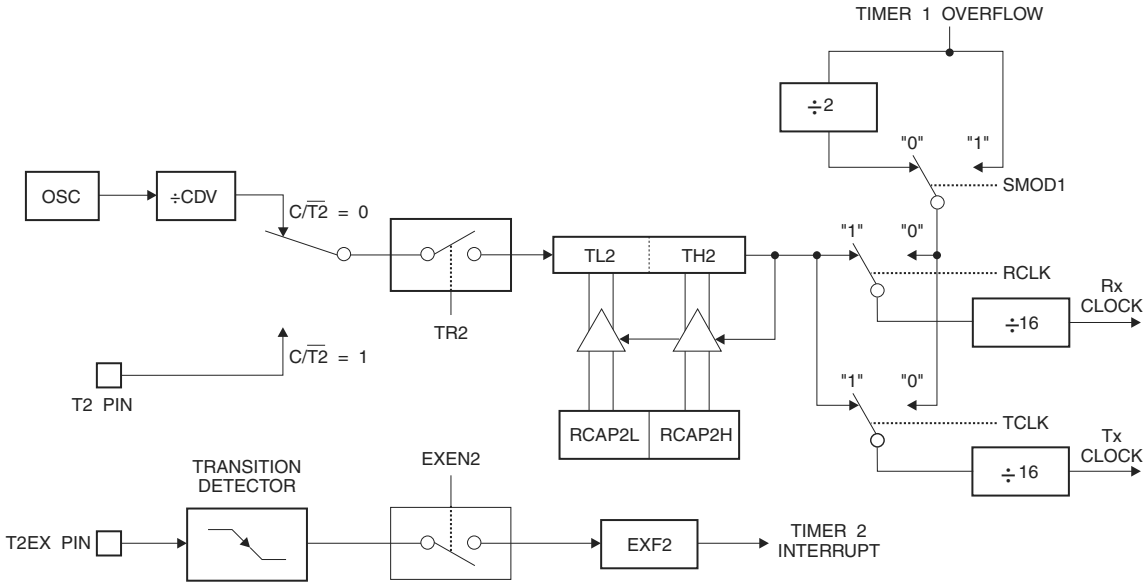
DCEN	T2EX	Direction	Behavior
0	X	Up	BOTTOM →MAX reload to BOTTOM
1	0	Down	MAX →BOTTOM underflow to MAX
1	1	Up	BOTTOM →MAX overflow to BOTTOM

12.3.1 Up Counter

Figure 12-2 shows Timer 2 automatically counting up when DCEN = 0. In this mode Timer 2 counts up to MAX and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with BOTTOM, the 16-bit value in RCAP2H and RCAP2L. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt. The Timer 2 overflow rate for this mode is given in the following equation:

$$\text{Auto-Reload Mode: DCEN = 0} \qquad \text{Time-out Period} = \frac{65536 - \{\text{RCAP2H}, \text{RCAP2L}\}}{\text{System Frequency}} \times (\text{TPS} + 1)$$

Figure 12-6. Timer 2 in Baud Rate Generator Mode



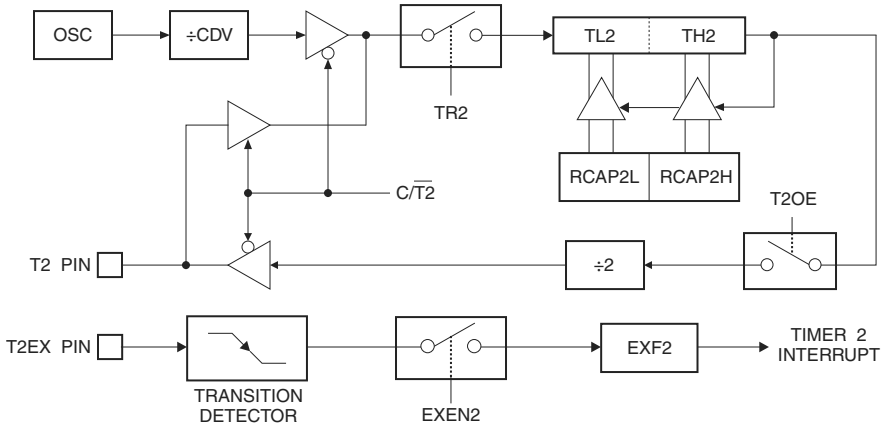
12.5 Frequency Generator (Programmable Clock Out)

Timer 2 can generate a 50% duty cycle clock on T2 (P1.0), as shown in Figure 13.. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to toggle its output at every timer overflow. To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer. The clock-out frequency depends on the system frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{System Frequency}}{2 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the frequency generator mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 12-7. Timer 2 in Clock-out Mode



Mode 0 transfers data LSB first whereas SPI or TWI are generally MSB first. Emulation of these interfaces may require bit reversal of the transferred data bytes. The following code example reverses the bits in the accumulator:

```
EX:    MOV  R7, #8
REVRS: RLC  A             ; C << msb (ACC)
       XCH  A, R6
       RRC  A             ; msb (ACC) >> B
       XCH  A, R6
       DJNZ R7, REVRS
```

14.5.2 Three-Wire (Full-Duplex) Mode

Three-Wire Mode is similar to Two-Wire except that the shift data input and data output are separated for full-duplex operation. Three-Wire Mode is enabled by setting the SPEN bit in TCONB. Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the 9th position of the transmit shift register and tells the TX Control Block to begin a transmission. The internal timing is such that one full bit slot may elapse between “write to SBUF” and activation of SEND.

SEND transfers the output of the shift register to the alternate output function line of P1.5, and also transfers Shift Clock to the alternate output function line of P1.7. As data bits shift out to the right, “0”s come in from the left. When the MSB of the data byte is at the output position of the shift register, the “1” that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain “0”s. This condition flags the TX Control block to do one last shift, then deactivate SEND and set TI.

Reception occurs simultaneously with transmission if REN = 1. Data is input from P1.6. When REN = 1 any write to SBUF causes the RX Control unit to write the bits 11111110B to the receive shift register and activates RECEIVE in the next clock phase. As data bits come in from the right, “1”s shift out to the left. When the “0” that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set. When REN = 0, the receiver is not enabled. When a transmission occurs, SBUF will not be updated and RI will not be set even though serial data is received on P1.6.

The relationship between the shift clock and data is identical to Two-Wire mode as listed in Table 14-5 and shown in Figure . Three-Wire mode uses different I/Os from Two-Wire mode and can be connected to SPI slave devices as shownin Figure 14-4. It is possible to time share the UART hardware between SPI devices connected on P1 and UART devices on P3 with the caveat that any asynchronous receptions on the RXD pin will be ignored while the UART is in Mode 0.

Figure 14-4. SPI Connections for UART Mode 0

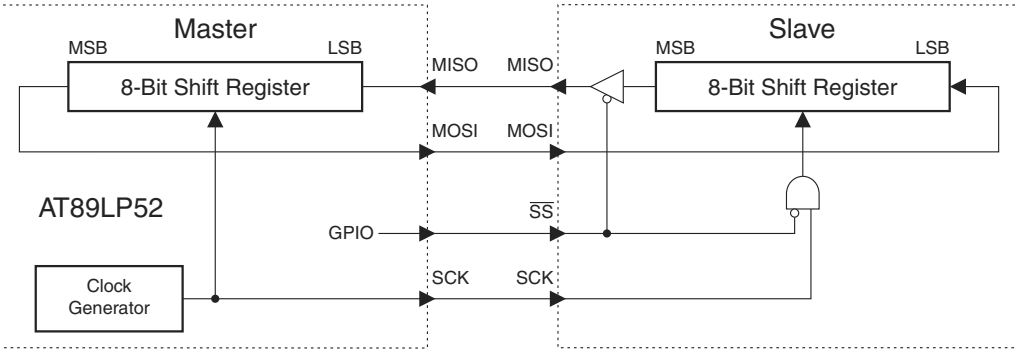
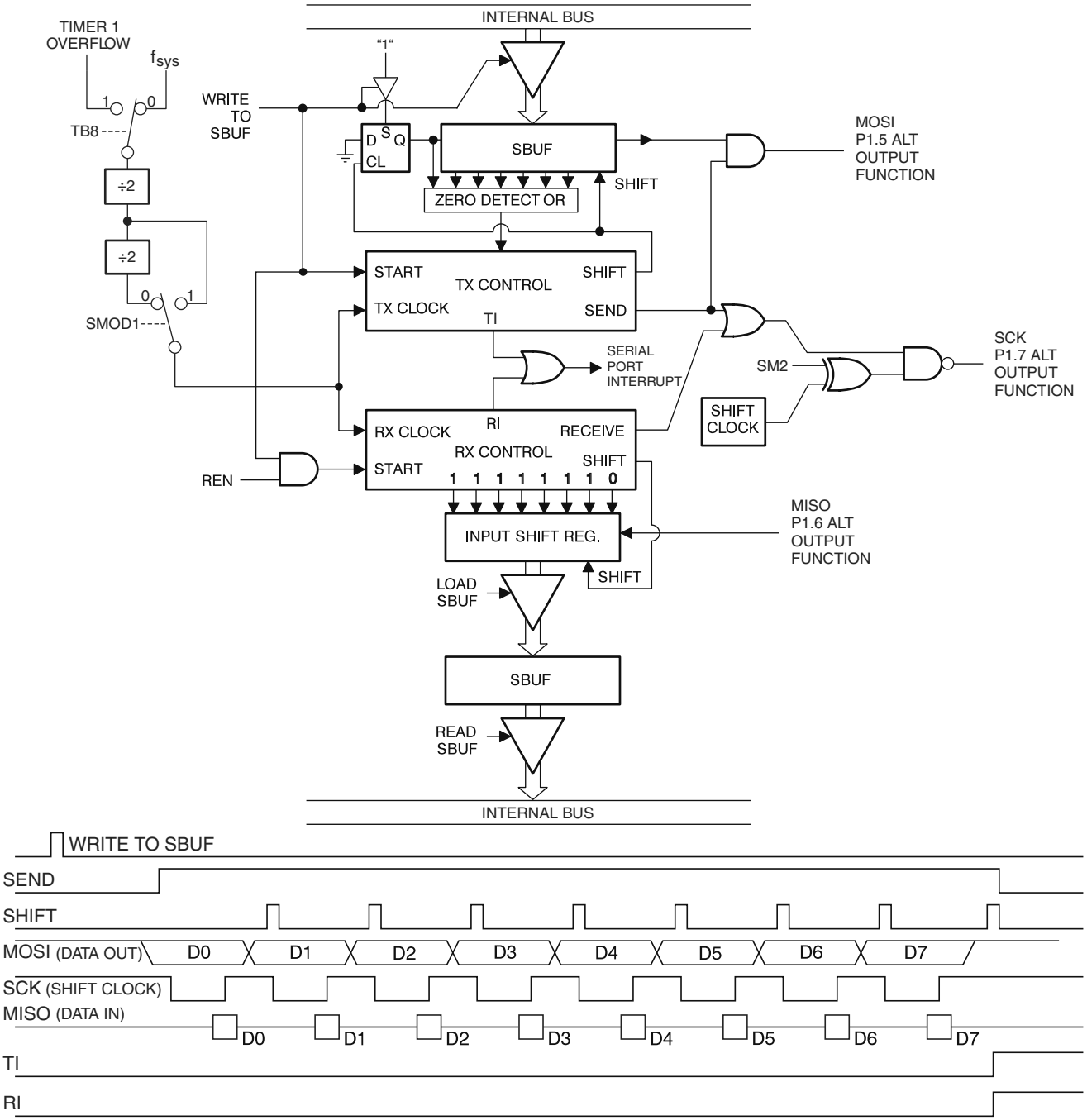


Figure 14-5. Serial Port Mode 0 (Three-Wire)



15. Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) protects the system from incorrect execution by triggering a system reset when it times out after the software has failed to feed the timer prior to the timer overflow. By Default the WDT counts CPU clock cycles. The prescaler bits, PS0, PS1 and PS2 in SFR WDTCON are used to set the period of the Watchdog Timer from 16K to 2048K clock cycles. The Timer Prescaler can also be used to lengthen the time-out period (see Table 6-2 on page 31) The WDT is disabled by Reset and during Power-down mode. When the WDT times out without being serviced, an internal RST pulse is generated to reset the CPU. See Table 15-1 for the available WDT period selections.

Table 15-1. Watchdog Timer Time-out Period Selection

WDT Prescaler Bits			Period(1) (Clock Cycles)
PS2	PS1	PS0	
0	0	0	16K
0	0	1	32K
0	1	0	64K
0	1	1	128K
1	0	0	256K
1	0	1	512K
1	1	0	1024K
1	1	1	2048K

Note: 1. The WDT time-out period is dependent on the system clock frequency.

$$\text{Time-out Period} = \frac{2^{(PS+14)}}{\text{System Frequency}} \times (TPS+1)$$

The Watchdog Timer consists of a 14-bit timer with 7-bit programmable prescaler. Writing the sequence 1EH/E1H to the WDTRST register enables the timer. When the WDT is enabled, the WDTEN bit in WDTCON will be set to “1”. To prevent the WDT from generating a reset when if overflows, the watchdog feed sequence must be written to WDTRST before the end of the time-out period. To feed the watchdog, two write instructions must be sequentially executed successfully. Between the two write instructions, SFR reads are allowed, but writes are not allowed. The instructions should move 1EH to the WDTRST register and then 1EH to the WDTRST register. An incorrect feed or enable sequence will cause an immediate watchdog reset. The program sequence to feed or enable the watchdog timer is as follows:

```
MOV WDTRST, #01Eh
MOV WDTRST, #0E1h
```

15.1 Software Reset

A Software Reset of the AT89LP51/52 is accomplished by writing the software reset sequence 5AH/A5H to the WDTRST SFR. The WDT does not need to be enabled to generate the software reset. A normal software reset will set the SWRST flag in WDTCON. However, if at any time an incorrect sequence is written to WDTRST (i.e. anything other than 1EH/E1H or 5AH/A5H), a software reset will immediately be generated and both the SWRST and WDTOVF flags will be set. In this manner an intentional software reset may be distinguished from a software error-generated reset. The program sequence to generate a software reset is as follows:

```
MOV WDTRST, #05Ah
MOV WDTRST, #0A5h
```

Table 15-2. WDTCON – Watchdog Control Register

WDTCON Address = A7H — Reset Value = 0000 0XX0B

Not Bit Addressable

	PS2	PS1	PS0	WDIDLE(1)	DISRTO(1)	SWRST	WDTOVF	WDTEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler bits for the watchdog timer (WDT). When all three bits are cleared to 0, the watchdog timer has a nominal period of 16K clock cycles. When all three bits are set to 1, the nominal period is 2048K clock cycles.
WDIDLE	WDT Disable during Idle(1). When WDIDLE = 0 the WDT continues to count in Idle mode. When WDIDLE = 1 the WDT halts counting in Idle mode.
DISRTO	Disable Reset Output(1). When DISTRO = 0 the reset pin is driven to the same level as POL when the WDT resets. When DISRTO = 1 the reset pin is input only.
SWRST	Software Reset Flag. Set when a software reset is generated by writing the sequence 5AH/A5H to WDTRST. Also set when an incorrect sequence is written to WDTRST. Must be cleared by software.
WDTOVF	Watchdog Overflow Flag. Set when a WDT rest is generated by the WDT timer overflow. Also set when an incorrect sequence is written to WDTRST. Must be cleared by software.
WDTEN	Watchdog Enable Flag. This bit is READ-ONLY and reflects the status of the WDT (whether it is running or not). The WDT is disabled after any reset and must be re-enabled by writing 1EH/E1H to WDTRST

Note: 1. WDTCON.4 and WDTCON.3 function as WDIDLE and DISRTO only in Fast mode. In Compatibility mode these bits are in AUXR. (See Table 3-3 on page 20)

Table 15-3. WDTRST – Watchdog Reset Register

WDTCON Address = A6H — **(Write-Only)**

Not Bit Addressable

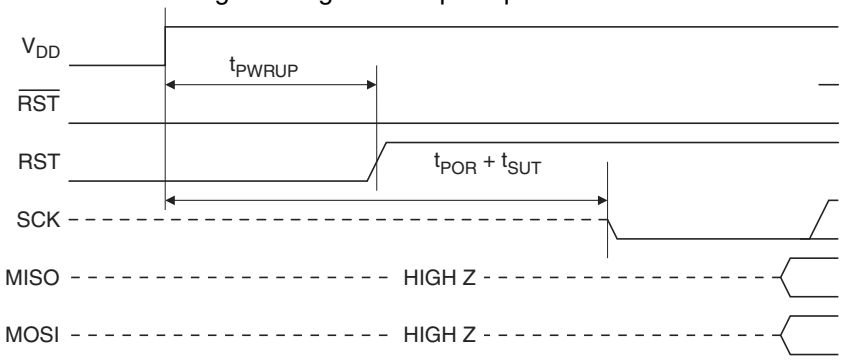
	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0

The WDT is enabled by writing the sequence 1EH/E1H to the WDTRST SFR. The current status may be checked by reading the WDTEN bit in WDTCON. To prevent the WDT from resetting the device, the same sequence 1EH/E1H must be written to WDTRST before the time-out interval expires. A software reset is generated by writing the sequence 5AH/A5H to WDTRST.

Table 16-1. Instruction Execution Times and Exceptions[1] (Continued)

MOV A, #data	2	6	2	74
MOV Rn, A	1	6	1	F8-FF
MOV Rn, direct	2	12	2	A8-AF
MOV Rn, #data	2	6	2	78-7F
MOV direct, A	2	6	2	F5
MOV direct, Rn	2	12	2	88-8F
MOV direct, direct	3	12	3	85
MOV direct, @Ri	2	12	2	86-87
MOV direct, #data	3	12	3	75
MOV @Ri, A	1	6	1	F6-F7
MOV @Ri, direct	2	12	2	A6-A7
MOV @Ri, #data	2	6	2	76-77
MOV DPTR, #data16	3	12	3	90
MOV /DPTR, #data16[2]	4	–	4	A5 90
MOVC A, @A+DPTR	1	12	3	93
MOVC A, @A+/DPTR[2]	2	–	4	A5 93
MOVC A, @A+PC	1	12	3	83
MOVX A, @Ri	1	12	2	E2-E3
MOVX A, @DPTR	1	12[3]	4[3]	E0
MOVX A, @/DPTR[2]	2	18[3]	5[3]	A5 E0
MOVX @Ri, A	1	12	2	F2-F3
MOVX @DPTR, A	1	12[3]	4[3]	F0
MOVX @/DPTR, A[2]	2	18[3]	5[3]	A5 F0
PUSH direct	2	12	2	C0
POP direct	2	12	2	D0
XCH A, Rn	1	6	1	C8-CF
XCH A, direct	2	6	2	C5
XCH A, @Ri	1	6	2	C6-C7
XCHD A, @Ri	1	6	2	D6-D7
		Clock Cycles		
Bit Operations	**Bytes**	**Compatibility**	**Fast**	**Hex Code**
CLR C	1	6	1	C3
CLR bit	2	6	2	C2
SETB C	1	6	1	D3
SETB bit	2	6	2	D2
CPL C	1	6	1	B3
CPL bit	2	6	2	B2
ANL C, bit	2	12	2	82
ANL C, bit	2	12	2	B0

Figure 17-9. Serial Programming Power-up Sequence

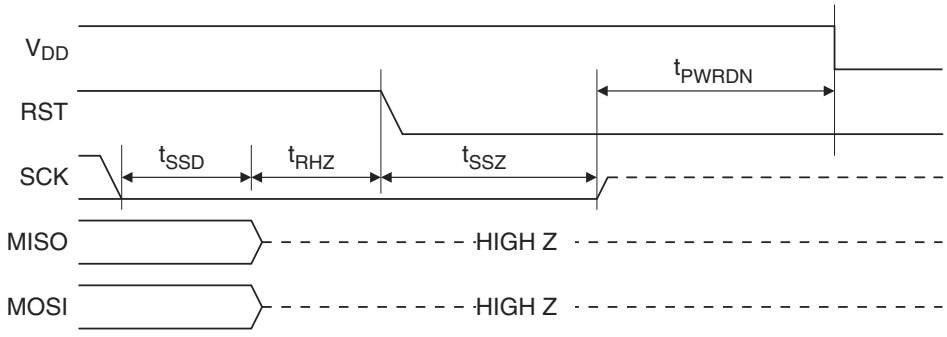


17.9.2 Power-down Sequence

Execute this sequence to power-down the device **after** programming.

1. Drive SCK low.
2. Wait at least t_{SSD} and Tristate MOSI.
3. Wait at least t_{RHZ} and drive RST low.
4. Wait at least t_{SSZ} and tristate SCK.
5. Wait no more than t_{PWRDN} and power off VDD.

Figure 17-10. Serial Programming Power-down Sequence



17.9.3 ISP Start Sequence

Execute this sequence to exit CPU execution mode and enter ISP mode when the device has passed Power-On Reset and is already operational.

1. Drive RST high.
2. Wait $t_{RLZ} + t_{STL}$.
3. Drive SCK low.
4. Start programming session.

17.9.6 Timing Parameters

The timing parameters for Figure 17-9, Figure 17-10, Figure 17-11, Figure 17-12, Figure 17-14 and Figure 17-15 are shown in Table .

Table 17-6. Programming Interface Timing Parameters

Symbol	Parameter	Min	Max	Units
t_{CLCL}	System Clock Cycle Time	0	60	ns
t_{PWRUP}	Power On to $\overline{SS}$ High Time	10		µs
t_{POR}	Power-on Reset Time		100	µs
t_{PWRDN}	$\overline{SS}$ Tristate to Power Off		1	µs
t_{RLZ}	RST Low to I/O Tristate	t_{CLCL}	2 t_{CLCL}	ns
t_{STL}	RST Low Settling Time	100		ns
t_{RHZ}	RST High to $\overline{SS}$ Tristate	0	2 t_{CLCL}	ns
t_{SCK}	Serial Clock Cycle Time	200[1]		ns
t_{SHSL}	Clock High Time	75		ns
t_{SLSH}	Clock Low Time	50		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns
t_{SIS}	Serial Input Setup Time	10		ns
t_{SIH}	Serial Input Hold Time	10		ns
t_{SOH}	Serial Output Hold Time		10	ns
t_{SOV}	Serial Output Valid Time		35	ns
t_{PIS}	Parallel Input Setup Time	10		ns
t_{PIH}	Parallel Input Hold Time	10		ns
t_{POH}	Parallel Output Hold Time		10	ns
t_{POV}	Parallel Output Valid Time		35	ns
t_{SOE}	Serial Output Enable Time		10	ns
t_{SOX}	Serial Output Disable Time		25	ns
t_{POE}	Parallel Output Enable Time		10	ns
t_{POX}	Parallel Output Disable Time		25	ns
t_{SSE}	RST Active Lead Time	t_{SLSH}		ns
t_{SSD}	RST Inactive Lag Time	t_{SLSH}		ns
t_{ZSS}	SCK Setup to $\overline{SS}$ Low	25		ns
t_{SSZ}	SCK Hold after $\overline{SS}$ High	25		ns
t_{WR}	Write Cycle Time	2.5		ms
t_{AWR}	Write Cycle with Auto-Erase Time	5		ms
t_{ERS}	Chip Erase Cycle Time	7.5		ms

Note: 1. t_{SCK} is independent of t_{CLCL}.

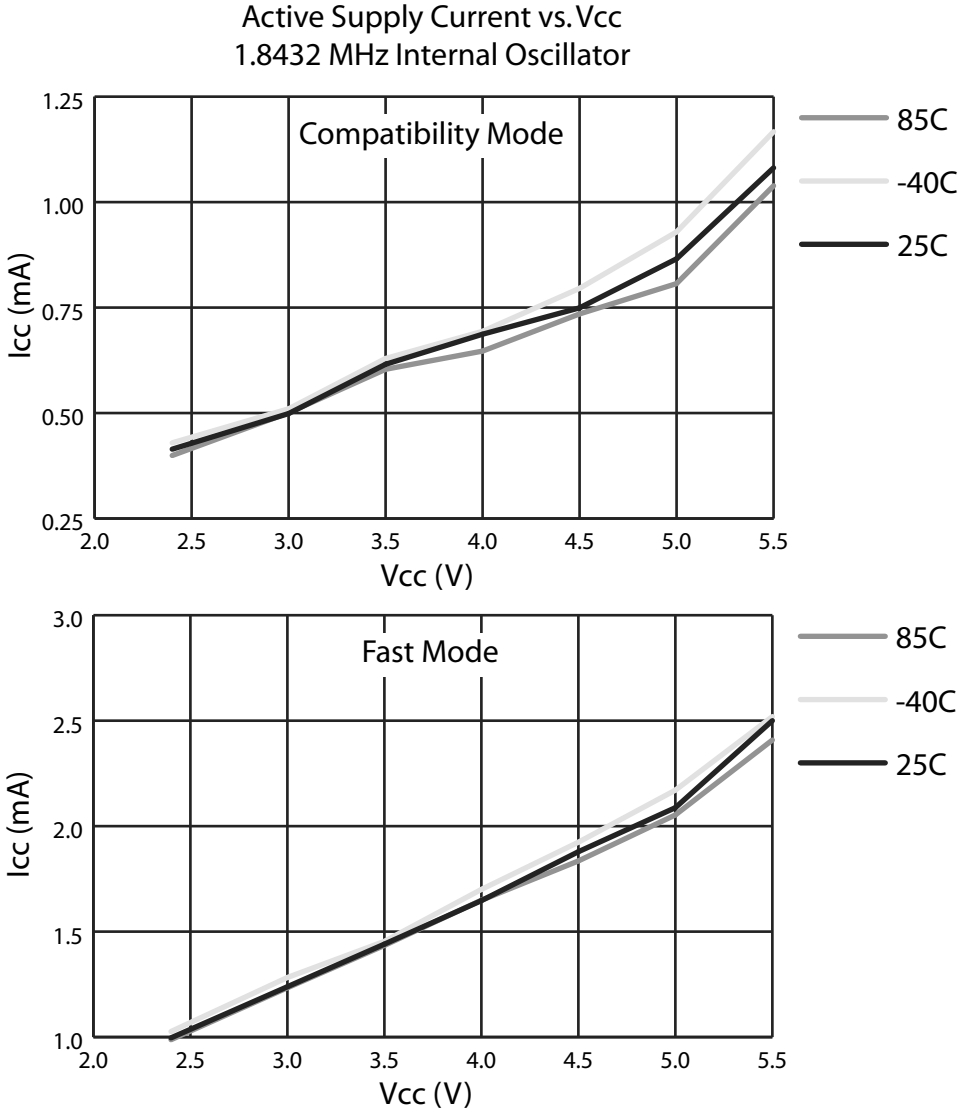
2. Minimum V_{DD} for Power-down is 2V.
3. Inputs are TTL-compatible when V_{DD} is 5V ± 10%

18.3 Typical Characteristics

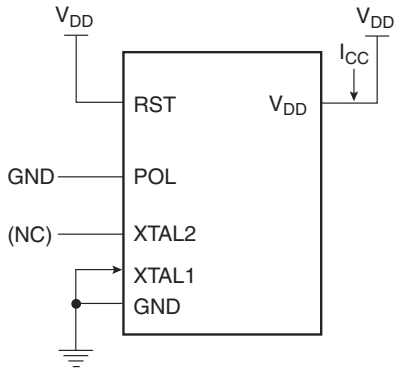
The following charts show typical behavior. These figures are not tested during manufacturing. All current consumption measurements are performed with all I/O pins configured as quasi-bidirectional (with internal pull-ups). A square wave generator with rail-to-rail output is used as an external clock source for consumption versus frequency measurements.

18.3.1 Supply Current (Internal Oscillator)

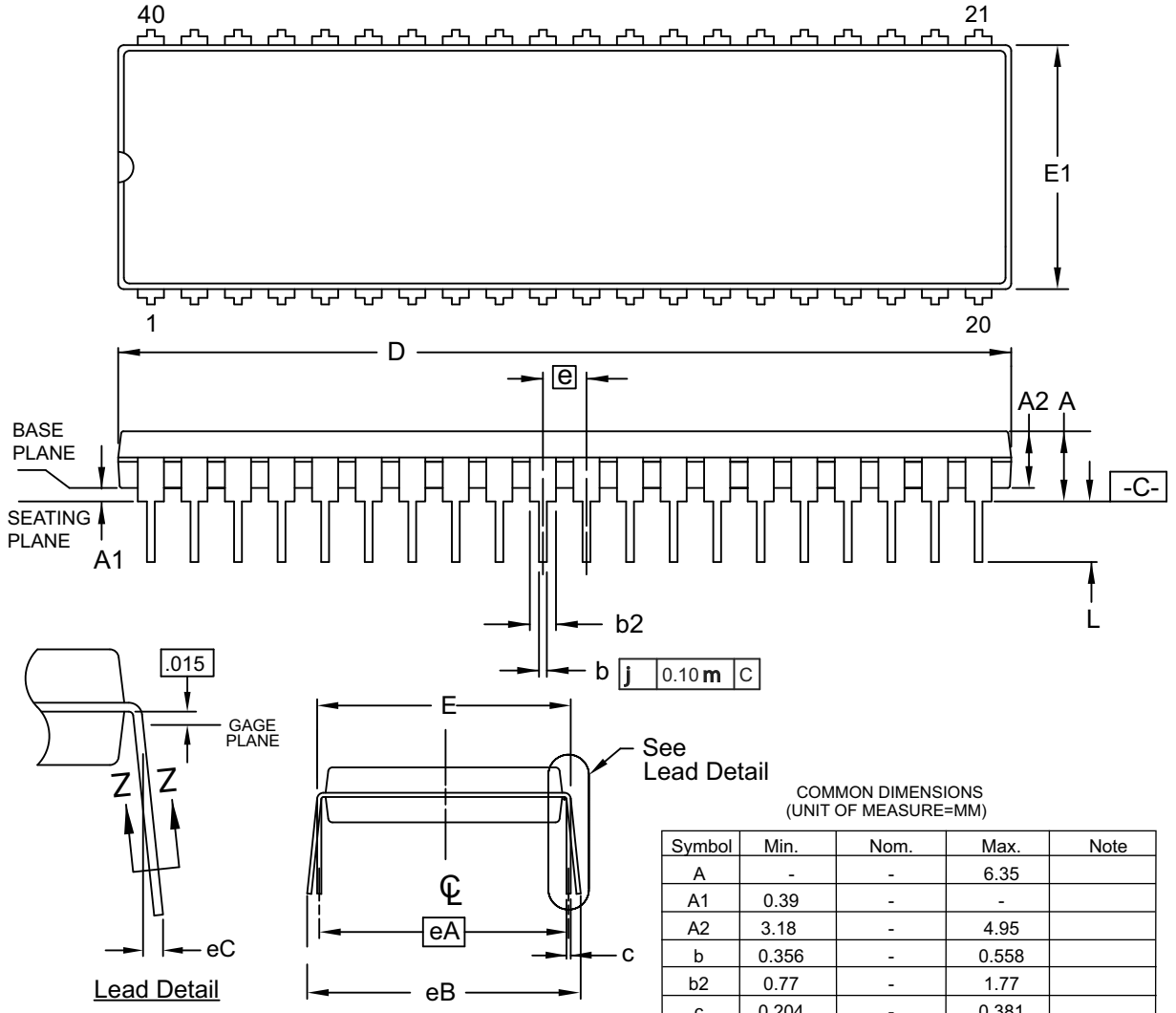
Figure 18-1. Active Supply Current vs. Vcc (1.8432 MHz Internal Oscillator)



18.8.6 I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{DD} = 2V to 5.5V



20.2 40P6 – PDIP



COMMON DIMENSIONS
(UNIT OF MEASURE=MM)

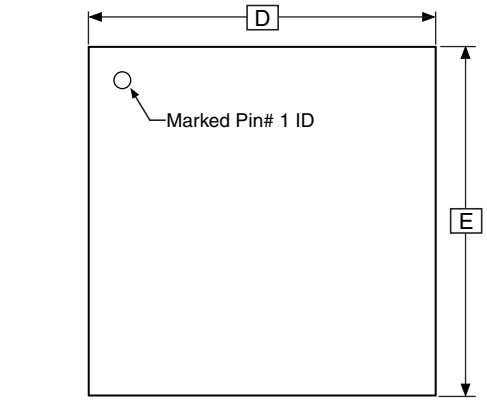
Symbol	Min.	Nom.	Max.	Note
A	-	-	6.35	
A1	0.39	-	-	
A2	3.18	-	4.95	
b	0.356	-	0.558	
b2	0.77	-	1.77	
c	0.204	-	0.381	
D	50.3	-	53.2	Note 2
E	15.24	-	15.87	
E1	12.32	-	14.73	Note 2
L	2.93	-	5.08	
e	2.54 BSC			
eA	15.24 BSC			
eB	-	-	17.78	
eC	0.000	-	1.524	

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

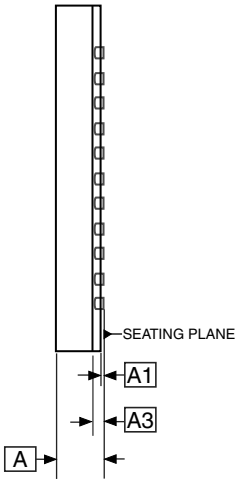
11/28/11

Package Drawing Contact: packagedrawings@atmel.com	**TITLE** **40P6**, 40-lead, 0.600”/15.24 mm Wide Plastic Dual Inline Package (PDIP)	**GPC** PBL	**DRAWING NO.** 40P6	**REV.** C

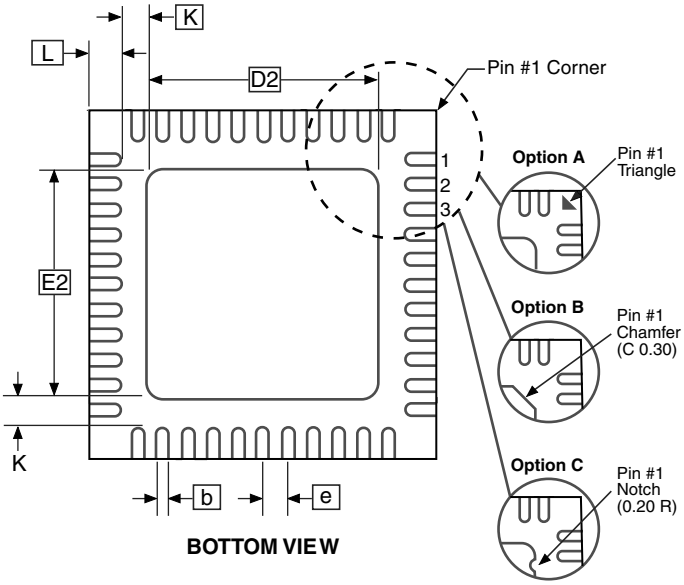
20.4 44M1 – VQFN/MLF



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

9/26/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	44M1, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)	ZWS	44M1	H