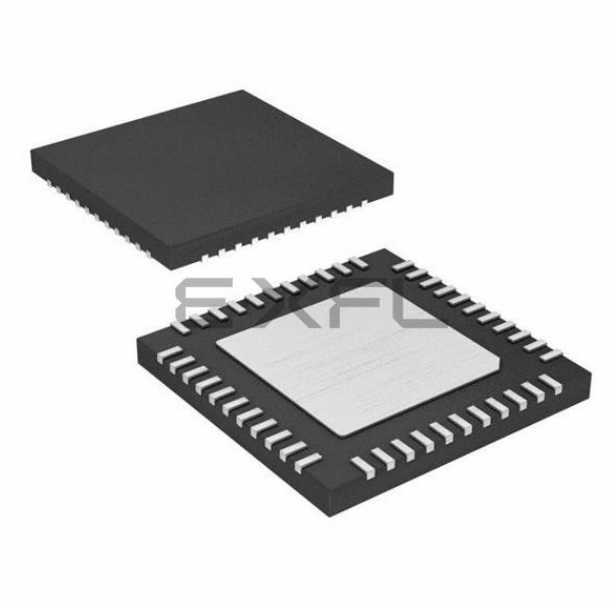

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp52-20mu

2.3.5 Interrupt Handling

With the addition of the IPH register, the AT89LP51/52 provides four levels of interrupt priority for greater flexibility in handling multiple interrupts. Also, Fast mode allows for faster interrupt response due to the shorter instruction execution times.

2.3.6 Serial Port

The timer prescaler increases the range of achievable baud rates when using Timer 1 to generate the baud rate in UART Modes 1 or 3, including an increase in the maximum baud rate available in Compatibility mode. Additional features include automatic address recognition and framing error detection.

The shift register mode (Mode 0) has been enhanced with more control of the polarity, phase and frequency of the clock and full-duplex operation. This allows emulation of master serial pheriperal (SPI) and two-wire (TWI) interfaces.

2.3.7 I/O Ports

The P0, P1, P2 and P3 I/O ports of the AT89LP51/52 may be configured in four different modes. The default setting depends on the Tristate-Port User Fuse (See Section 17.7 on page 86). When the fuse is set all the I/O ports revert to input-only (tristated) mode at power-up or reset. When the fuse is not active, ports P1, P2 and P3 start in quasi-bidirectional mode and P0 starts in open-drain mode. P4 always operates in quasi-bidirectional mode. P0 can be configured to have internal pull-ups by placing it in quasi-bidirectional or output modes. This can reduce system cost by removing the need for external pull-ups on Port 0.

The P4.4–P4.7 pins are additional I/Os that replace the normally dedicated ALE, PSEN, XTAL1 and XTAL2 pins of the AT89S51/52. These pins can be used as additional I/Os depending on the configuration of the clock and external memory.

2.3.8 Security

The AT89LP51/52 does not support the extenal access pin ($\overline{EA}$). Therefore it is not possible to execute from external program memory in address range 0000H–1FFFH. When the third Lockbit is enabled (Lock Mode 4) external program execution is disabled for all addresses above 1FFFH. This differs from AT89S51/52 where Lock Mode 4 prevents $\overline{EA}$ from being sampled low, but may still allow external execution at addresses outside the 8K internal space.

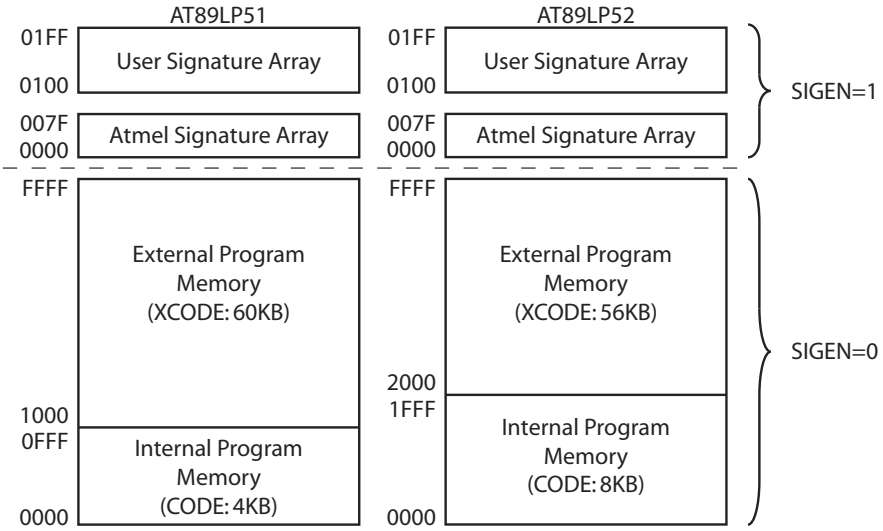
2.3.9 Programming

The AT89LP51/52 supports a richer command set for In-System Programming (ISP). Existing AT89S51/52 programmers should be able to program the AT89LP51/52 in byte mode. In page mode the AT89LP51/52 only supports programming of a half-page of 64 bytes and therefore requires an extra address byte as compared to AT89S51/52. Furthermore the device signature is located at addresses 0000H, 0001H and 0003H instead of 0000H, 0100H and 0200H.

Table 2-3. Compatibility Mode versus Fast Mode Summary

Feature	Compatibility	Fast
Instruction Fetch in System Clocks	3	1
Instruction Execution Time in System Clocks	6, 12, 18 or 24	1, 2, 3, 4 or 5
Default System Clock Divisor	2	1
Default Timer Prescaler Divisor	6	1

Figure 3-1. Program Memory Map



3.1.1 External Program Memory Interface

The AT89LP51/52 uses the standard 8051 external program memory interface with the upper address on Port 2, the lower address and data in/out multiplexed on Port 0, and the ALE and $\overline{\text{PSEN}}$ strobes. Program memory addresses are always 16-bits wide, even though the actual amount of program memory used may be less than 64K byes. External program execution sacrifices two full 8-bit ports, P0 and P2, to the function of addressing the program memory.

Figure 3-2 shows a hardware configuration for accessing up to 64K bytes of external ROM using a 16-bit linear address. Port 0 serves as a multiplexed address/data bus to the ROM. The Address Latch Enable strobe (ALE) is used to latch the lower address byte into an external register so that Port 0 can be freed for data input/output. Port 2 provides the upper address byte throughout the operation. $\overline{\text{PSEN}}$ strobes the external memory.

Figure 3-3 shows the timing of the external program memory interface. ALE is emitted at a constant rate of 1/3 of the system clock with a 1/3 duty cycle. $\overline{\text{PSEN}}$ is emitted at a similar rate, but with 50% duty cycle. The new address changes in the middle of the ALE pulse for latching on the falling edge and is tristated at the falling edge of $\overline{\text{PSEN}}$. The instruction data is sampled from P0 and latched internally during the high phase of the clock prior to the rising edge of $\overline{\text{PSEN}}$. This timing applies to both Compatibility and Fast modes. In Compatibility mode there is no difference in instruction timing between internal and external execution.

Figure 3-2. Executing from External Program Memory

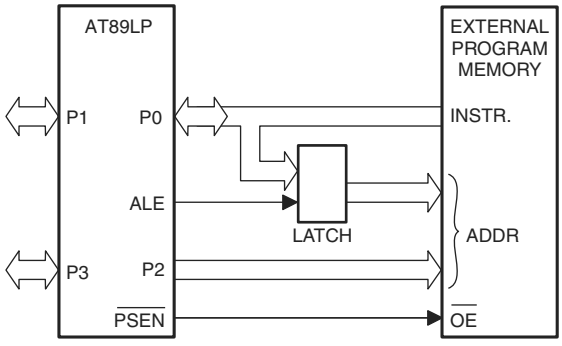
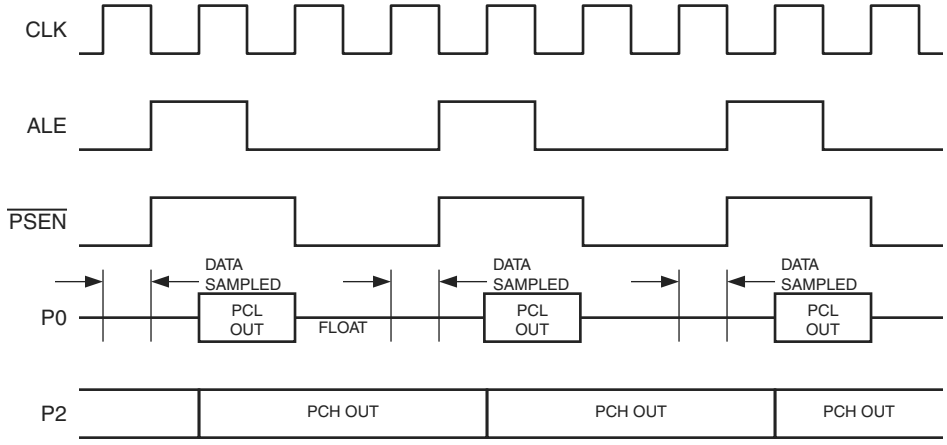
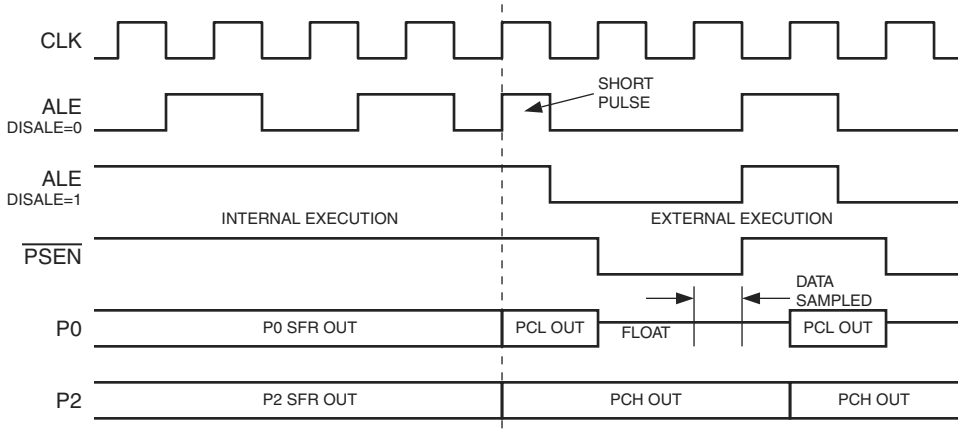


Figure 3-3. External Program Memory Fetches



In order for Fast mode to fetch externally, two wait states must be inserted for every clock cycle, increasing the instruction execution time by a factor of 3. However, due to other optimizations, external Fast mode instructions may still be 1/4 to 1/2 faster than their Compatibility mode equivalents. Note that if ALE is allowed to toggle in Fast mode, there is a possibility that when the CPU jumps from internal to external execution a short pulse may occur on ALE as shown in Figure 3-4. The setup time from the address to the falling edge of ALE remains the same. However, this behavior can be avoided by setting the DISALE bit prior to any jump above the 8K border.

Figure 3-4. Internal/External Program Memory Boundary (Fast Mode)



3.1.2 SIG

In addition to the 64K code space, the AT89LP51/52 also supports a 256-byte User Signature Array and a 128-byte Atmel Signature Array that are accessible by the CPU. The Atmel Signature Array is initialized with the Device ID in the factory. The User Signature Array is available for user identification codes or constant parameter data. Data stored in the signature array is not secure. Security bits will disable writes to the array; however, reads by an external device programmer are always allowed.

In order to read from the signature arrays, the SIGEN bit (AUXR1.3) must be set (See Table 5-3 on page 28). While SIGEN is one, MOVC A,@A+DPTR will access the signature arrays. The User Signature Array is mapped from addresses 0100h to 01FFh and the Atmel Signature Array is mapped from addresses 0000h to 007Fh. SIGEN must be cleared before using MOVC to

Figure 3-13. Fast Mode External Data Memory Read Cycle (WS = 00B)

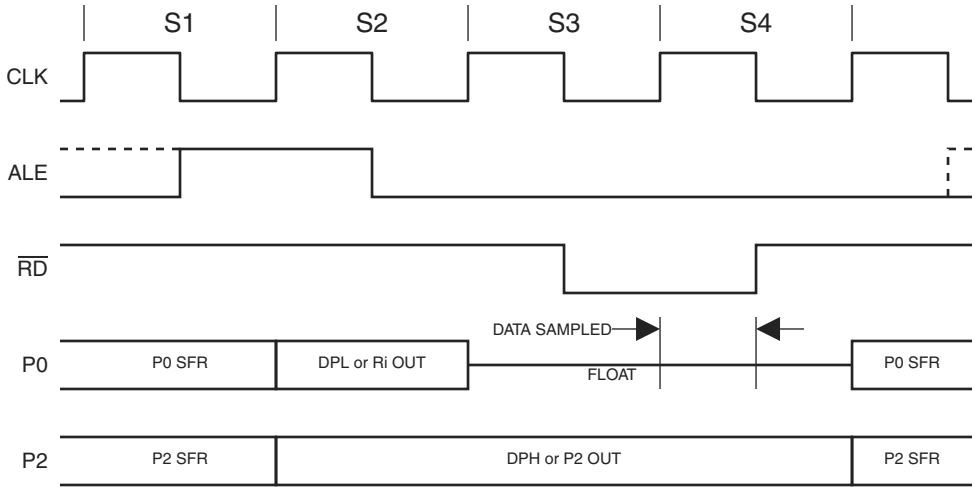


Figure 3-14. Compatibility Mode External Data Memory Write Cycle (WS0 = 0)

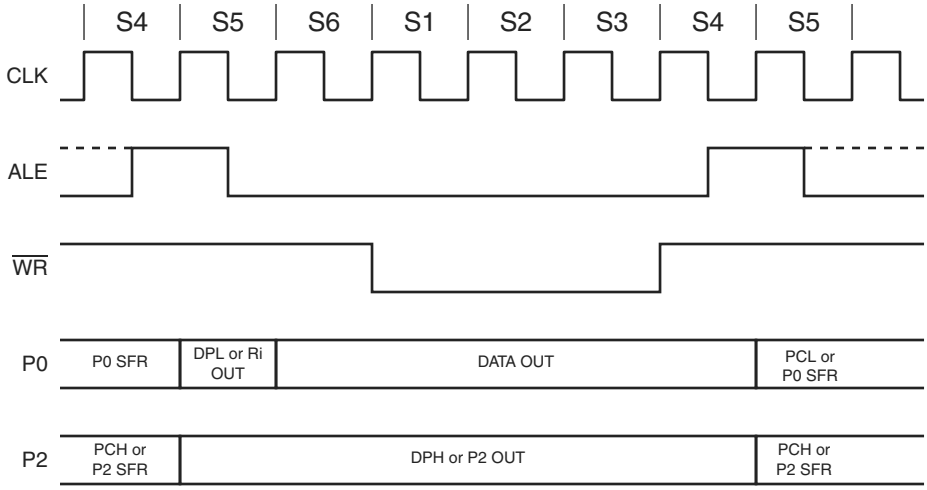


Figure 3-15. Compatibility Mode External Data Memory Read Cycle (WS0 = 0)

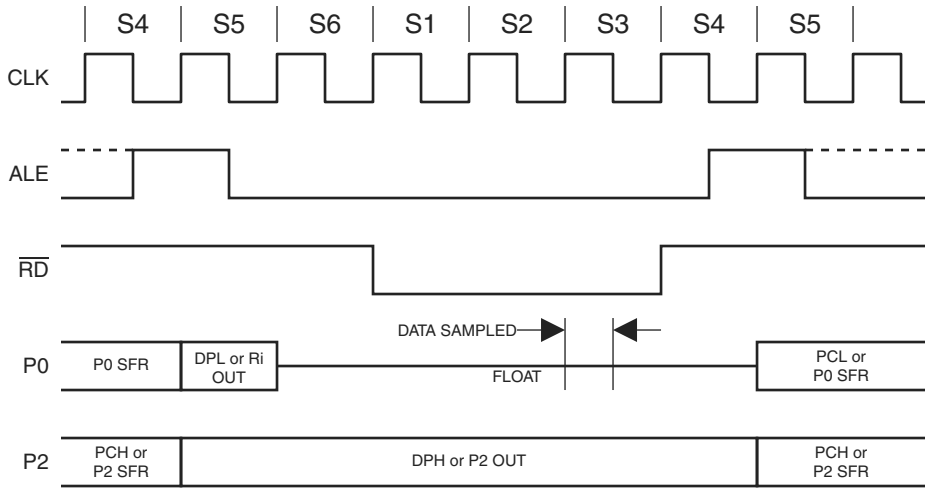


Figure 3-16. MOVX with One Wait State (WS = 01B)

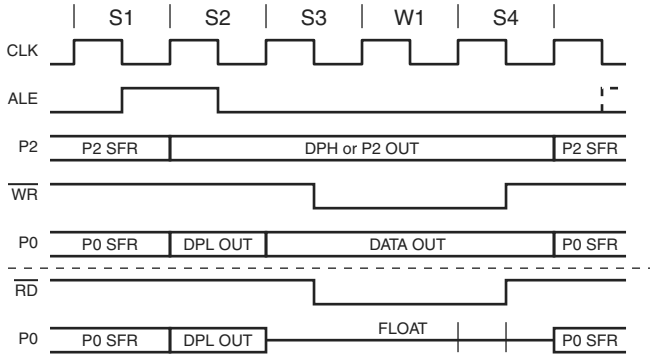


Figure 3-17. MOVX with Two Wait States (WS = 10B)

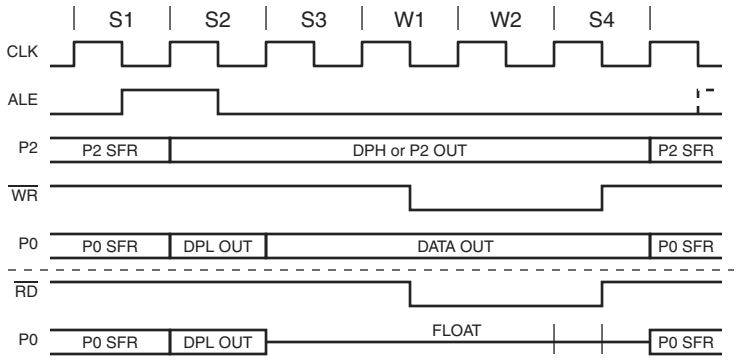
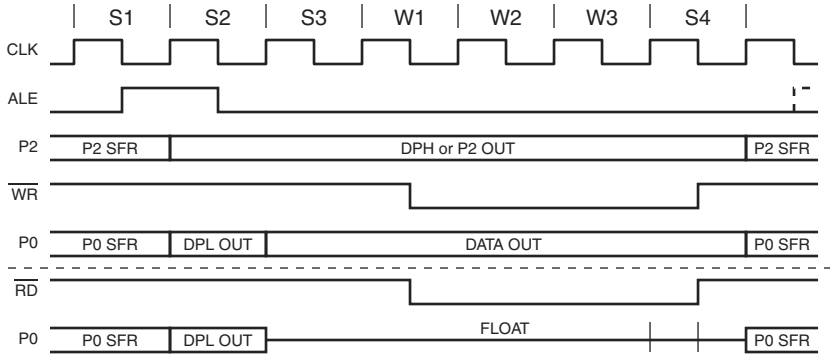
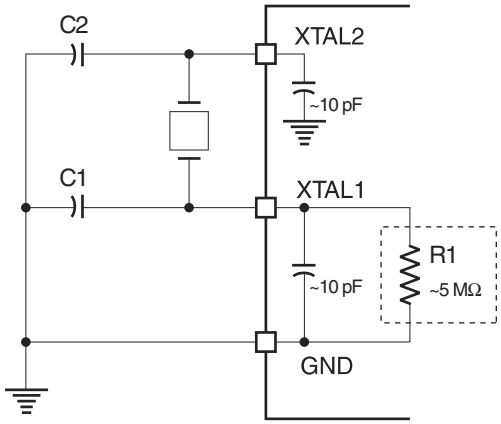


Figure 3-18. MOVX with Three Wait States (WS = 11B)



An optional 5 MΩ on-chip resistor can be connected between XTAL1 and GND. This resistor can improve the startup characteristics of the oscillator especially at higher frequencies. The resistor can be enabled/disabled with the R1 User Fuse (See “User Configuration Fuses” on page 86.)

Figure 6-2. Crystal Oscillator Connections

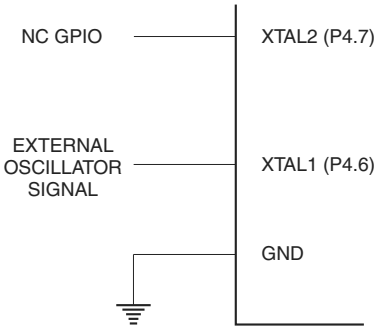


Note: 1. C1, C2 = 5 pF ±5pF for Crystals
= 5 pF ±5pF for Ceramic Resonators

6.2 External Clock Source

The external clock option disables the oscillator amplifier and allows XTAL1 to be driven directly by an external clock source as shown in Figure 6-3. XTAL2 may be left unconnected, used as general purpose I/O P4.7, or configured to output a divided version of the system clock.

Figure 6-3. External Clock Drive Configuration



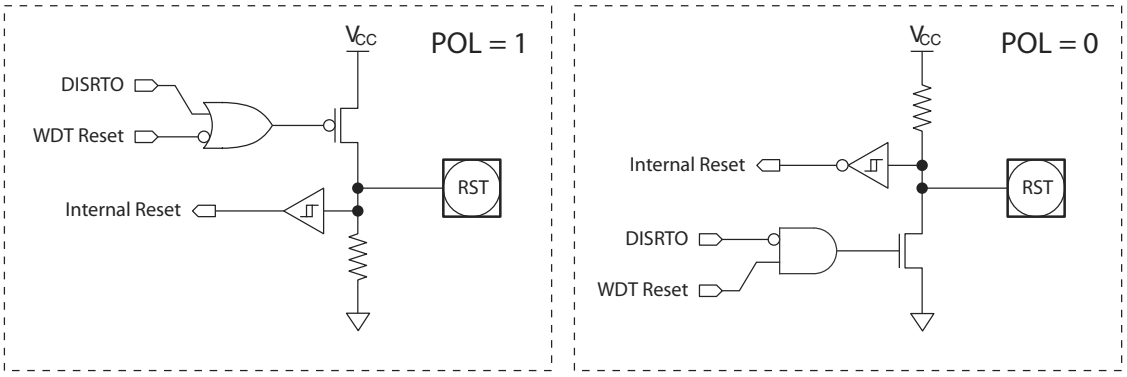
6.3 Internal RC Oscillator

The AT89LP51/52 has an Internal Auxiliary oscillator tuned to 1.8432 MHz ±2.0%. When enabled as the clock source, XTAL1 and XTAL2 may be used as P4.6 and P4.7 respectively.

The AT89LP51/52 includes an on-chip Power-On Reset and Brown-out Detector circuit that ensures that the device is reset from system power up. In most cases a RC startup circuit is not required on the RST pin, reducing system cost, and the RST pin may be left unconnected if a board-level reset is not present.

Note: RST also serves as the In-System Programming (ISP) enable. ISP is enabled when the external reset pin is held active. When ISP is disabled by fuse, ISP may only be entered by pulling RST active during power-up. If this behavior is necessary, it is recommended to use an active-low reset so that ISP can be entered by shorting RST to GND at power-up.

Figure 7-3. Reset Pin Structure



7.4 Watchdog Reset

When the Watchdog times out, it will generate a reset pulse lasting 49 clock cycles. By default this pulse is also output on the RST pin. To disable the RST output the DISRTO bit in AUXR (Compatibility mode) or WDTCON (Fast mode) must be set to one. Watchdog reset will set the WDTOVF flag in WDTCON. To prevent a Watchdog reset, the watchdog reset sequence 1EH/E1H must be written to WDTRST before the Watchdog times out. See “Programmable Watchdog Timer” on page 73. for details on the operation of the Watchdog.

7.5 Software Reset

The CPU may generate a 49-clock cycle reset pulse by writing the software reset sequence 5AH/A5H to the WDRST register. A software reset will set the SWRST bit in WDTCON. See “Software Reset” on page 73 for more information on software reset. Writing any sequences other than 5AH/A5H or 1EH/E1H to WDTRST will generate an immediate reset and set both WDTOVF and SWRST to flag an error. Software reset will also drive the RST pin active unless DISRTO is set.

8. Power Saving Modes

The AT89LP51/52 supports two different power-reducing modes: Idle and Power-down. These modes are accessed through the PCON register. Additional steps may be required to achieve the lowest possible power consumption while using these modes.

8.1 Idle Mode

Setting the IDL bit in PCON enters idle mode. Idle mode halts the internal CPU clock. The CPU state is preserved in its entirety, including the RAM, stack pointer, program counter, program status word, and accumulator. The Port pins hold the logic states they had at the time that Idle was activated. Idle mode leaves the peripherals running in order to allow them to wake up the

11. Timer 0 and Timer 1

The AT89LP51/52 has two 16-bit Timer/Counters, Timer 0 and Timer 1, with the following features:

- Two independent 16-bit timer/counters with 8-bit reload registers
- UART baud rate generation using Timer 1
- Output pin toggle on timer overflow
- Split timer mode allows for three separate timers (2 8-bit, 1 16-bit)
- Gated modes allow timers to run/halt based on an external input

Timer 0 and Timer 1 have similar modes of operation. As timers, the timer registers normally increase every clock cycle. Thus, the registers count clock cycles. The timer rate can be prescaled by a value between 1 and 16 using the Timer Prescaler (see Table 6-2 on page 31). Both Timers share the same prescaler. In Compatibility mode CDV defaults to 2, so a clock cycle consists of two oscillator periods,and the prescaler defaults to 6 making the count rate equal to 1/12 of the oscillator frequency. By default in Fast mode CDV = 0 and TPS = 0 so the count rate is equal to the oscillator frequency.

As counters, the timer registers are incremented in response to a 1-to-0 transition at the corresponding input pins, T0 or T1. In Fast mode the external input is sampled every clock cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since 2 clock cycles are required to recognize a 1-to-0 transition, the maximum count rate is 1/2 of the system frequency. There are no restrictions on the duty cycle of the input signal, but it should be held for at least one full clock cycle to ensure that a given level is sampled at least once before it changes.

In Compatibility mode the counter input sampling is controlled by the prescaler. Since TPS defaults to 6 in this mode, the pins are sampled every six system clocks. Therefore the input signal should be held for at least six clock cycles to ensure that a given level is sampled at least once before it changes.

Furthermore, the Timer or Counter functions for Timer 0 and Timer 1 have four operating modes: 13-bit timer, 16-bit timer, 8-bit auto-reload timer, and split timer. The control bits C/T in the Special Function Register TMOD select the Timer or Counter function. The bit pairs (M1, M0) in TMOD select the operating modes.

Table 11-1. Timer 0/1 Register Summary

Name	Address	Purpose	Bit-Addressable
TCON	88H	Control	Y
TMOD	89H	Mode	N
TL0	8AH	Timer 0 low-byte	N
TL1	8BH	Timer 1 low-byte	N
TH0	8CH	Timer 0 high-byte	N
TH1	8DH	Timer 1 high-byte	N
TCONB	91H	Mode	N

Figure 12-2. Timer 2 Diagram: Auto-Reload Mode (DCEN = 0)

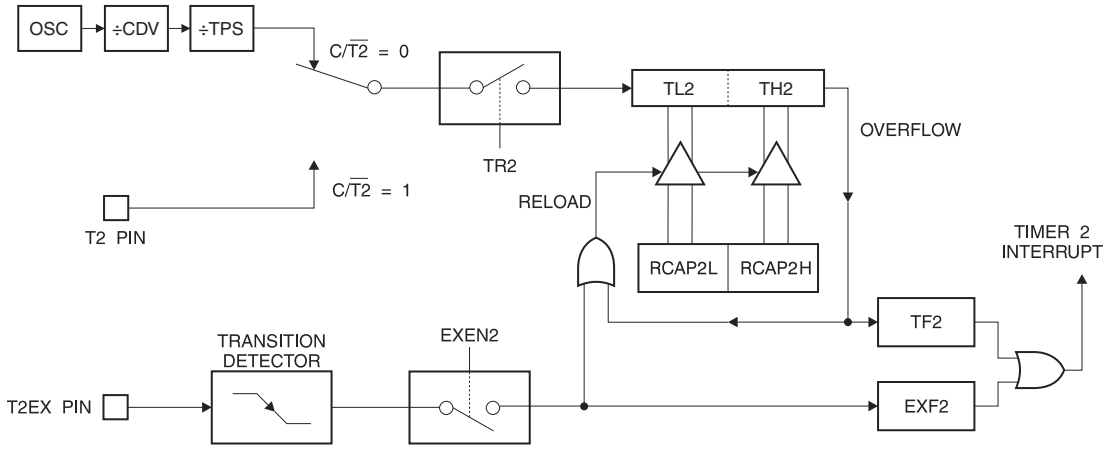
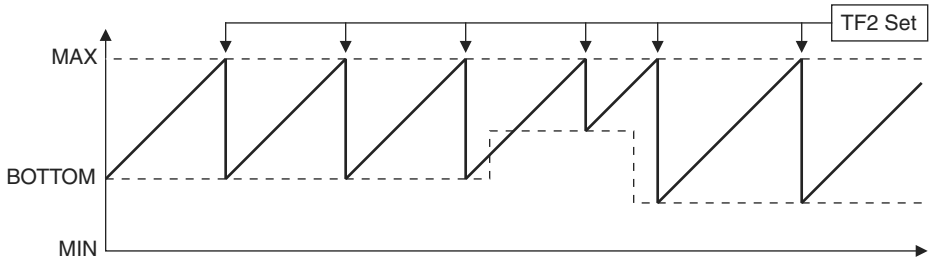


Figure 12-3. Timer 2 Waveform: Auto-Reload Mode (DCEN = 0)

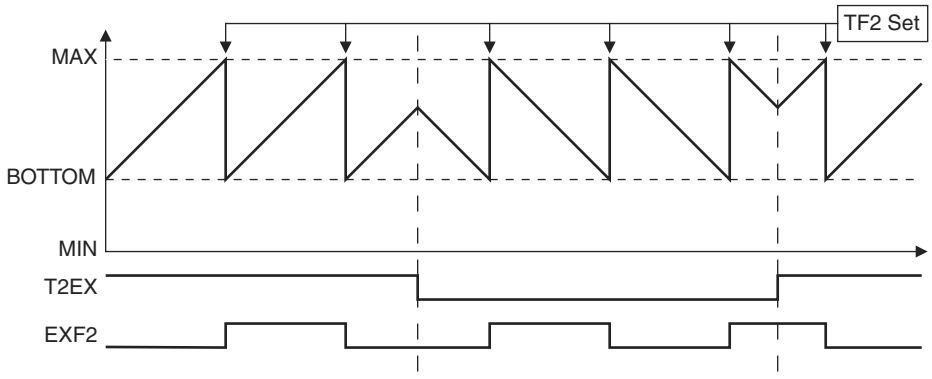


12.3.2 Up or Down Counter

Setting DCEN = 1 enables Timer 2 to count up or down, as shown in Figure 12-5. In this mode, the T2EX pin controls the direction of the count (if EXEN2 = 1). A logic 1 at T2EX makes Timer 2 count up. When $T2CM_{1-0}$ = 00B, the timer will overflow at MAX and set the TF2 bit. This overflow also causes BOTTOM, the 16-bit value in RCAP2H and RCAP2L, to be reloaded into the timer registers, TH2 and TL2, respectively. A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal BOTTOM, the 16-bit value stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes MAX to be reloaded into the timer registers. The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

The behavior of Timer 2 when DCEN is enabled is shown in Figure 12-4.

Figure 12-4. Timer 2 Waveform: Auto-Reload Mode (DCEN = 1)



state of the clock when not currently transmitting/receiving. The SMOD1 bit determines if the output data is stable for both edges of the clock, or just one.

Table 14-5. Mode 0 Clock and Data Modes

SM2	SMOD1	Clock Idle	Data Changes	Data Sampled
0	0	High	While clock is high	Positive edge of clock
0	1	High	Negative edge of clock	Positive edge of clock
1	0	Low	While clock is low	Negative edge of clock
1	1	Low	Negative edge of clock	Positive edge of clock

In Two-Wire configuration Mode 0 may be used as a hardware accelerator for software emulation of serial interfaces such as a half-duplex Serial Peripheral Interface (SPI) master in mode (0,0) or (1,1) or a Two-Wire Interface (TWI) in master mode. An example of Mode 0 emulating a TWI master device is shown in Figure 14-2. In this example, the start, stop, and acknowledge are handled in software while the byte transmission is done in hardware. Falling/rising edges on TXD are created by setting/clearing SM2. Rising/falling edges on RXD are forced by setting/clearing the P3.0 register bit. SM2 and P3.0 must be 1 while the byte is being transferred.

Figure 14-1. Mode 0 Waveforms (Two-Wire)

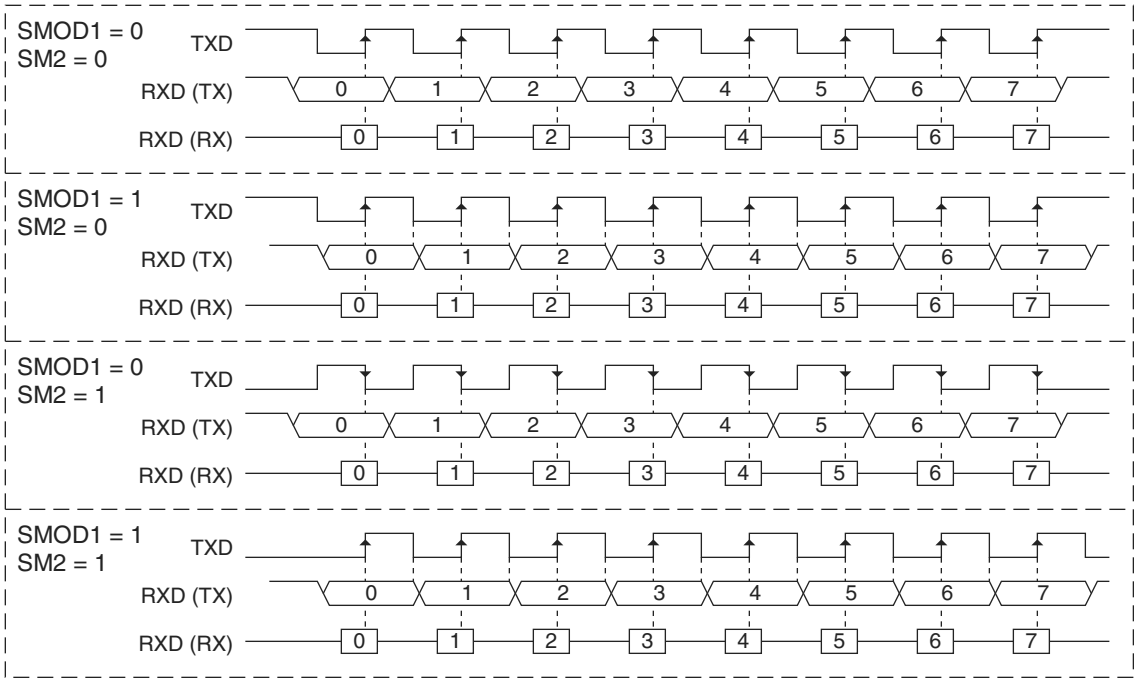


Figure 14-2. UART Mode 0 TWI Emulation (SMOD1 = 1)

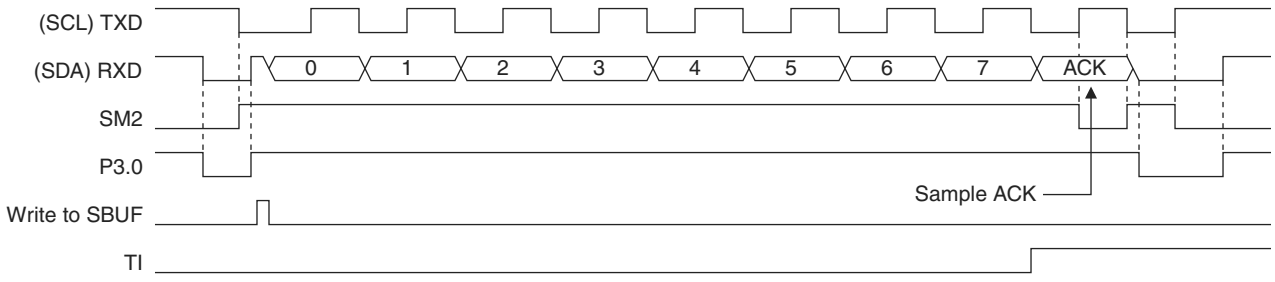
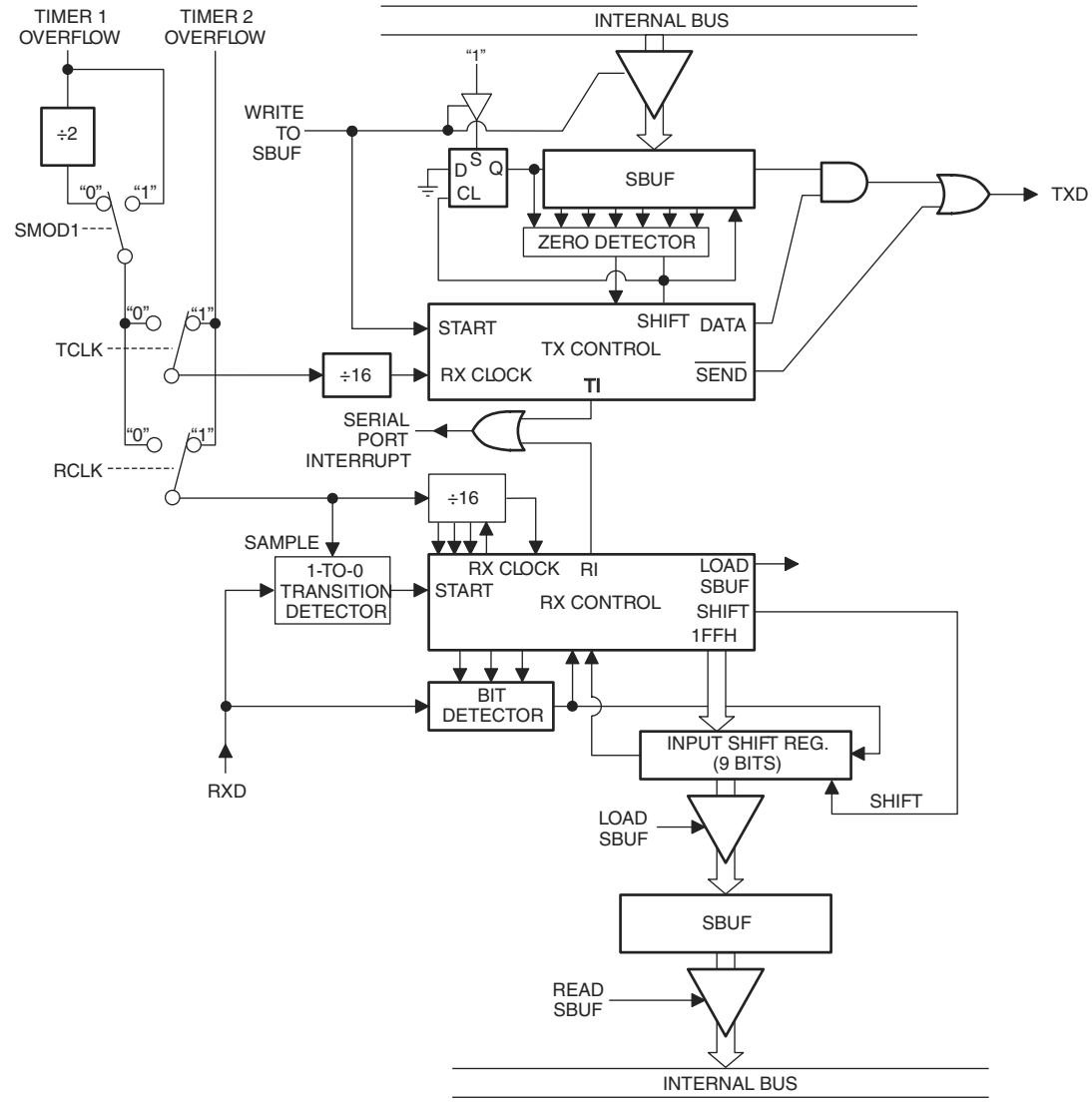


Figure 14-6. Serial Port Mode 1



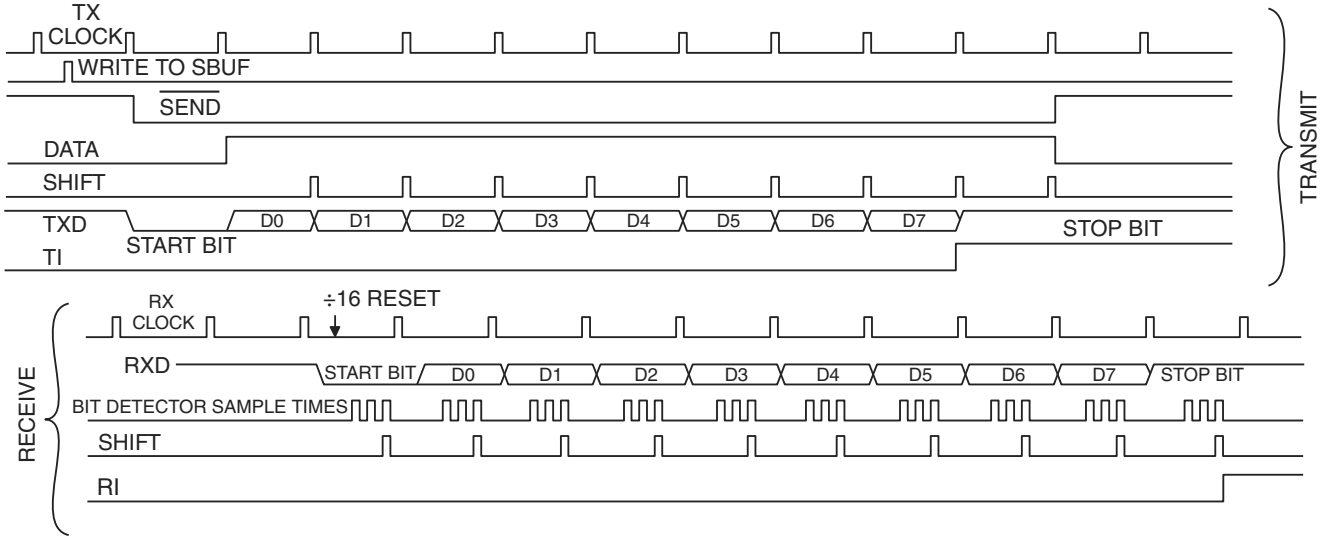


Table 16-1. Instruction Execution Times and Exceptions[1] (Continued)

ORL C, bit	2	12	2	72
ORL C, /bit	2	12	2	A0
MOV C, bit	2	6	2	A2
MOV bit, C	2	12	2	92
		Clock Cycles		
Branching	**Bytes**	**Compatibility**	**Fast**	**Hex Code**
JC rel	2	12	3	40
JNC rel	2	12	3	50
JB bit, rel	3	12	4	20
JNB bit, rel	3	12	4	30
JBC bit, rel	3	12	4	10
JZ rel	2	12	3	60
JNZ rel	2	12	3	70
SJMP rel	2	12	3	80
ACALL addr11	2	12	3	11,31,51,71,91, B1,D1,F1
LCALL addr16	3	12	4	12
RET	1	12	4	22
RETI	1	12	4	32
AJMP addr11	2	12	3	01,21,41,61,81, A1,C1,E1
LJMP addr16	3	12	4	02
JMP @A+DPTR	1	12	2	73
JMP @A+PC[2]	2	12	3	A5 73
CJNE A, direct, rel	3	12	4	B5
CJNE A, #data, rel	3	12	4	B4
CJNE Rn, #data, rel	3	12	4	B8-BF
CJNE @Ri, #data, rel	3	12	4	B6-B7
CJNE A, @R0, rel[2]	3	18	4	A5 B6
CJNE A, @R1, rel[2]	3	18	4	A5 B7
DJNZ Rn, rel	2	12	3	D8-DF
DJNZ direct, rel	3	12	4	D5
NOP	1	6	1	00

Notes:
1. A clock cycle is one period of the output of the system clock divider. For Fast mode the divider defaults to 1, so the clock cycle equals the oscillator period. For Compatibility mode the divider defaults to 2, so the clock cycle is twice the oscillator period, or conversely the clock count is half the number of oscillator periods.
2. This escaped instruction is an extension to the instruction set.
3. This is the minimum time for MOVX with no wait states. In Compatibility mode an additional 24 clocks are added for the wait state. In Fast mode, 1 clock is added for each wait state (0–3).

17. Programming the Flash Memory

The Atmel AT89LP51/52 microcontroller features 8K bytes of on-chip In-System Programmable Flash program memory and 256bytes of nonvolatile Flash data memory. In-System Programming allows programming and reprogramming of the microcontroller positioned inside the end system. Using a simple 3-wire SPI interface, the programmer communicates serially with the AT89LP51/52 microcontroller, reprogramming all nonvolatile memories on the chip. In-System Programming eliminates the need for physical removal of the chips from the system. This will save time and money, both during development in the lab, and when updating the software or parameters in the field. The programming interface of the AT89LP51/52 includes the following features:

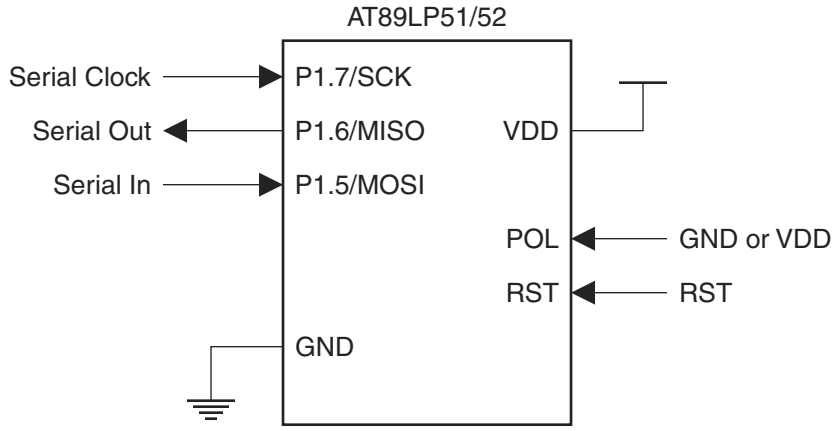
- Three-wire serial SPI Programming Interface or 11-pin Parallel Interface
- Selectable Polarity Reset Entry into Programming
- User Signature Array
- Flexible Page Programming
- Row Erase Capability
- Page Write with Auto-Erase Commands
- Programming Status Register

For more detailed information on In-System Programming, refer to the Application Note entitled “AT89LP In-System Programming Specification”.

17.1 Physical Interface

The AT89LP51/52 provides a standard programming command set with two physical interfaces: a bit-serial and a byte-parallel interface. Normal Flash programming utilizes the Serial Peripheral Interface (SPI) pins of an AT89LP51/52 microcontroller. The SPI is a full-duplex synchronous serial interface consisting of three wires: Serial Clock (SCK), Master-In/Slave-out (MISO), and Master-out/Slave-in (MOSI)). When programming an AT89LP51/52 device, the programmer always operates as the SPI master, and the target system always operates as the SPI slave. To enter or remain in Programming mode the device’s reset line (RST) must be held active. With the addition of VDD and GND, an AT89LP51/52 microcontroller can be programmed with a minimum of seven connections as shown in Figure 17-1.

Figure 17-1. In-System Programming Device Connections



17.3 Command Format

Programming commands consist of an opcode byte, two address bytes, and one or 64 data bytes. Figure 17-4 on page 82 shows a simplified flow chart of a command sequence.

A sample command packet is shown in Figure 17-5 on page 83. The packet does not use a chip select. Command bytes are issued serially on MOSI. Data output bytes are received serially on MISO. The command is not complete until all bytes have been transfered, including any don't care bytes.

Page oriented instructions always include a full 16-bit address. The higher order bits select the page and the lower order bits select the byte within that page. The AT89LP51/52 allocates 6 bits for byte address, 1 bit for low/high half page selection and 9 bits for page address. The half page to be accessed is always fixed by the page address and half select as transmitted. The byte address specifies the starting address for the first data byte. After each data byte has been transmitted, the byte address is incremented to point to the next data byte. This allows a page command to linearly sweep the bytes within a page. If the byte address is incremented past the last byte in the half page, the byte address will roll over to the first byte in the same half page. While loading bytes into the page buffer, overwriting previously loaded bytes will result in data corruption.

For a summary of available commands, see Table 17-2 on page 84.

Figure 17-4. Command Sequence Flow Chart

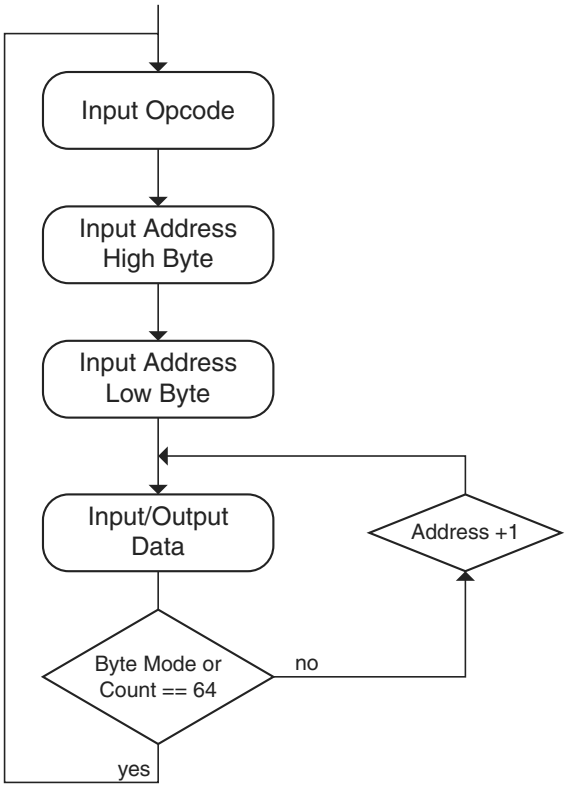


Figure 17-5. ISP Command Packet (Serial Byte)

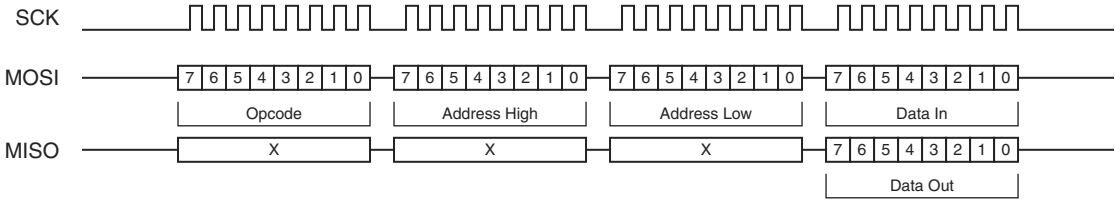


Figure 17-6. ISP Command Packet (Serial Page)

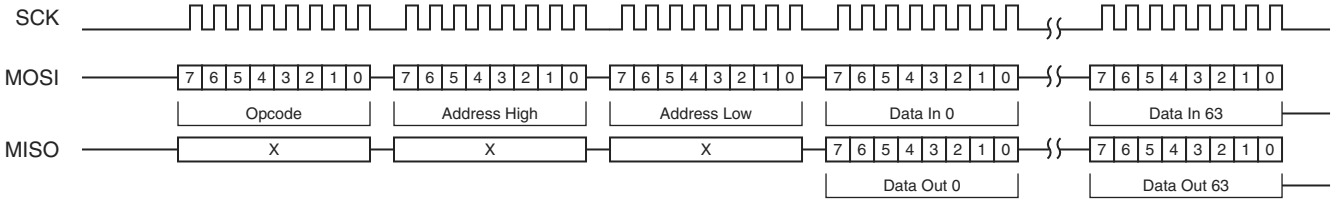


Figure 17-7. ISP Command Packet (Parallel Byte)

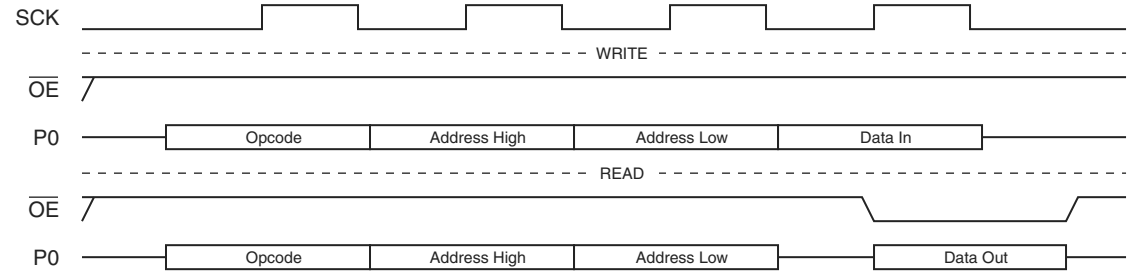


Figure 17-8. ISP Command Packet (Parparallel Page)

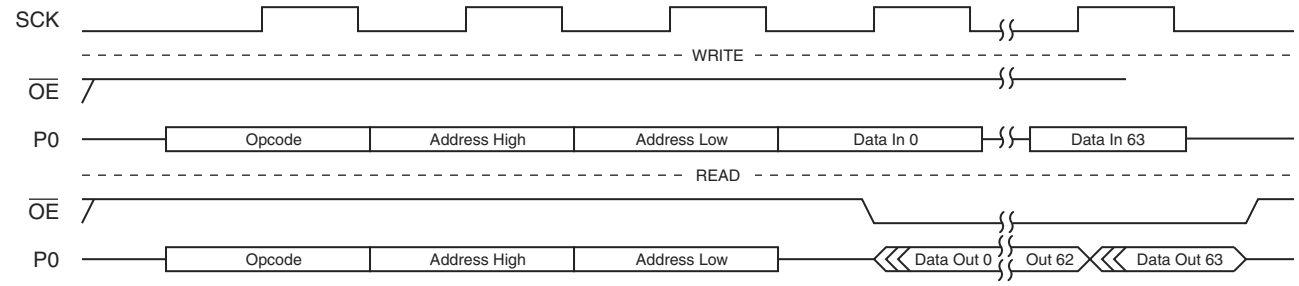
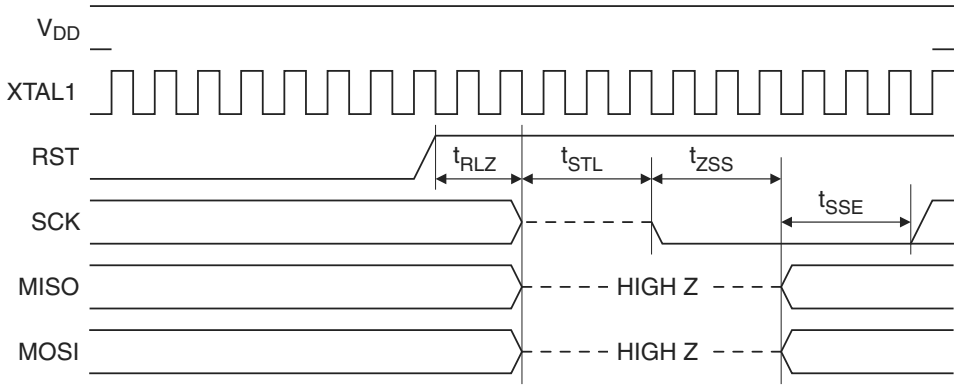


Figure 17-11. In-System Programming (ISP) Start Sequence

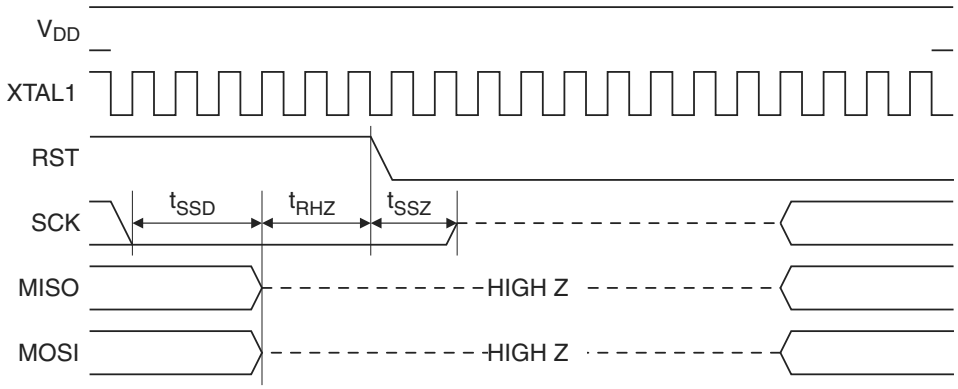


17.9.4 ISP Exit Sequence

Execute this sequence to exit ISP mode and resume CPU execution mode.

1. Drive SCK low.
1. Wait at least t_{SSD}.
2. Tristate MOSI.
3. Wait at least t_{RHZ} and bring RST low.
4. Wait t_{SSZ} and tristate SCK.

Figure 17-12. In-System Programming (ISP) Exit Sequence



Note: The waveforms on this page are not to scale.

17.9.5 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is a byte-oriented full-duplex synchronous serial communication channel. During In-System Programming, the programmer always acts as the SPI master and the target device always acts as the SPI slave. The target device receives serial data on MOSI and outputs serial data on MISO. The Programming Interface implements a standard SPI Port with a fixed data order and For In-System Programming, bytes are transferred MSB first as shown in Figure 17-13. The SCK phase and polarity follow SPI clock mode 0 (CPOL = 0, CPHA = 0) where bits are sampled on the rising edge of SCK and output on the falling edge of SCK. For more detailed timing information see Figure 17-14.

18.3.2 Supply Current (External Clock)

Figure 18-3. Active Supply Current vs. Frequency

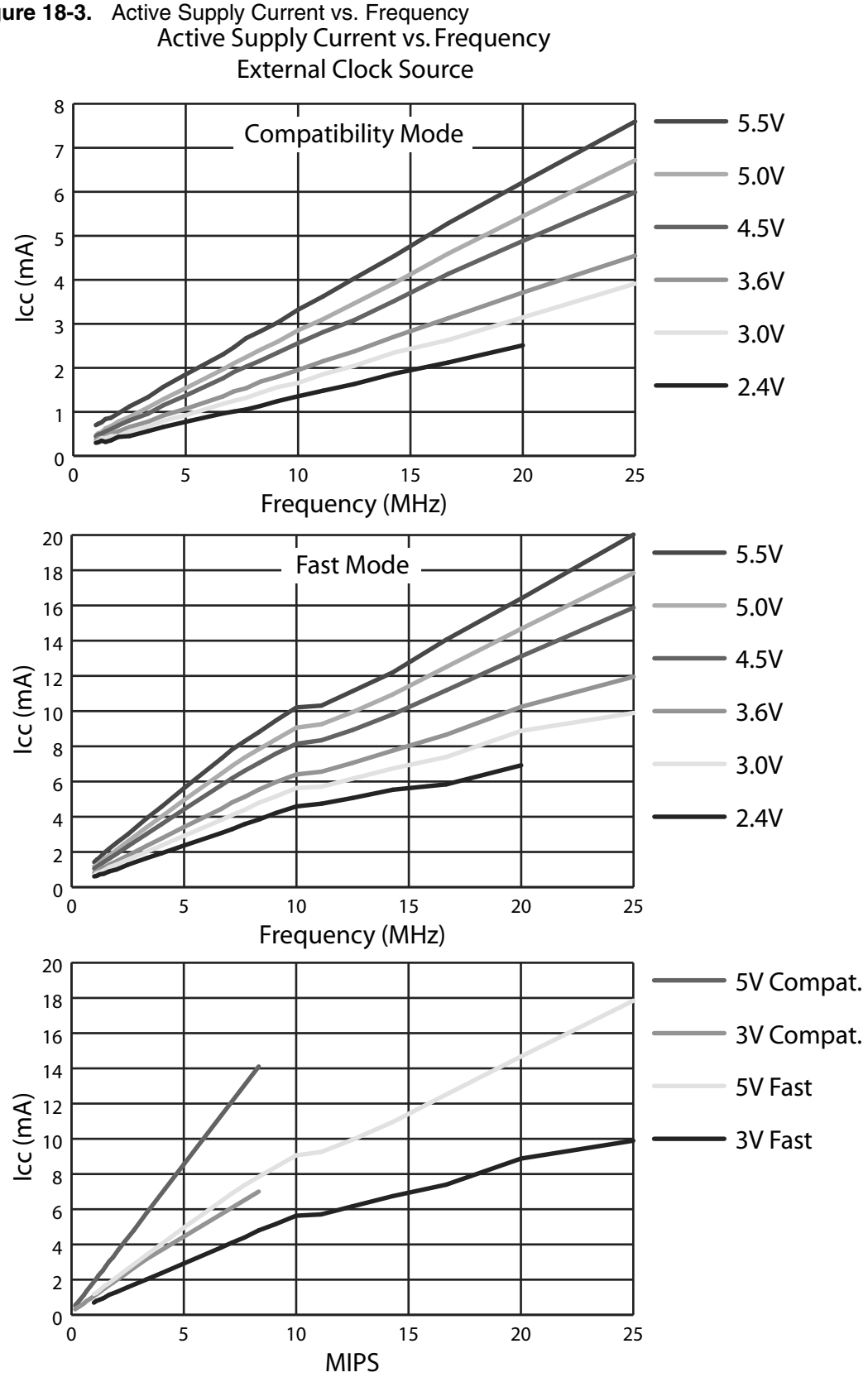


Figure 18-14. External Program Memory Read Cycle

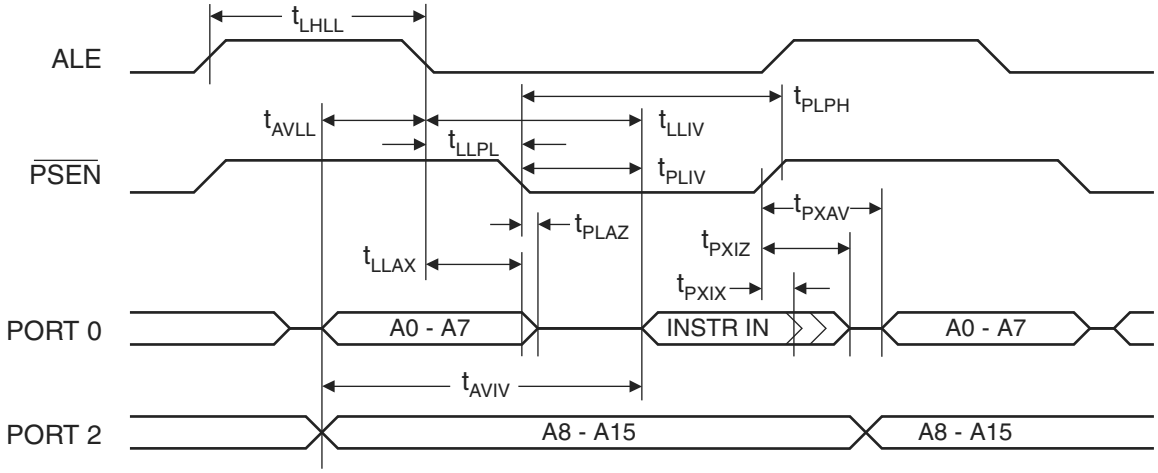


Figure 18-15. External Data Memory Read Cycle

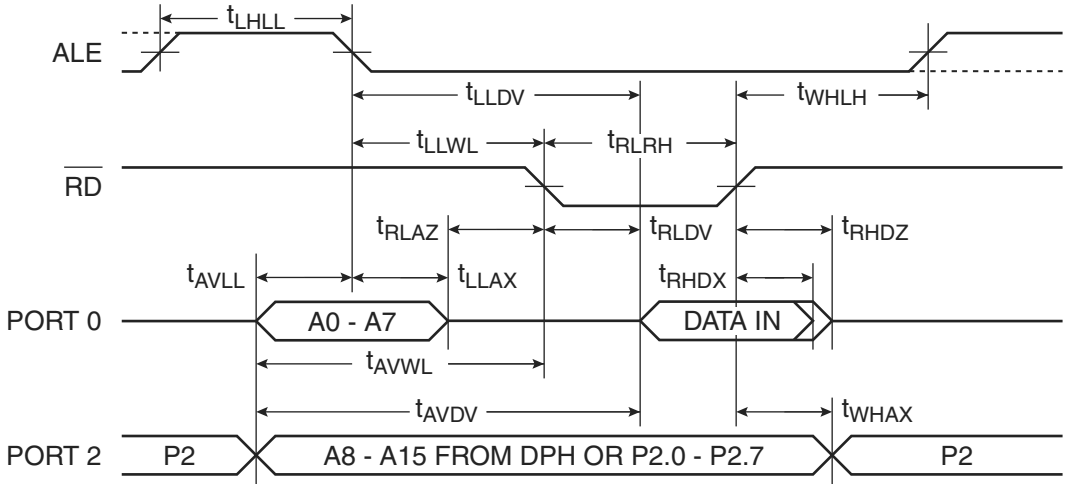
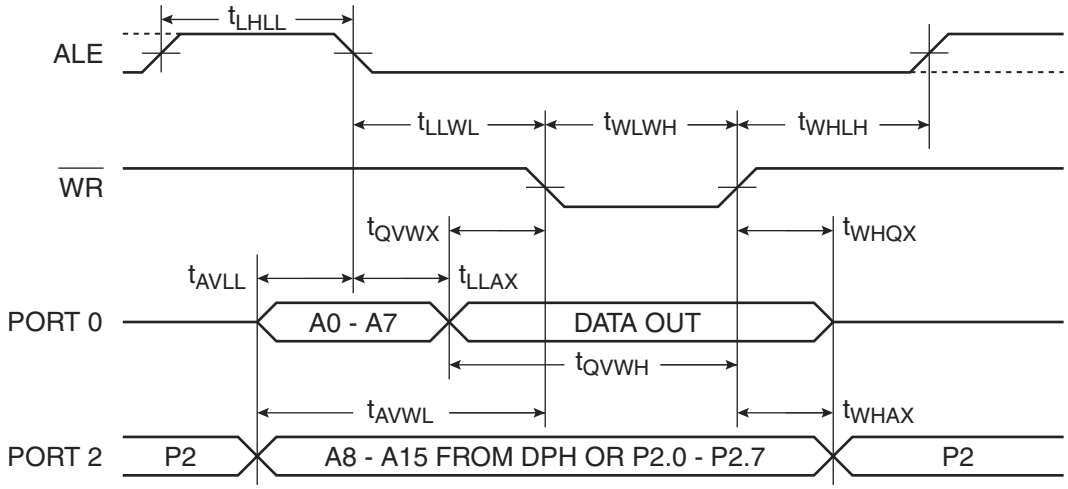


Figure 18-16. External Data Memory Write Cycle



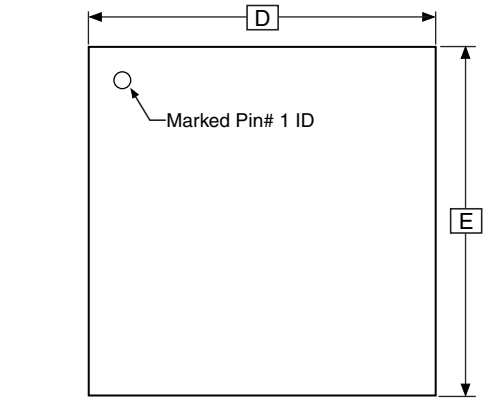
19. Ordering Information

19.1 Green Package Option (Pb/Halide-free)

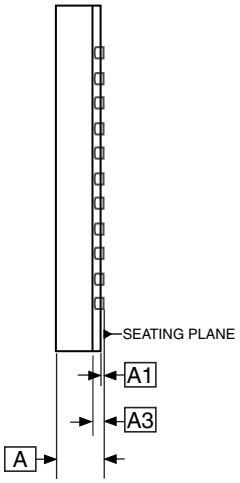
Speed (MHz)	Power Supply	Code Memory	Ordering Code	Package	Operation Range
20	2.4V to 5.5V	4KB	AT89LP51-20AU AT89LP51-20PU AT89LP51-20JU AT89LP51-20MU	44A 40P6 44J 44M1	Industrial (-40° C to 85° C)
20	2.4V to 5.5V	8KB	AT89LP52-20AU AT89LP52-20PU AT89LP52-20JU AT89LP52-20MU	44A 40P6 44J 44M1	Industrial (-40° C to 85° C)

Package Types	
44A	44-lead, Thin Plastic Quad Flat Package (TQFP)
40P6	40-lead, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
44M1	44-pad, 7 x 7 x 1.0 mm Body, Plastic Very Thin Quad Flat No Lead Package (VQFN/MLF)

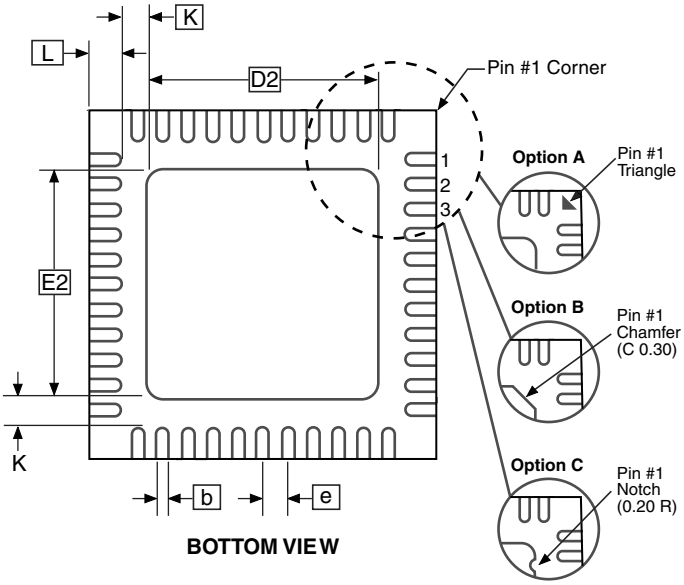
20.4 44M1 – VQFN/MLF



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

9/26/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	44M1, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)	ZWS	44M1	H