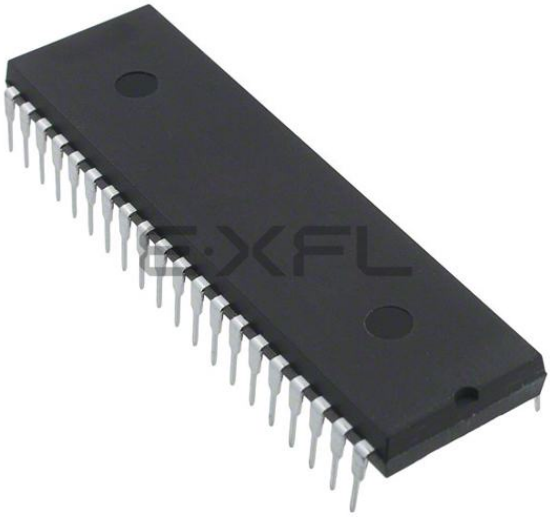

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp52-20pu

Table 2-3. Compatibility Mode versus Fast Mode Summary

Feature	Compatibility	Fast
Pin Sampling Rate ($\overline{INT0}$, $\overline{INT1}$, T0, T1, T2, T2EX)	Prescaler Rate	System Clock
Minimum RST input pulse in System Clocks	12	2
WDIDLE and DISRTO bit locations	AUXR	WDTCON

3. Memory Organization

The AT89LP51/52 uses a Harvard Architecture with separate address spaces for program and data memory. The program memory has a regular linear address space with support for 64K bytes of directly addressable application code. The data memory has 256 bytes of internal RAM and 128 bytes of Special Function Register I/O space. The AT89LP51/52 supports up to 64K bytes of external data memory, with portions of the external data memory space implemented on chip as nonvolatile Flash data memory. External program memory is supported for addresses above 8K. The memory address spaces of the AT89LP51/52 are listed in Table 3-1.

Table 3-1. AT89LP51/52 Memory Address Spaces

Name	Description	Range
DATA	Directly addressable internal RAM	00H–7FH
IDATA	Indirectly addressable internal RAM and stack space	00H–FFH
SFR	Directly addressable I/O register space	80H–FFH
FDATA	On-chip nonvolatile Flash data memory	0000H–00FFH
XDATA	External data memory	0100H–FFFFH
CODE	On-chip nonvolatile Flash program memory	0000H–0FFFH (AT89LP51) 0000H–1FFFH (AT89LP52)
XCODE	External program memory	2000H–FFFFH (AT89LP51) 1000H–FFFFH (AT89LP52)
SIG	On-chip nonvolatile Flash signature array	0000H–01FFH

3.1 Program Memory

The AT89LP51/52 contains 4K/8K bytes of on-chip In-System Programmable Flash memory for program storage, plus support for up to 60K/56K bytes of external program memory. The Flash memory has an endurance of at least 10,000 write/erase cycles and a minimum data retention time of 10 years. The reset and interrupt vectors are located within the first 83 bytes of program memory (refer to Table 9-1 on page 38). Constant tables can be allocated within the entire 64K program memory address space for access by the MOVC instruction. A map of the AT89LP51/52 program memory is shown in Figure 3-1.

Figure 3-10. External Data Memory 16-bit Linear Address Mode

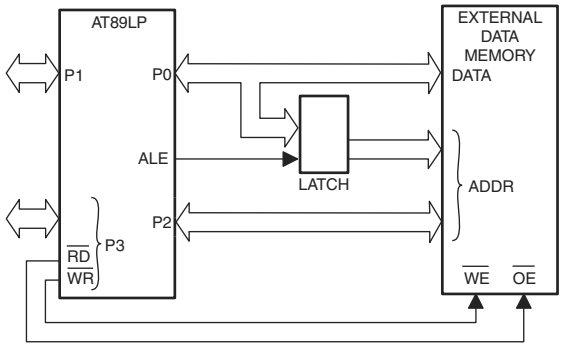
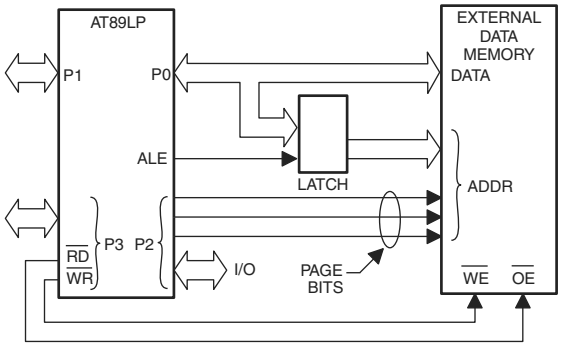


Figure 3-11 shows a hardware configuration for accessing 256-byte blocks of external RAM using an 8-bit paged address. Port 0 serves as a multiplexed address/data bus to the RAM. The ALE strobe is used to latch the address byte into an external register so that Port 0 can be freed for data input/output. The Port 2 I/O lines (or other ports) can provide control lines to page the memory; however, this operation is not handled automatically by hardware. The software application must change the Port 2 register when appropriate to access different pages. The MOVX @Ri instructions use Paged Address mode.

Figure 3-11. External Data Memory 8-bit Paged Address Mode



Note that prior to using the external memory interface, $\overline{WR}$ (P3.6) and $\overline{RD}$ (P3.7) must be configured as outputs. See Section 10.1 “Port Configuration” on page 41. P0 and P2 are configured automatically to push-pull output mode when outputting address or data and P0 is automatically tristated when inputting data regardless of the port configuration. The Port 0 configuration will determine the idle state of Port 0 when not accessing the external memory.

Figure 3-12 and Figure 3-13 show examples of external data memory write and read cycles, respectively. The address on P0 and P2 is stable at the falling edge of ALE. The idle state of ALE is controlled by DISALE (AUXR.0). When DISALE = 0 the ALE toggles at a constant rate when not accessing external memory. When DISALE = 1 the ALE is weakly pulled high. DISALE must be one in order to use P4.4 as a general-purpose I/O. The WS bits in AUXR can extended the $\overline{RD}$ and $\overline{WR}$ strobes by 1, 2 or 3 cycles as shown in Figures 3-16, 3-17 and 3-18. If a longer strobe is required, the application can scale the system clock with the clock divider to meet the requirements (See Section 6.4 on page 31).

Figure 3-16. MOVX with One Wait State (WS = 01B)

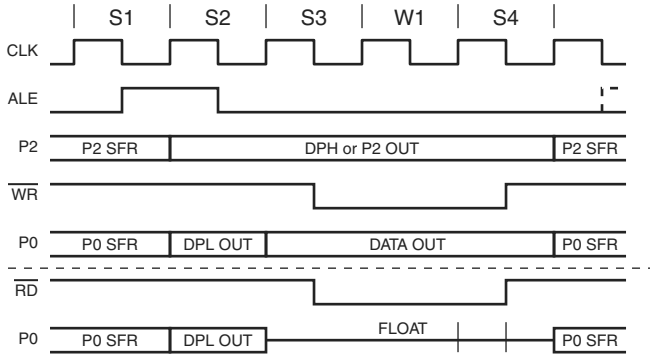


Figure 3-17. MOVX with Two Wait States (WS = 10B)

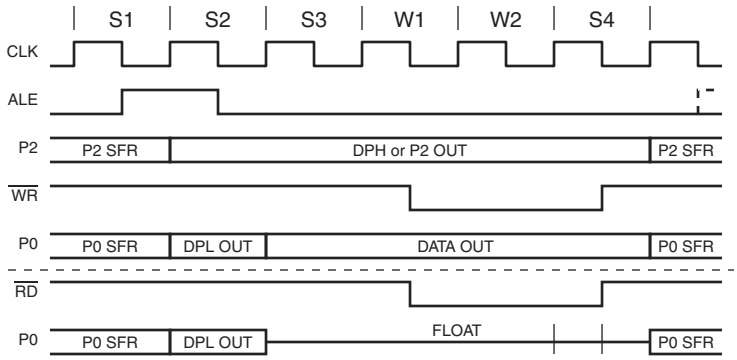
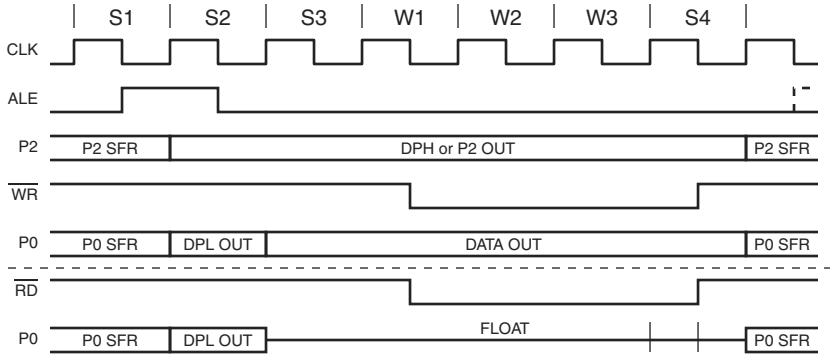


Figure 3-18. MOVX with Three Wait States (WS = 11B)



instruction is 5 cycles long. If the instruction in progress is RETI, the additional wait time cannot be more than 9 cycles (a maximum of 4 more cycles to complete the instruction in progress, plus a maximum of 5 cycles to complete the next instruction). Thus, in a single-interrupt system, the response time is always more than 5 clock cycles and less than 14 clock cycles. See Figure 9-1 and Figure 9-2.

Figure 9-1. Minimum Interrupt Response Time (Fast Mode)

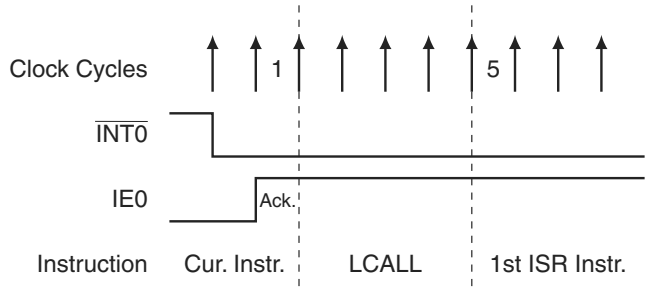


Figure 9-2. Maximum Interrupt Response Time (Fast Mode)

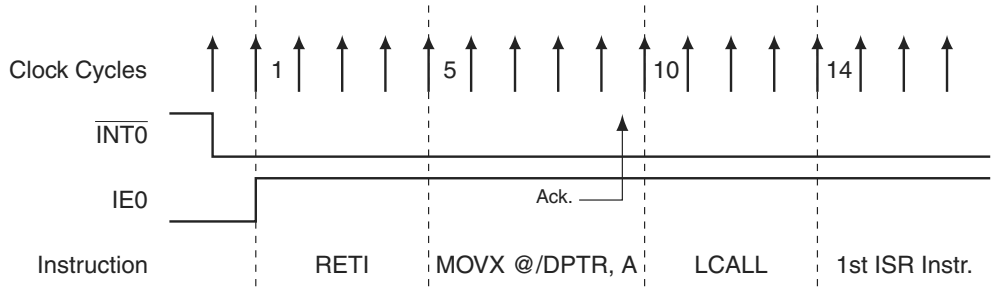


Figure 9-3. Minimum Interrupt Response Time (Compatibility Mode)

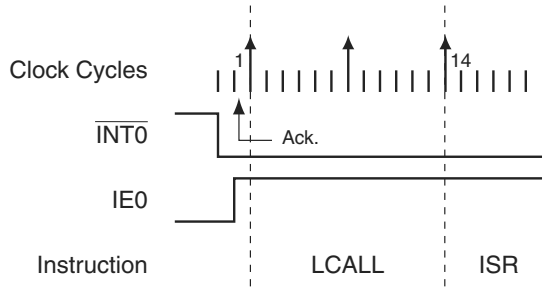
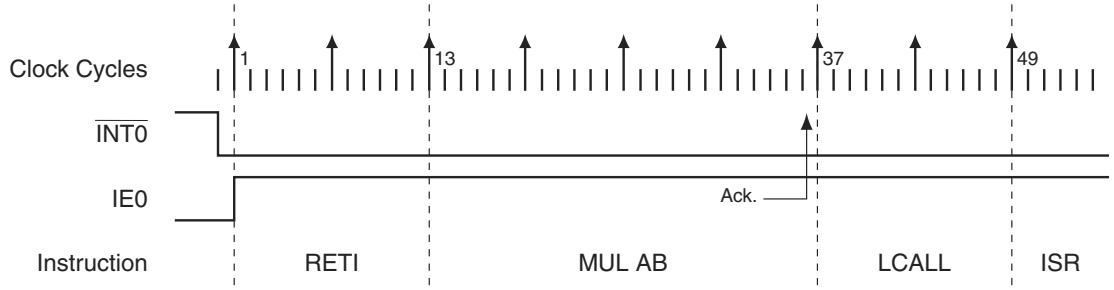


Figure 9-4. Maximum Interrupt Response Time (Compatibility Mode)



11. Timer 0 and Timer 1

The AT89LP51/52 has two 16-bit Timer/Counters, Timer 0 and Timer 1, with the following features:

- Two independent 16-bit timer/counters with 8-bit reload registers
- UART baud rate generation using Timer 1
- Output pin toggle on timer overflow
- Split timer mode allows for three separate timers (2 8-bit, 1 16-bit)
- Gated modes allow timers to run/halt based on an external input

Timer 0 and Timer 1 have similar modes of operation. As timers, the timer registers normally increase every clock cycle. Thus, the registers count clock cycles. The timer rate can be prescaled by a value between 1 and 16 using the Timer Prescaler (see Table 6-2 on page 31). Both Timers share the same prescaler. In Compatibility mode CDV defaults to 2, so a clock cycle consists of two oscillator periods,and the prescaler defaults to 6 making the count rate equal to 1/12 of the oscillator frequency. By default in Fast mode CDV = 0 and TPS = 0 so the count rate is equal to the oscillator frequency.

As counters, the timer registers are incremented in response to a 1-to-0 transition at the corresponding input pins, T0 or T1. In Fast mode the external input is sampled every clock cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since 2 clock cycles are required to recognize a 1-to-0 transition, the maximum count rate is 1/2 of the system frequency. There are no restrictions on the duty cycle of the input signal, but it should be held for at least one full clock cycle to ensure that a given level is sampled at least once before it changes.

In Compatibility mode the counter input sampling is controlled by the prescaler. Since TPS defaults to 6 in this mode, the pins are sampled every six system clocks. Therefore the input signal should be held for at least six clock cycles to ensure that a given level is sampled at least once before it changes.

Furthermore, the Timer or Counter functions for Timer 0 and Timer 1 have four operating modes: 13-bit timer, 16-bit timer, 8-bit auto-reload timer, and split timer. The control bits C/T in the Special Function Register TMOD select the Timer or Counter function. The bit pairs (M1, M0) in TMOD select the operating modes.

Table 11-1. Timer 0/1 Register Summary

Name	Address	Purpose	Bit-Addressable
TCON	88H	Control	Y
TMOD	89H	Mode	N
TL0	8AH	Timer 0 low-byte	N
TL1	8BH	Timer 1 low-byte	N
TH0	8CH	Timer 0 high-byte	N
TH1	8DH	Timer 1 high-byte	N
TCONB	91H	Mode	N

Figure 11-5. Timer 0/1 Toggle Mode 2 Waveform

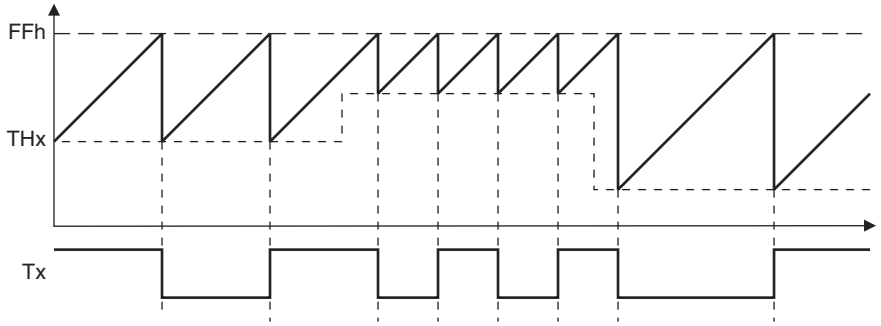


Table 11-4. TMOD – Timer/Counter Mode Control Register

TMOD Address = 089H — Reset Value = 0000 0000B

Not Bit Addressable

	GATE1	C/$\overline{T1}$	T1M1	T1M0	GATE0	C/$\overline{T0}$	T0M0	T0M1
Bit	7	6	5	4	3	2	1	0

Symbol	Function
GATE1	Timer 1 Gating Control. When set, Timer/Counter 1 is enabled only while $\overline{INT1}$ pin is high and TR1 control pin is set. When cleared, Timer 1 is enabled whenever TR1 control bit is set.
C/$\overline{T1}$	Timer or Counter Selector 1. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from T1 input pin). C/$\overline{T1}$ must be zero when using Timer 1 in Clock Out mode.
T1M1 T1M0	Timer 1 Operating Mode **Mode** / **T1M1** / **T1M0** / **Operation** 0 / 0 / 0 / 13-bit Timer Mode. 8-bit Timer/Counter TH1 with TL1 as 5-bit prescaler. 1 / 0 / 1 / 16-bit Timer Mode. TH1 and TL1 are cascaded to form a 16-bit Timer/Counter. 2 / 1 / 0 / 8-bit Auto Reload Mode. TH1 holds a value which is reloaded into 8-bit Timer/Counter TL1 each time it overflows. 3 / 1 / 1 / Timer/Counter 1 is stopped
GATE0	Timer 0 Gating Control. When set, Timer/Counter 0 is enabled only while $\overline{INT0}$ pin is high and TR0 control pin is set. When cleared, Timer 0 is enabled whenever TR0 control bit is set.
C/$\overline{T0}$	Timer or Counter Selector 0. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from T0 input pin). C/$\overline{T0}$ must be zero when using Timer 0 in Clock Out mode.
T0M1 T0M0	Timer 0 Operating Mode **Mode** / **T0M1** / **T0M0** / **Operation** 0 / 0 / 0 / 13-bit Timer Mode. 8-bit Timer/Counter TH0 with TL0 as 5-bit prescaler. 1 / 0 / 1 / 16-bit Timer Mode. TH0 and TL0 are cascaded to form a 16-bit Timer/Counter. 2 / 1 / 0 / 8-bit Auto Reload Mode. TH0 holds a value which is reloaded into 8-bit Timer/Counter TL0 each time it overflows. 3 / 1 / 1 / Split Timer Mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.

The Timer 1 overflow rate normally determines the baud rates in Modes 1 and 3. When Timer 1 is the baud rate generator, the baud rates are determined by the Timer 1 overflow rate and the value of SMOD1 according to the following equation:

$$\frac{\text{Modes 1, 3}}{\text{Baud Rate}} = \frac{2^{\text{SMOD1}}}{32} \times \text{(Timer 1 Overflow Rate)}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either timer or counter operation in any of its 3 running modes. In the most typical applications, it is configured for timer operation in auto-reload mode (high nibble of TMOD = 0010B). In this case, the baud rate is given by the following formula:

$$\frac{\text{Modes 1, 3}}{\text{Baud Rate}} = \frac{2^{\text{SMOD1}}}{32} \times \frac{\text{System Frequency}}{[256 - (\text{TH1})]} \times \frac{1}{\text{TPS} + 1}$$

Table 14-2 lists commonly used baud rates and how they can be obtained from Timer 1.

Table 14-2. Commonly Used Baud Rates Generated by Timer 1

				Timer 1			
Baud Rate	**f_{osc} (MHz)**	**CDV**	**SMOD1**	**C/$\overline{T}$**	**Mode**	**TPS**	**Reload Value**
Mode 0 Max: 6 MHz	12	0	1	X	X	0	X
Mode 2 Max: 750K	12	0	1	X	X	0	X
Modes 1, 3 Max: 750K	12	0	1	0	2	0	F4H
19.2K	11.059	0	1	0	2	0	DCH
9.6K	11.059	0	0	0	2	0	DCH
4.8K	11.059	0	0	0	2	0	B8H
2.4K	11.059	0	0	0	2	0	70H
1.2K	11.059	0	0	0	1	0	FEE0H
137.5	11.986	0	0	0	1	0	F55CH
110	6	0	1	0	1	0	F2AFH
110	12	0	0	0	1	0	F2AFH
19.2K	11.059	1	1	0	2	5	FDH
9.6K	11.059	1	0	0	2	5	FDH
4.8K	11.059	1	0	0	2	5	FAH
2.4K	11.059	1	0	0	2	5	F4H
1.2K	11.059	1	0	0	2	5	E8H
137.5	11.986	1	0	0	2	5	1DH
110	6	1	0	0	2	5	72H
110	12	1	0	0	1	5	FEEBH

14.2.2 Using Timer 2 to Generate Baud Rates

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON. Under these conditions, the baud rates for transmit and receive can be simultaneously different by using Timer 1 for transmit and Timer 2 for receive, or vice versa. The baud rate generator mode

is similar to the auto-reload mode, in that a rollover causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software. In this case, the baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation:

$$\text{Modes 1 and 3 Baud Rate} = \frac{1}{16} \times \frac{\text{System Frequency}}{[65536 - (\text{RCAP2H,RCAP2L})]}$$

Table 14-3 lists commonly used baud rates and how they can be obtained from Timer 2.

Table 14-3. Commonly Used Baud Rates Generated by Timer 2

Baud Rate	f_{osc} (MHz)	CDV	Timer 2			
			CP/$\overline{RL2}$	C/$\overline{T2}$	TCLK or RCLK	Reload Value
Max: 750K	12	0	0	0	1	FFFFH
19.2K	11.059	0	0	0	1	FFDCH
9.6K	11.059	0	0	0	1	FFB8H
4.8K	11.059	0	0	0	1	FF70H
2.4K	11.059	0	0	0	1	FEE0H
1.2K	11.059	0	0	0	1	FDC0H
137.5	11.986	0	0	0	1	EAB8H
110	6	0	0	0	1	F2AFH
110	12	0	0	0	1	E55EH
19.2K	11.059	1	0	0	1	FFEEH
9.6K	11.059	1	0	0	1	FFDCH
4.8K	11.059	1	0	0	1	FFB8H
2.4K	11.059	1	0	0	1	FF70H
1.2K	11.059	1	0	0	1	FEE0H
137.5	11.986	1	0	0	1	F55CH
110	12	1	0	0	1	F2AFH

14.3 Framing Error Detection

In addition to all of its usual modes, the UART can perform framing error detection by looking for missing stop bits, and automatic address recognition. When used for framing error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software. The FE bit will be set by a framing error regardless of the state of SMOD0.

14.4 Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON for Modes 1, 2 or 3. In the 9-bit UART modes, Mode 2 and Mode 3, the Receive

The Broadcast Address for each slave is created by taking the logic OR of SADDR and SADEN. Zeros in this result are trended as don't cares. In most cases, interpreting the don't cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with "0"s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

14.5 More About Mode 0

In Mode 0, the UART is configured as either a two wire half-duplex or three wire full-duplex synchronous serial interface. In two-wire mode serial data enters and exits through RXD and TXD outputs the shift clock. In three-wire mode serial data enters through MISO, exits through MOSI and SCK outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. Figure 14-3 and Figure 14-5 on page 67 show simplified functional diagrams of the serial port in Mode 0 and associated timing. The baud rate is programmable to 1/2 or 1/4 the system frequency by setting/clearing the SMOD1 bit in Fast mode, or 1/3 or 1/6 the system frequency in Compatibility mode. However, changing SMOD1 has an effect on the relationship between the clock and data as described below. The baud rate can also be generated by Timer 1 by setting TB8. Table 14-4 lists the baud rate options for Mode 0.

Table 14-4. Mode 0 Baud Rates

TB8	SMOD1	Baud Rate (Fast)	Baud Rate (Compatibility)
0	0	$f_{SYS}/4$	$f_{SYS}/6$
0	1	$f_{SYS}/2$	$f_{SYS}/3$
1	0	(Timer 1 Overflow) / 4	(Timer 1 Overflow) / 4
1	1	(Timer 1 Overflow) / 2	(Timer 1 Overflow) / 2

14.5.1 Two-Wire (Half-Duplex) Mode

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a "1" into the 9th position of the transmit shift register and tells the TX Control Block to begin a transmission. The internal timing is such that one full bit slot may elapse between "write to SBUF" and activation of SEND.

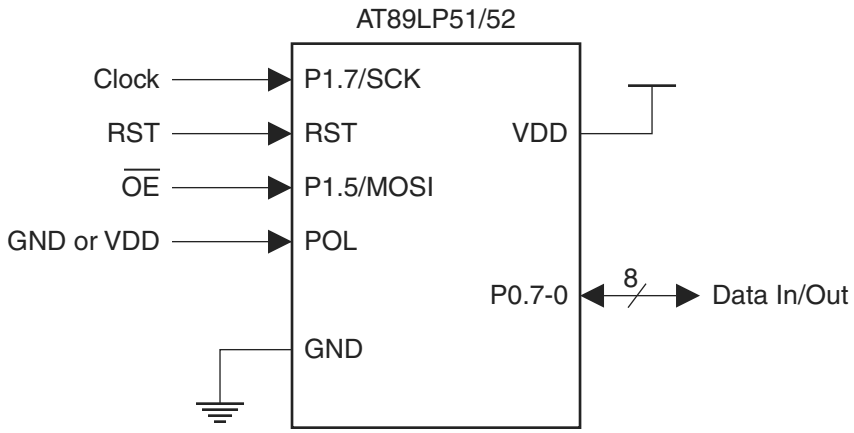
SEND transfers the output of the shift register to the alternate output function line of P3.0, and also transfers Shift Clock to the alternate output function line of P3.1. As data bits shift out to the right, "0"s come in from the left. When the MSB of the data byte is at the output position of the shift register, the "1" that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain "0"s. This condition flags the TX Control block to do one last shift, then deactivate SEND and set TI.

Reception is initiated by the condition REN = 1 and RI = 0. At the next clock cycle, the RX Control unit writes the bits 11111110B to the receive shift register and activates RECEIVE in the next clock phase. RECEIVE enables Shift Clock to the alternate output function line of P3.1. As data bits come in from the right, "1"s shift out to the left. When the "0" that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set.

The relationship between the shift clock and data is determined by the combination of the SM2 and SMOD1 bits as listed in Table 14-5 and shown in Figure . The SM2 bit determines the idle

The Parallel interface is a special mode of the serial interface, i.e. the serial interface is used to enable the parallel interface. After enabling the interface serially over P1.7/SCK and P1.5/MOSI, P1.5 is reconfigured as an active-low output enable ($\overline{OE}$) for data on Port 0. When $\overline{OE}$ = 1, command, address and write data bytes are input on Port 0 and sampled at the rising edge of SCK. When $\overline{OE}$ = 0, read data bytes are output on Port 0 and should be sampled on the falling edge of SCK. The P1.7/SCK and RST pins continue to function in the same manner. With the addition of VDD and GND, the parallel interface requires a minimum of fourteen connections as shown in Figure 17-2. Note that a connection to P1.6/MISO is not required for using the parallel interface.

Figure 17-2. Parallel Programming Device Connections

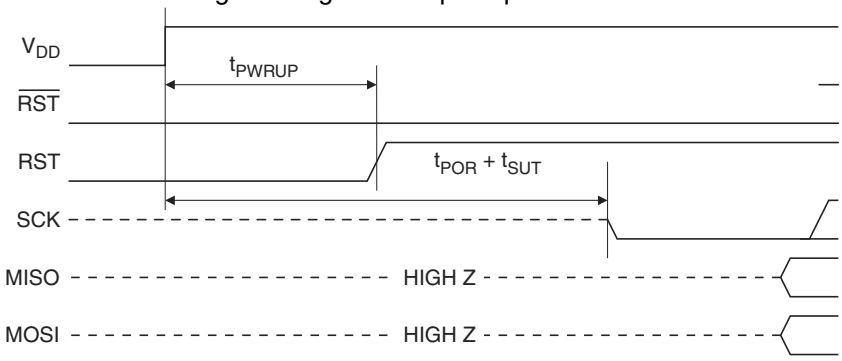


The Programming Interface is the only means of externally programming the AT89LP51/52 microcontroller. The Interface can be used to program the device both in-system and in a standalone serial programmer. The Interface does not require any clock other than SCK and is not limited by the system clock frequency. During Programming the system clock source of the target device can operate normally.

When designing a system where In-System Programming will be used, the following observations must be considered for correct operation:

- The ISP interface uses the SPI clock mode 0 (CPOL = 0, CPHA = 0) exclusively with a maximum frequency of 5 MHz.
- The AT89LP51/52 will enter programming mode only when its reset line (RST) is active. To simplify this operation, it is recommended that the target reset can be controlled by the In-System programmer. To avoid problems, the In-System programmer should be able to keep the entire target system reset for the duration of the programming cycle. The target system should never attempt to drive the three SPI lines while reset is active.
- The ISP Enable Fuse must be set to allow programming during any reset period. If the ISP Fuse is disabled, ISP may only be entered at POR. To enter programming the RST pin must be driven active prior to the end of Power-On Reset (POR). After POR has completed the device will remain in ISP mode until RST is brought inactive. Once the initial ISP session has ended, the power to the target device must be cycled OFF and ON to enter another session. Note that if this method is required, an active-low reset polarity is recommended.
- For standalone programmers, an active-low reset polarity is recommended (POL = 0). RST may then be tied directly to GND to ensure correct entry into Programming mode regardless of the device settings.

Figure 17-9. Serial Programming Power-up Sequence

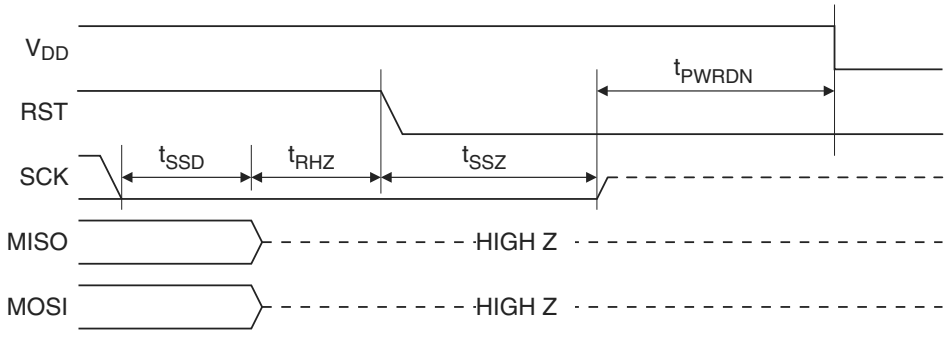


17.9.2 Power-down Sequence

Execute this sequence to power-down the device **after** programming.

1. Drive SCK low.
2. Wait at least t_{SSD} and Tristate MOSI.
3. Wait at least t_{RHZ} and drive RST low.
4. Wait at least t_{SSZ} and tristate SCK.
5. Wait no more than t_{PWRDN} and power off VDD.

Figure 17-10. Serial Programming Power-down Sequence



17.9.3 ISP Start Sequence

Execute this sequence to exit CPU execution mode and enter ISP mode when the device has passed Power-On Reset and is already operational.

1. Drive RST high.
2. Wait $t_{RLZ} + t_{STL}$.
3. Drive SCK low.
4. Start programming session.

17.9.6 Timing Parameters

The timing parameters for Figure 17-9, Figure 17-10, Figure 17-11, Figure 17-12, Figure 17-14 and Figure 17-15 are shown in Table .

Table 17-6. Programming Interface Timing Parameters

Symbol	Parameter	Min	Max	Units
t_{CLCL}	System Clock Cycle Time	0	60	ns
t_{PWRUP}	Power On to $\overline{SS}$ High Time	10		µs
t_{POR}	Power-on Reset Time		100	µs
t_{PWRDN}	$\overline{SS}$ Tristate to Power Off		1	µs
t_{RLZ}	RST Low to I/O Tristate	t_{CLCL}	2 t_{CLCL}	ns
t_{STL}	RST Low Settling Time	100		ns
t_{RHZ}	RST High to $\overline{SS}$ Tristate	0	2 t_{CLCL}	ns
t_{SCK}	Serial Clock Cycle Time	200[1]		ns
t_{SHSL}	Clock High Time	75		ns
t_{SLSH}	Clock Low Time	50		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns
t_{SIS}	Serial Input Setup Time	10		ns
t_{SIH}	Serial Input Hold Time	10		ns
t_{SOH}	Serial Output Hold Time		10	ns
t_{SOV}	Serial Output Valid Time		35	ns
t_{PIS}	Parallel Input Setup Time	10		ns
t_{PIH}	Parallel Input Hold Time	10		ns
t_{POH}	Parallel Output Hold Time		10	ns
t_{POV}	Parallel Output Valid Time		35	ns
t_{SOE}	Serial Output Enable Time		10	ns
t_{SOX}	Serial Output Disable Time		25	ns
t_{POE}	Parallel Output Enable Time		10	ns
t_{POX}	Parallel Output Disable Time		25	ns
t_{SSE}	RST Active Lead Time	t_{SLSH}		ns
t_{SSD}	RST Inactive Lag Time	t_{SLSH}		ns
t_{ZSS}	SCK Setup to $\overline{SS}$ Low	25		ns
t_{SSZ}	SCK Hold after $\overline{SS}$ High	25		ns
t_{WR}	Write Cycle Time	2.5		ms
t_{AWR}	Write Cycle with Auto-Erase Time	5		ms
t_{ERS}	Chip Erase Cycle Time	7.5		ms

Note: 1. t_{SCK} is independent of t_{CLCL}.

Figure 18-2. Idle Supply Current vs. Vcc (1.8432 MHz Internal Oscillator)

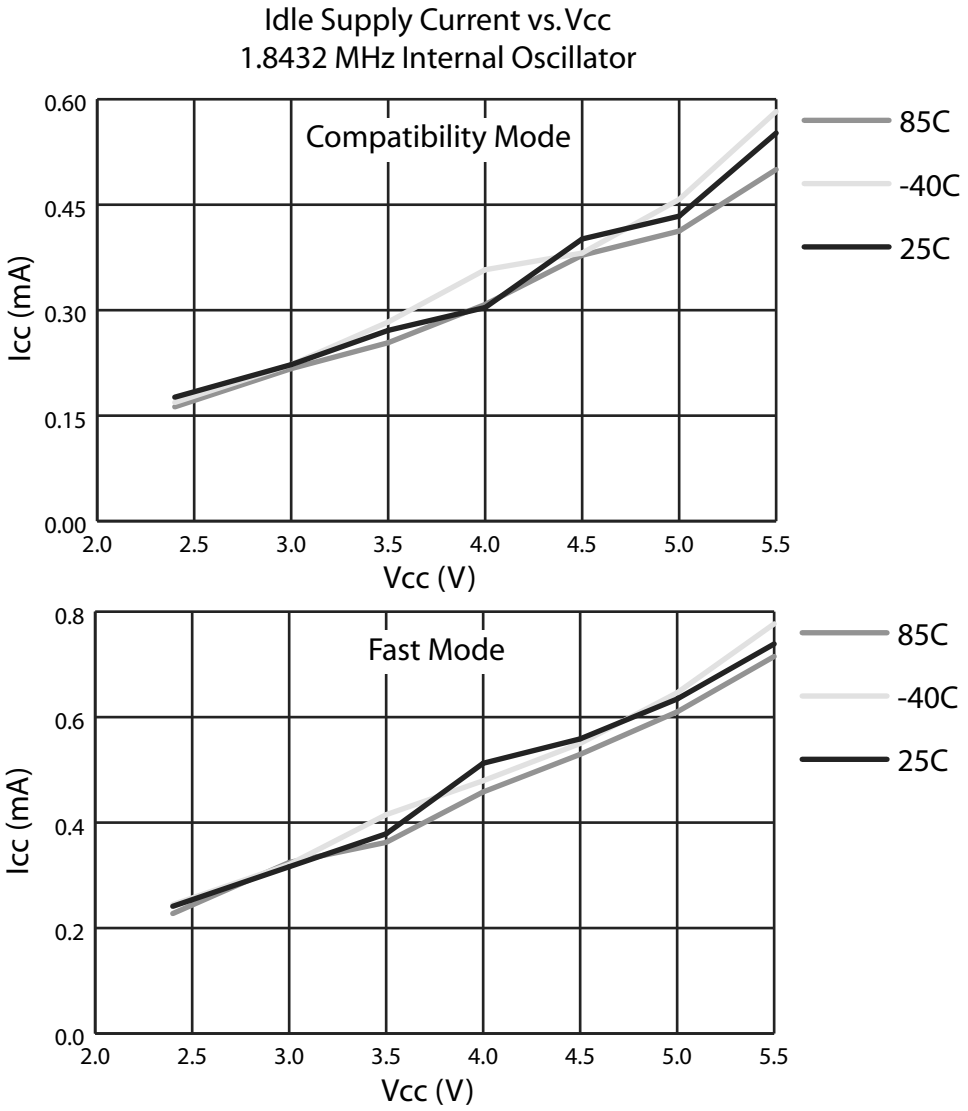
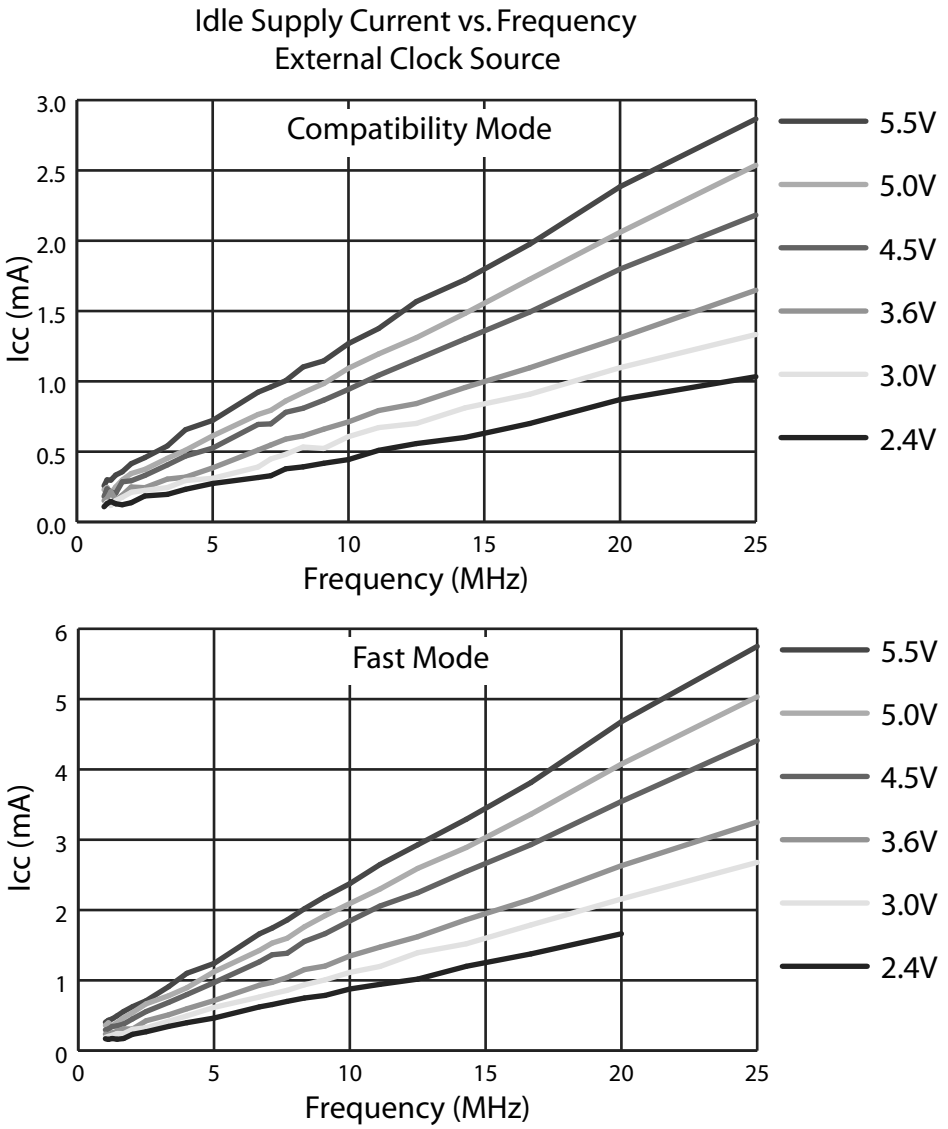


Figure 18-4. Idle Supply Current vs. Frequency



18.3.4 Quasi-Bidirectional Output

Figure 18-7. Quasi-Bidirectional Output I-V Source Characteristic at 5V

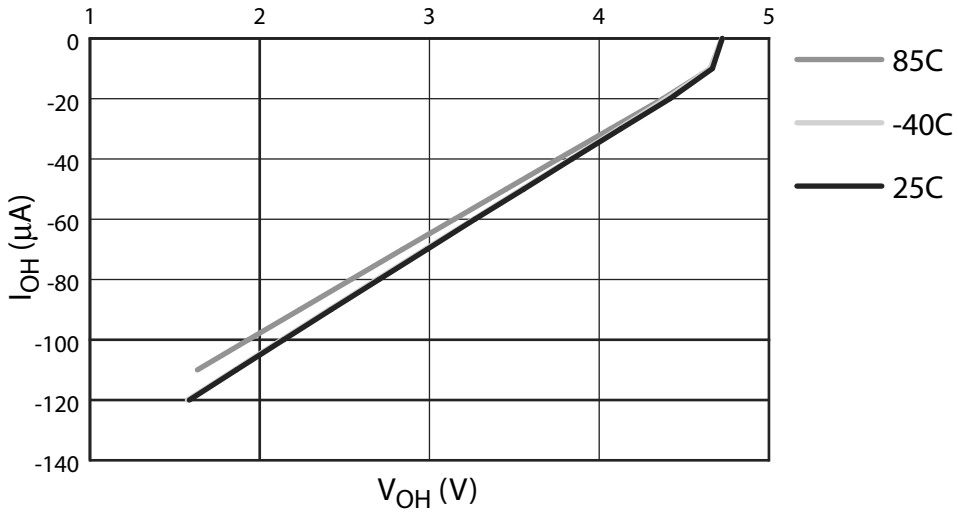


Figure 18-8. Quasi-Bidirectional Output I-V Source Characteristic at 3V

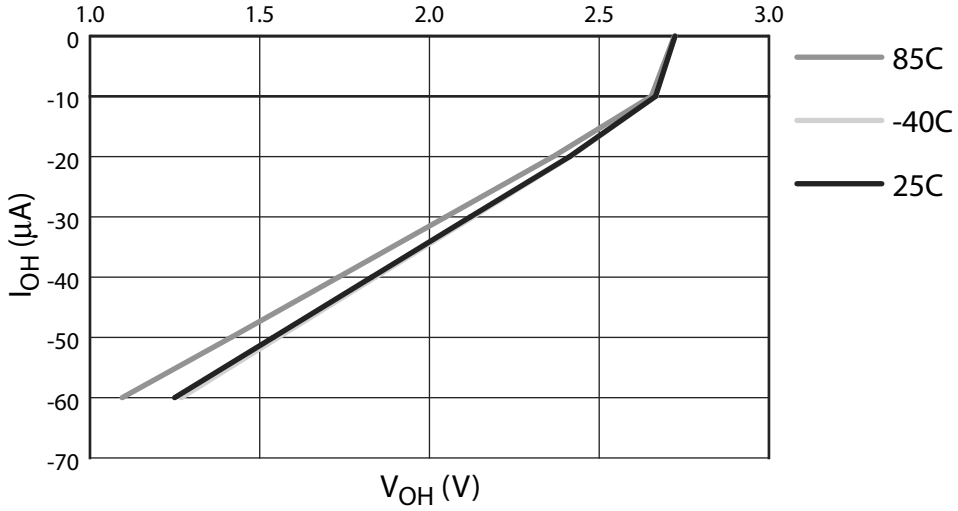


Figure 18-11. Push-Pull Output I-V Sink Characteristic at 5V

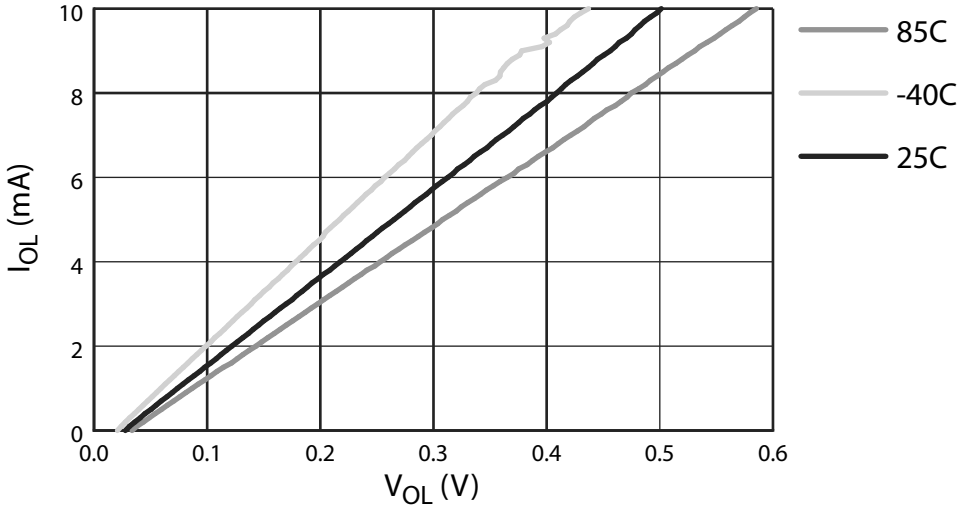
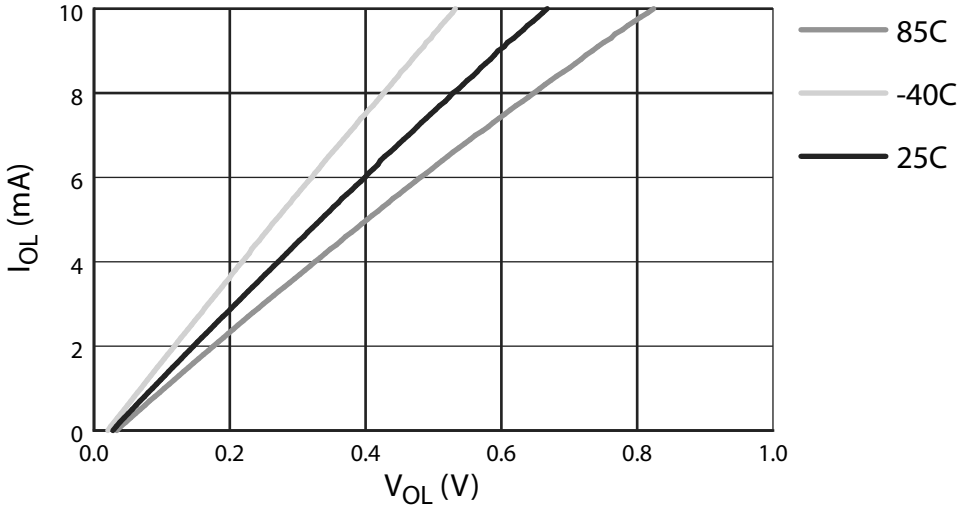


Figure 18-12. Push-Pull Output I-V Sink Characteristic at 3V

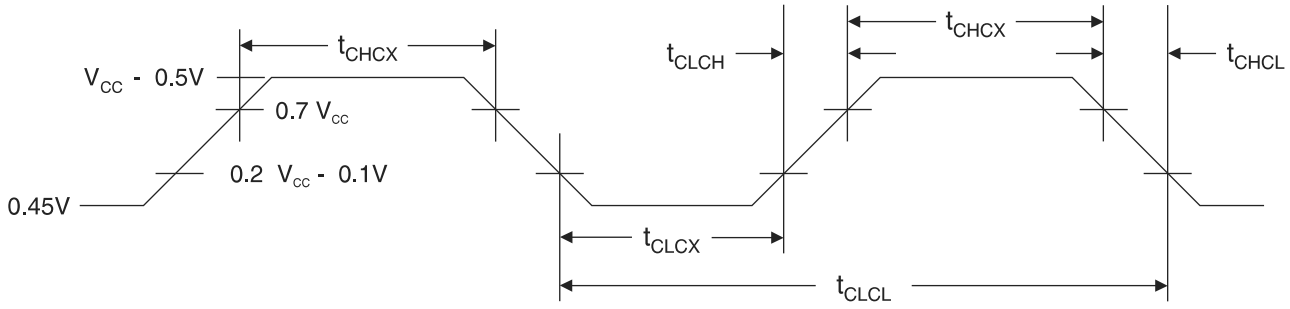


Note: The I_{OL}/V_{OL} characteristic applies to Push-Pull, Quasi-Bidirectional and Open-Drain modes.

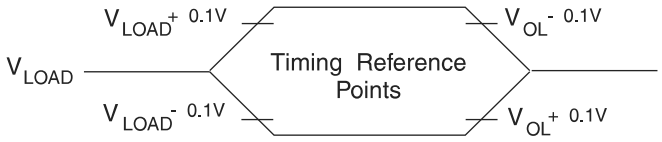
18.4 Clock Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{DD} = 2.4 to 5.5V, unless otherwise noted.

Figure 18-13. External Clock Drive Waveform

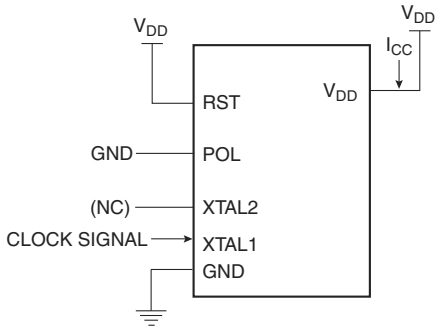


18.8.2 Float Waveform(1)



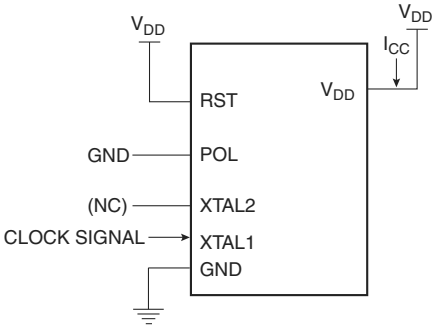
Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

18.8.3 I_{CC} Test Condition, Active Mode, All Other Pins are Disconnected(1)

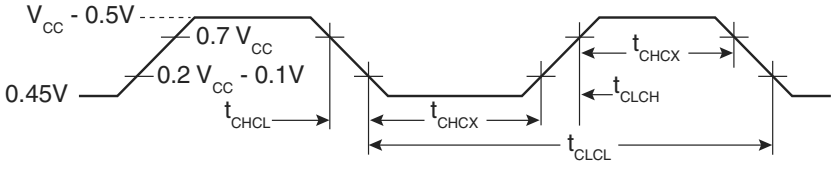


Notes: 1. For active supply current measurements all ports are configured in quasi-bidirectional mode. Timers 0, 1 and 2 are configured to be free running in their default timer modes. The CPU executes a simple random number generator that accesses RAM and SFR bus, and exercises the ALU and hardware multiplier.

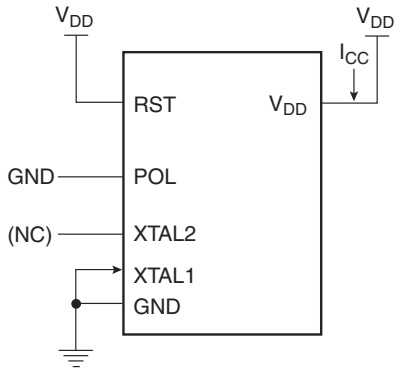
18.8.4 I_{CC} Test Condition, Idle Mode, All Other Pins are Disconnected



18.8.5 Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns



18.8.6 I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{DD} = 2V to 5.5V



Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: (+1) (408) 441-0311
Fax: (+1) (408) 487-2600
www.atmel.com
8051@atmel.com

Atmel Asia Limited
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
JAPAN
Tel: (+81) (3) 3523-3551
Fax: (+81) (3) 3523-7581