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Details

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Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08sh32vtl

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Chapter 4 Memory

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x1845	PTAPS	0	0	0	0	PTAPS3	PTAPS2	PTAPS1	PTAPS0
0x1846	PTAES	0	0	0	0	PTAES3	PTAES2	PTAES1	PTAES0
0x1847	Reserved	—	—	_	—	—	_	—	—
0x1848	PTBPE	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
0x1849	PTBSE	PTBSE7	PTBSE6	PTBSE5	PTBSE4	PTBSE3	PTBSE2	PTBSE1	PTBSE0
0x184A	PTBDS	PTBDS7	PTBDS6	PTBDS5	PTBDS4	PTBDS3	PTBDS2	PTBDS1	PTBDS0
0x184B	Reserved	_	_	_	_	_	_	_	
0x184C	PTBSC	0	0	0	0	PTBIF	PTBACK	PTBIE	PTBMOD
0x184D	PTBPS	0	0	0	0	PTBPS3	PTBPS2	PTBPS1	PTBPS0
0x184E	PTBES	0	0	0	0	PTBES3	PTBES2	PTBES1	PTBES0
0x184F	Reserved	_	_		_		_	_	_
0x1850	PTCPE	PTCPE7	PTCPE6	PTCPE5	PTCPE4	PTCPE3	PTCPE2	PTCPE1	PTCPE0
0x1851	PTCSE	PTCSE7	PTCSE6	PTCSE5	PTCSE4	PTCSE3	PTCSE2	PTCSE1	PTCSE0
0x1852	PTCDS	PTCDS7	PTCDS6	PTCDS5	PTCDS4	PTCDS3	PTCDS2	PTCDS1	PTCDS0
0x1853	GNGC	GNGPS7	GNGPS6	GNGPS5	GNGPS4	GNGPS3	GNGPS2	GNGPS1	GNGEN
0x1854	Reserved	_	_		_		1	1	1
0x1855	Reserved	_	_		_		1	1	1
0x1856	Reserved	_	_		_		0	0	0
0x1857– 0x185F	Reserved								

Table 4-3. High-Page Register Summary (Sheet 2 of 2)



the MCU secure. During development, whenever the FLASH is erased, it is good practice to immediately program the SEC00 bit to 0 in NVOPT so SEC01:SEC00 = 1:0. This would allow the MCU to remain unsecured after a subsequent reset.

The on-chip debug module cannot be enabled while the MCU is secure. The separate background debug controller can still be used for background memory access commands of unsecured resources.

A user can choose to allow or disallow a security unlocking mechanism through an 8-byte backdoor security key. If the nonvolatile KEYEN bit in NVOPT/FOPT is 0, the backdoor key is disabled and there is no way to disengage security without completely erasing all FLASH locations. If KEYEN is 1, a secure user program can temporarily disengage security by:

- 1. Writing 1 to KEYACC in the FCNFG register. This makes the FLASH module interpret writes to the backdoor comparison key locations (NVBACKKEY through NVBACKKEY+7) as values to be compared against the key rather than as the first step in a FLASH program or erase command.
- 2. Writing the user-entered key values to the NVBACKKEY through NVBACKKEY+7 locations. These writes must be done in order starting with the value for NVBACKKEY and ending with NVBACKKEY+7. STHX should not be used for these writes because these writes cannot be done on adjacent bus cycles. User software normally would get the key codes from outside the MCU system through a communication interface such as a serial I/O.
- 3. Writing 0 to KEYACC in the FCNFG register. If the 8-byte key that was just written matches the key stored in the FLASH locations, SEC01:SEC00 are automatically changed to 1:0 and security will be disengaged until the next reset.

The security key can be written only from secure memory (either RAM or FLASH), so it cannot be entered through background commands without the cooperation of a secure user program.

The backdoor comparison key (NVBACKKEY through NVBACKKEY+7) is located in FLASH memory locations in the nonvolatile register space so users can program these locations exactly as they would program any other FLASH memory location. The nonvolatile registers are in the same 512-byte block of FLASH as the reset and interrupt vectors, so block protecting that space also block protects the backdoor comparison key. Block protects cannot be changed from user application programs, so if the vector space is block protected, the backdoor security key mechanism cannot permanently change the block protect, security settings, or the backdoor key.

Security can always be disengaged through the background debug interface by taking these steps:

- 1. Disable any block protections by writing FPROT. FPROT can be written only with background debug commands, not from application software.
- 2. Mass erase FLASH if necessary.
- 3. Blank check FLASH. Provided FLASH is completely erased, security is disengaged until the next reset.

To avoid returning to secure mode after the next reset, program NVOPT so SEC01:SEC00 = 1:0.

4.7 FLASH Registers and Control Bits

The FLASH module has nine 8-bit registers in the high-page register space, two locations (NVOPT, NVPROT) in the nonvolatile register space in FLASH memory are copied into corresponding high-page



Chapter 6 Parallel Input/Output Control

6.6.1.6 Port A Interrupt Status and Control Register (PTASC)



Figure 6-8. Port A Interrupt Status and Control Register (PTASC)

Table 6-7. PTASC Register Field Descriptions

Field	Description
3 PTAIF	 Port A Interrupt Flag — PTAIF indicates when a port A interrupt is detected. Writes have no effect on PTAIF. 0 No port A interrupt detected. 1 Port A interrupt detected.
2 PTAACK	Port A Interrupt Acknowledge — Writing a 1 to PTAACK is part of the flag clearing mechanism. PTAACK always reads as 0.
1 PTAIE	 Port A Interrupt Enable — PTAIE determines whether a port A interrupt is enabled. 0 Port A interrupt request not enabled. 1 Port A interrupt request enabled.
0 PTAMOD	 Port A Detection Mode — PTAMOD (along with the PTAES bits) controls the detection mode of the port A interrupt pins. 0 Port A pins detect edges only. 1 Port A pins detect both edges and levels.

6.6.1.7 Port A Interrupt Pin Select Register (PTAPS)



Figure 6-9. Port A Interrupt Pin Select Register (PTAPS)

Table 6-8. PTAPS Register Field Descriptions

Field	Description
3:0 PTAPS[3:0]	 Port A Interrupt Pin Selects — Each of the PTAPSn bits enable the corresponding port A interrupt pin. 0 Pin not enabled as interrupt. 1 Pin enabled as interrupt.



Chapter 6 Parallel Input/Output Control

6.6.3 Port C Registers

Port C is controlled by the registers listed below.

6.6.3.1 Port C Data Register (PTCD)



Figure 6-19. Port C Data Register (PTCD)

Table 6-18. PTCD Register Field Descriptions

Field	Description
7:0 PTCD[7:0]	 Port C Data Register Bits — For port C pins that are inputs, reads return the logic level on the pin. For port C pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port C pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTCD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups disabled.

6.6.3.2 Port C Data Direction Register (PTCDD)

	7	6	5	4	3	2	1	0
R W	PTCDD7	PTCDD6	PTCDD5	PTCDD4	PTCDD3	PTCDD2	PTCDD1	PTCDD0
Reset:	0	0	0	0	0	0	0	0

Figure 6-20. Port C Data Direction Register (PTCDD)

Table 6-19. PTCDD Register Field Descriptions

Field	Description
7:0 PTCDD[7:0]	Data Direction for Port C Bits — These read/write bits control the direction of port C pins and what is read for PTCD reads.
	 Input (output driver disabled) and reads return the pin value. Output driver enabled for port C bit n and PTCD reads return the contents of PTCDn.



Chapter 7 Central Processor Unit (S08CPUV3)

Source	Operation	dress lode	Object Code	/cles	Cyc-by-Cyc Details	Affect on CCR		
l i onn		PΦ Φ		ΰ	Details	V 1 1 H	INZC	
BPL rel	Branch if Plus (if N = 0)	REL	2A rr	3	qqq	-11-		
BRA rel	Branch Always	REL	20 rr	3	qqq	- 1 1 -		
BRCLR n,opr8a,rel	Branch if Bit <i>n</i> in Memory Clear (if (Mn) = 0)	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 dd rr 03 dd rr 05 dd rr 07 dd rr 09 dd rr 0B dd rr 0D dd rr 0F dd rr	5 5 5 5 5 5 5 5 5	rpppp rpppp rpppp rpppp rpppp rpppp rpppp	- 1 1 -	\$	
BRN rel	Branch Never	REL	21 rr	3	qqq	- 1 1 -		
BRSET n,opr8a,rel	Branch if Bit <i>n</i> in Memory Set (if (Mn) = 1)	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 dd rr 02 dd rr 04 dd rr 06 dd rr 08 dd rr 0A dd rr 0C dd rr 0E dd rr	5 5 5 5 5 5 5 5 5	rpppp rpppp rpppp rpppp rpppp rpppp	- 1 1 -	\$	
BSET n,opr8a	Set Bit <i>n</i> in Memory (Mn ← 1)	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 dd 12 dd 14 dd 16 dd 18 dd 1A dd 1C dd 1E dd	5 5 5 5 5 5 5 5 5 5 5	rfwpp rfwpp rfwpp rfwpp rfwpp rfwpp rfwpp rfwpp	- 1 1 -		
BSR rel	$\begin{array}{c} \text{Branch to Subroutine} \\ \text{PC} \leftarrow (\text{PC}) + \$0002 \\ \text{push (PCL); SP} \leftarrow (\text{SP}) - \$0001 \\ \text{push (PCH); SP} \leftarrow (\text{SP}) - \$0001 \\ \text{PC} \leftarrow (\text{PC}) + \textit{rel} \end{array}$	REL	AD rr	5	qqqaa	- 1 1 -		
CBEQ opr8a,rel CBEQA #opr8i,rel CBEQX #opr8i,rel CBEQ oprx8,X+,rel CBEQ ,X+,rel CBEQ oprx8,SP,rel	Compare and Branch if $(A) = (M)$ Branch if $(A) = (M)$ Branch if $(X) = (M)$ Branch if $(A) = (M)$ Branch if $(A) = (M)$ Branch if $(A) = (M)$	DIR IMM IMM IX1+ IX+ SP1	31 dd rr 41 ii rr 51 ii rr 61 ff rr 71 rr 9E 61 ff rr	5 4 5 5 6	rpppp pppp pppp rpppp rfppp prpppp	- 1 1 -		
CLC	Clear Carry Bit (C \leftarrow 0)	INH	98	1	p	- 1 1 -	0	
CLI	Clear Interrupt Mask Bit (I \leftarrow 0)	INH	9A	1	q	- 1 1 -	0	
CLR opr8a CLRA CLRX CLRH CLR oprx8,X CLR ,X CLR oprx8,SP	Clear $M \leftarrow \$00$ $A \leftarrow \$00$ $X \leftarrow \$00$ $H \leftarrow \$00$ $M \leftarrow \$00$ $M \leftarrow \$00$ $M \leftarrow \$00$	DIR INH INH IX1 IX SP1	3F dd 4F 5F 8C 6F ff 7F 9E 6F ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwp prfwpp	011-	- 0 1 -	

Table 7-2. Instruction Set Summary (Sheet 3 of 9)



8.5 External Signal Description

The ACMP has two analog input pins, ACMP+ and ACMP- and one digital output pin ACMPO. Each of these pins can accept an input voltage that varies across the full operating voltage range of the MCU. As shown in Figure 8-2, the ACMP- pin is connected to the inverting input of the comparator, and the ACMP+ pin is connected to the comparator non-inverting input if ACBGS is a 0. As shown in Figure 8-2, the ACMPO pin can be enabled to drive an external pin.

The signal properties of ACMP are shown in Table 8-1.

Signal	Function	I/O
ACMP-	Inverting analog input to the ACMP. (Minus input)	Η
ACMP+	Non-inverting analog input to the ACMP. (Positive input)	I
ACMPO	Digital output of the ACMP.	0

Table 8-1. Signal Properties

8.6 Memory Map

8.6.1 Register Descriptions

The ACMP includes one register:

• An 8-bit status and control register

Refer to the direct-page register summary in the memory section of this data sheet for the absolute address assignments for all ACMP registers. This section refers to registers and control bits only by their names.

Some MCUs may have more than one ACMP, so register names include placeholder characters to identify which ACMP is being referenced.



Field	Description
5 ACFE	 Compare Function Enable — ACFE is used to enable the compare function. 0 Compare function disabled 1 Compare function enabled
4 ACFGT	 Compare Function Greater Than Enable — ACFGT is used to configure the compare function to trigger when the result of the conversion of the input being monitored is greater than or equal to the compare value. The compare function defaults to triggering when the result of the compare of the input being monitored is less than the compare value. Compare triggers when input is less than compare level Compare triggers when input is greater than or equal to compare level

Table 9-4. ADCSC2 Register Field Descriptions (continued)

9.3.3 Data Result High Register (ADCRH)

ADCRH contains the upper two bits of the result of a 10-bit conversion. When configured for 8-bit conversions both ADR8 and ADR9 are equal to zero. ADCRH is updated each time a conversion completes except when automatic compare is enabled and the compare condition is not met. In 10-bit MODE, reading ADCRH prevents the ADC from transferring subsequent conversion results into the result registers until ADCRL is read. If ADCRL is not read until after the next conversion is completed, then the intermediate conversion result will be lost. In 8-bit mode there is no interlocking with ADCRL. In the case that the MODE bits are changed, any data in ADCRH becomes invalid.



Figure 9-6. Data Result High Register (ADCRH)

9.3.4 Data Result Low Register (ADCRL)

ADCRL contains the lower eight bits of the result of a 10-bit conversion, and all eight bits of an 8-bit conversion. This register is updated each time a conversion completes except when automatic compare is enabled and the compare condition is not met. In 10-bit mode, reading ADCRH prevents the ADC from transferring subsequent conversion results into the result registers until ADCRL is read. If ADCRL is not read until the after next conversion is completed, then the intermediate conversion results will be lost. In 8-bit mode, there is no interlocking with ADCRH. In the case that the MODE bits are changed, any data in ADCRL becomes invalid.



Chapter 9 Analog-to-Digital Converter (S08ADCV1)



Figure 9-10. Configuration Register (ADCCFG)

Table 9-5. ADCCFG Register Field Descriptions

Field	Description
7 ADLPC	 Low Power Configuration — ADLPC controls the speed and power configuration of the successive approximation converter. This is used to optimize power consumption when higher sample rates are not required. 0 High speed configuration 1 Low power configuration: {FC31}The power is reduced at the expense of maximum clock speed.
6:5 ADIV	Clock Divide Select — ADIV select the divide ratio used by the ADC to generate the internal clock ADCK. Table 9-6 shows the available clock configurations.
4 ADLSMP	 Long Sample Time Configuration — ADLSMP selects between long and short sample time. This adjusts the sample period to allow higher impedance inputs to be accurately sampled or to maximize conversion speed for lower impedance inputs. Longer sample times can also be used to lower overall power consumption when continuous conversions are enabled if high conversion rates are not required. Short sample time Long sample time
3:2 MODE	Conversion Mode Selection — MODE bits are used to select between 10- or 8-bit operation. See Table 9-7.
1:0 ADICLK	Input Clock Select — ADICLK bits select the input clock source to generate the internal clock ADCK. See Table 9-8.

Table 9-6. Clock Divide Select

ADIV	Divide Ratio	Clock Rate
00	1	Input clock
01	2	Input clock ÷ 2
10	4	Input clock ÷ 4
11	8	Input clock ÷ 8

Table 9-7. Conversion Modes

MODE	Mode Description			
00	8-bit conversion (N=8)			
01	Reserved			
10	10-bit conversion (N=10)			
11	Reserved			



Chapter 11 Internal Clock Source (S08ICSV2)

- CLKS bits are written to 00
- IREFS bit is written to 1
- RDIV bits are written to divide trimmed reference clock to be within the range of 31.25 kHz to 39.0625 kHz.

In FLL engaged internal mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the internal reference clock. The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the internal reference clock is enabled.

11.4.1.2 FLL Engaged External (FEE)

The FLL engaged external (FEE) mode is entered when all the following conditions occur:

- CLKS bits are written to 00
- IREFS bit is written to 0
- RDIV bits are written to divide reference clock to be within the range of 31.25 kHz to 39.0625 kHz

In FLL engaged external mode, the ICSOUT clock is derived from the FLL clock which is controlled by the external reference clock. The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the external reference clock is enabled.

11.4.1.3 FLL Bypassed Internal (FBI)

The FLL bypassed internal (FBI) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is active or LP bit is written to 0

In FLL bypassed internal mode, the ICSOUT clock is derived from the internal reference clock. The FLL clock is controlled by the internal reference clock, and the FLL loop will lock the FLL frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK will be available for BDC communications, and the internal reference clock is enabled.

11.4.1.4 FLL Bypassed Internal Low Power (FBILP)

The FLL bypassed internal low power (FBILP) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is not active and LP bit is written to 1

In FLL bypassed internal low power mode, the ICSOUT clock is derived from the internal reference clock and the FLL is disabled. The ICSLCLK will be not be available for BDC communications, and the internal reference clock is enabled.

Chapter 12 Modulo Timer (S08MTIMV1)



 \triangle = Pin can be enabled as part of the ganged output drive feature

- NOTE: PTC7-PTC0 and PTA7-PTA6 not available on 16--pin Packages
 - PTC7-PTC4 and PTA7-PTA6 not available on 20-pin Packages
 - For the 16-pin and 20-pin packages: V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL}, are double bonded to V_{DD} and V_{SS} respectively.
 - When PTA4 is configured as BKGD, pin becomes bi-directional.

Figure 12-1. MC9S08SH32 Series Block Diagram Highlighting MTIM Block and Pins



Chapter 13 Real-Time Counter (S08RTCV1)



Chapter 14 Serial Communications Interface (S08SCIV4)

14.1.3 Block Diagram

Figure 14-2 shows the transmitter portion of the SCI.



Figure 14-2. SCI Transmitter Block Diagram

Chapter 15 Serial Peripheral Interface (S08SPIV3)



15.1.1 Features

Features of the SPI module include:

- Master or slave mode operation
- Full-duplex or single-wire bidirectional option
- Programmable transmit bit rate
- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting

15.1.2 Block Diagrams

This section includes block diagrams showing SPI system connections, the internal organization of the SPI module, and the SPI clock dividers that control the master mode bit rate.

15.1.2.1 SPI System Block Diagram

Figure 15-2 shows the SPI modules of two MCUs connected in a master-slave arrangement. The master device initiates all SPI data transfers. During a transfer, the master shifts data out (on the MOSI pin) to the slave while simultaneously shifting data in (on the MISO pin) from the slave. The transfer effectively exchanges the data that was in the SPI shift registers of the two SPI systems. The SPSCK signal is a clock output from the master and an input to the slave. The slave device must be selected by a low level on the slave select input (\overline{SS} pin). In this system, the master device has configured its \overline{SS} pin as an optional slave select output.



Figure 15-2. SPI System Connections

MC9S08SH32 Series Data Sheet, Rev. 3



Chapter 15 Serial Peripheral Interface (S08SPIV3)

The most common uses of the SPI system include connecting simple shift registers for adding input or output ports or connecting small peripheral devices such as serial A/D or D/A converters. Although Figure 15-2 shows a system where data is exchanged between two MCUs, many practical systems involve simpler connections where data is unidirectionally transferred from the master MCU to a slave or from a slave to the master MCU.

15.1.2.2 SPI Module Block Diagram

Figure 15-3 is a block diagram of the SPI module. The central element of the SPI is the SPI shift register. Data is written to the double-buffered transmitter (write to SPIxD) and gets transferred to the SPI shift register at the start of a data transfer. After shifting in a byte of data, the data is transferred into the double-buffered receiver where it can be read (read from SPIxD). Pin multiplexing logic controls connections between MCU pins and the SPI module.

When the SPI is configured as a master, the clock output is routed to the SPSCK pin, the shifter output is routed to MOSI, and the shifter input is routed from the MISO pin.

When the SPI is configured as a slave, the SPSCK pin is routed to the clock input of the SPI, the shifter output is routed to MISO, and the shifter input is routed from the MOSI pin.

In the external SPI system, simply connect all SPSCK pins to each other, all MISO pins together, and all MOSI pins together. Peripheral devices often use slightly different names for these pins.



Field	Description
7 CHnF	Channel n flag. When channel n is an input-capture channel, this read/write bit is set when an active edge occurs on the channel n pin. When channel n is an output compare or edge-aligned/center-aligned PWM channel, CHnF is set when the value in the TPM counter registers matches the value in the TPM channel n value registers. When channel n is an edge-aligned/center-aligned PWM channel and the duty cycle is set to 0% or 100%, CHnF will not be set even when the value in the TPM counter registers matches the value in the TPM channel n value registers. A corresponding interrupt is requested when CHnF is set and interrupts are enabled (CHnIE = 1). Clear CHnF by reading TPMxCnSC while CHnF is set and then writing a logic 0 to CHnF. If another interrupt request occurs before the clearing sequence is complete, the sequence is reset so CHnF remains set after the clear sequence completed for the earlier CHnF. This is done so a CHnF interrupt request cannot be lost due to clearing a previous CHnF. Reset clears the CHnF bit. Writing a logic 1 to CHnF has no effect. 0 No input capture or output compare event occurred on channel n 1 Input capture or output compare event on channel n
6 CHnIE	 Channel n interrupt enable. This read/write bit enables interrupts from channel n. Reset clears CHnIE. Channel n interrupt requests disabled (use for software polling) Channel n interrupt requests enabled
5 MSnB	Mode select B for TPM channel n. When CPWMS=0, MSnB=1 configures TPM channel n for edge-aligned PWM mode. Refer to the summary of channel mode and setup controls in Table 16-7.
4 MSnA	 Mode select A for TPM channel n. When CPWMS=0 and MSnB=0, MSnA configures TPM channel n for input-capture mode or output compare mode. Refer to Table 16-7 for a summary of channel mode and setup controls. Note: If the associated port pin is not stable for at least two bus clock cycles before changing to input capture mode, it is possible to get an unexpected indication of an edge trigger.
3–2 ELSnB ELSnA	Edge/level select bits. Depending upon the operating mode for the timer channel as set by CPWMS:MSnB:MSnA and shown in Table 16-7, these bits select the polarity of the input edge that triggers an input capture event, select the level that will be driven in response to an output compare match, or select the polarity of the PWM output. Setting ELSnB:ELSnA to 0:0 configures the related timer pin as a general purpose I/O pin not related to any timer functions. This function is typically used to temporarily disable an input capture channel or to make the timer pin available as a general purpose I/O pin when the associated timer channel is set up as a software timer that does not require the use of a pin.

Table 16-6. TPMxCnSC Field Descriptions

Table 16-7. Mode, Edge, and Level Selection

CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration	
Х	XX	00	Pin not used for TPM - revert to general purpose I/O or other peripheral control		



Chapter 16 Timer/PWM Module (S08TPMV3)

(becomes unlatched) when the TPMxCnSC register is written (whether BDM mode is active or not). Any write to the channel registers will be ignored during the input capture mode.

When BDM is active, the coherency mechanism is frozen (unless reset by writing to TPMxCnSC register) such that the buffer latches remain in the state they were in when the BDM became active, even if one or both halves of the channel register are read while BDM is active. This assures that if the user was in the middle of reading a 16-bit register when BDM became active, it will read the appropriate value from the other half of the 16-bit value after returning to normal execution. The value read from the TPMxCnVH and TPMxCnVL registers in BDM mode is the value of these registers and not the value of their read buffer.

In output compare or PWM modes, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer. After both bytes are written, they are transferred as a coherent 16-bit value into the timer-channel registers according to the value of CLKSB:CLKSA bits and the selected mode, so:

- If (CLKSB:CLKSA = 0:0), then the registers are updated when the second byte is written.
- If (CLKSB:CLKSA not = 0:0 and in output compare mode) then the registers are updated after the second byte is written and on the next change of the TPM counter (end of the prescaler counting).
- If (CLKSB:CLKSA not = 0:0 and in EPWM or CPWM modes), then the registers are updated after the both bytes were written, and the TPM counter changes from (TPMxMODH:TPMxMODL - 1) to (TPMxMODH:TPMxMODL). If the TPM counter is a free-running counter then the update is made when the TPM counter changes from 0xFFFE to 0xFFFF.

The latching mechanism may be manually reset by writing to the TPMxCnSC register (whether BDM mode is active or not). This latching mechanism allows coherent 16-bit writes in either big-endian or little-endian order which is friendly to various compiler implementations.

When BDM is active, the coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active even if one or both halves of the channel register are written while BDM is active. Any write to the channel registers bypasses the buffer latches and directly write to the channel register while BDM is active. The values written to the channel register while BDM is active are used for PWM & output compare operation once normal execution resumes. Writes to the channel registers while BDM is active do not interfere with partial completion of a coherency sequence. After the coherency mechanism has been fully exercised, the channel registers are updated using the buffered values written (while BDM was not active) by the user.

16.4 Functional Description

All TPM functions are associated with a central 16-bit counter which allows flexible selection of the clock source and prescale factor. There is also a 16-bit modulo register associated with the main counter.

The CPWMS control bit chooses between center-aligned PWM operation for all channels in the TPM (CPWMS=1) or general purpose timing functions (CPWMS=0) where each channel can independently be configured to operate in input capture, output compare, or edge-aligned PWM mode. The CPWMS control bit is located in the main TPM status and control register because it affects all channels within the TPM and influences the way the main counter operates. (In CPWM mode, the counter changes to an up/down mode rather than the up-counting mode used for general purpose timer functions.)



17.3.6 Hardware Breakpoints

The BRKEN control bit in the DBGC register may be set to 1 to allow any of the trigger conditions described in Section 17.3.5, "Trigger Modes," to be used to generate a hardware breakpoint request to the CPU. TAG in DBGC controls whether the breakpoint request will be treated as a tag-type breakpoint or a force-type breakpoint. A tag breakpoint causes the current opcode to be marked as it enters the instruction queue. If a tagged opcode reaches the end of the pipe, the CPU executes a BGND instruction to go to active background mode rather than executing the tagged opcode. A force-type breakpoint causes the CPU to finish the current instruction and then go to active background mode.

If the background mode has not been enabled (ENBDM = 1) by a serial WRITE_CONTROL command through the BKGD pin, the CPU will execute an SWI instruction instead of going to active background mode.

17.4 Register Definition

This section contains the descriptions of the BDC and DBG registers and control bits.

Refer to the high-page register summary in the device overview chapter of this data sheet for the absolute address assignments for all DBG registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

17.4.1 BDC Registers and Control Bits

The BDC has two registers:

- The BDC status and control register (BDCSCR) is an 8-bit register containing control and status bits for the background debug controller.
- The BDC breakpoint match register (BDCBKPT) holds a 16-bit breakpoint match address.

These registers are accessed with dedicated serial BDC commands and are not located in the memory space of the target MCU (so they do not have addresses and cannot be accessed by user programs).

Some of the bits in the BDCSCR have write limitations; otherwise, these registers may be read or written at any time. For example, the ENBDM control bit may not be written while the MCU is in active background mode. (This prevents the ambiguous condition of the control bit forbidding active background mode while the MCU is already in active background mode.) Also, the four status bits (BDMACT, WS, WSF, and DVF) are read-only status indicators and can never be written by the WRITE_CONTROL serial BDC command. The clock switch (CLKSW) control bit may be read or written at any time.



A.12.3 SPI

Table A-15 and Figure A-14 through Figure A-17 describe the timing requirements for the SPI system.

Num ¹	С	Rating ²		Symbol	Min	Max	Unit
1	D	Cycle time	Master Slave	t _{SCK} t _{SCK}	2 4	2048 —	t _{cyc} t _{cyc}
2	D	Enable lead time	Master Slave	t _{Lead} t _{Lead}	 1/2	1/2	t _{SCK} t _{SCK}
3	D	Enable lag time	Master Slave	t _{Lag} t _{Lag}	 1/2	1/2	t _{SCK} t _{SCK}
4	D	Clock (SPSCK) high time Master and Slave		t _{SCKH}	1/2 t _{SCK} – 25	_	ns
5	D	Clock (SPSCK) low time Master and Slave		t _{SCKL}	1/2 t _{SCK} – 25	_	ns
6	D	Data setup time (inputs)	Master Slave	t _{SI(M)} t _{SI(S)}	30 30		ns ns
7	D	Data hold time (inputs)	Master Slave	t _{HI(M)} t _{HI(S)}	30 30		ns ns
8	D	Access time, slave ³		t _A	0	40	ns
9	D	Disable time, slave ⁴		t _{dis}	—	40	ns
10	D	Data setup time (outputs)	Master Slave	t _{SO} t _{SO}		25 25	ns ns
11	D	Data hold time (outputs)	Master Slave	t _{но} t _{но}	-10 -10		ns ns
12	D	Operating frequency	Master Slave	f _{op} f _{op}	f _{Bus} /2048 dc	5 ⁵ f _{Bus} /4	MHz

Table A-15.	SPI Electrical	Characteristic
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¹ Refer to Figure A-14 through Figure A-17.

² All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

³ Time to data active from high-impedance state.

⁴ Hold time to high-impedance state.

⁵ Maximum baud rate must be limited to 5 MHz due to input filter characteristics.



A.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

A.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Parameter	Symbol	Conditions	Frequency	f _{OSC} /f _{BUS}	Level ¹ (Max)	Unit
	V _{RE_TEM}	$V_{DD} = 5 V$ $T_A = +25^{\circ}C$ package type 28 TSSOP	0.15 – 50 MHz	4 MHz crystal 20 MHz bus	12	dBμV
			50 – 150 MHz		12	
Radiated emissions,			150 – 500 MHz		6	
electric field			500 – 1000 MHz		-8	
			IEC Level ²		Ν	—
			SAE Level ³		2	—

Table A-17. Radiated Emissions, Electric Field

¹ Data based on qualification test results.

 $^2~$ IEC Level Maximums: N \leq 12dBµV, L \leq 24dBµV, I \leq 36dBµV

 3 SAE Level Maximums: 1 \leq 10dBµV, 2 \leq 20dBµV, 3 \leq 30dBµV, 4 \leq 40dBµV