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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	8-Bit
Speed	75MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	12
Program Memory Size	3KB (2K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	137 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/parallax/sx20ac-ss-g

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1.2 Key Features

50 MIPS Performance

- SX20AC/SX28AC: DC - 75 MHz
- SX20AC/SX28AC: 13.3 ns instruction cycle, 39.9 ns internal interrupt response
- 1 instruction per clock (branches 3)

EE/FLASH Program Memory and SRAM Data Memory

- Access time of < 13.3 ns provides single cycle access
- EE/Flash rated for > 10,000 rewrite cycles
- 2048 Words EE/Flash program memory
- 136x8 bits SRAM data memory

CPU Features

- Compact instruction set
- All instructions are single cycle except branch
- Eight-level push/pop hardware stack for subroutine linkage
- Fast table lookup capability through run-time readable code (IREAD instruction)
- Totally predictable program execution flow for hard real-time applications

Fast and Deterministic Interrupt

- Jitter-free 3-cycle internal interrupt response
- Hardware context save/restore of key resources such as PC, W, STATUS, and FSR within the 3-cycle interrupt response time
- External wakeup/interrupt capability on Port B (8 pins)

Flexible I/O

- All pins individually programmable as I/O
- Inputs are TTL or CMOS level selectable
- All pins have selectable internal pull-ups
- Selectable Schmitt Trigger inputs on Ports B, and C
- All outputs capable of sourcing/sinking 30 mA
- Port A outputs have symmetrical drive
- Analog comparator support on Port B (RB0 OUT, RB1 IN-, RB2 IN+)
- Selectable I/O operation synchronous to the oscillator clock

Hardware Peripheral Features

- One 8-bit Real Time Clock/Counter (RTCC) with programable 8-bit prescaler
- Watchdog Timer (shares the RTCC prescaler)
- Analog comparator
- Brown-out detector
- Multi-Input Wakeup logic on 8 pins
- Internal RC oscillator with configurable rate from 31.25 kHz to 4 MHz
- Power-On-Reset

Packages

- 20-pin SSOP, 28-pin DIP/SSOP

Programming and Debugging Support

- On- chip in-system programming support with serial and parallel interfaces
- In-system serial programming via oscillator pins
- On-chip in-System debugging support logic
- Real-time emulation, full program debug, and integrated development environment offered by third party tool vendors

1.3 Architecture

The SX devices use a modified Harvard architecture. This architecture uses two separate memories with separate address buses, one for the program and one for data, while allowing transfer of data from program memory to SRAM. This ability allows accessing data tables from program memory. The advantage of this architecture is that instruction fetch and memory transfers can be overlapped with a multi-stage pipeline, which means the next instruction can be fetched from program memory while the current instruction is being executed using data from the data memory.

Ubicom has developed a revolutionary RISC-based architecture and memory design techniques that is 20 times faster than conventional MCUs, deterministic, jitter free, and totally reprogramable.

The SX family implements a four-stage pipeline (fetch, decode, execute, and write back), which results in execution of one instruction per clock cycle. For example, at the maximum operating frequency of 75 MHz, instructions are executed at the rate of one per 13.3ns clock cycle.

1.3.1 The Virtual Peripheral Concept

Virtual Peripheral concept enables the “software system on a chip” approach. Virtual Peripheral, a software module that replaces a traditional hardware peripheral, takes advantage of the Ubicom architecture’s high performance and deterministic nature to produce same results as the hardware peripheral with much greater flexibility.

The speed and flexibility of the Ubicom architecture complemented with the availability of the Virtual Peripheral library, simultaneously address a wide range of engineering and product development concerns. They decrease the product development cycle dramatically, shortening time to production to as little as a few days.

Ubicom’s time-saving Virtual Peripheral library gives the system designers a choice of ready-made solutions, or a head start on developing their own peripherals. So, with Virtual Peripheral modules handling established functions, design engineers can concentrate on adding value to other areas of the application.

The concept of Virtual Peripheral combined with in-system re-programmability provides a power development platform ideal for the communications industry because of the numerous and rapidly evolving standards and protocols.

Overall, the concept of Virtual Peripheral provides benefits such as using a more simple device, reduced component count, fast time to market, increased flexibility in design, customization to your application, and ultimately overall system cost reduction.

Some examples of Virtual Peripheral modules are:

- Communication interfaces such as I^2C™, Microwire™ (µ-Wire), SPI, IrDA Stack, UART, and Modem functions
- Frequency generation and measurement
- PPM/PWM output
- Delta/Sigma ADC
- DTMF generation/detection
- PSK/FSK generation/detection
- FFT/DFT based algorithms

1.3.2 The Communications Controller

The combination of the Ubicom hardware architecture and the Virtual Peripheral concept create a powerful, creative platform for the communications design communities: SX communications controller. Its high processing power, recofigurability, cost-effectiveness, and overall design freedom give the designer the power to build products for the future with the confidence of knowing that they can keep up with innovation in standards and other areas.

1.4 Programming and Debugging Support

The SX devices are currently supported by third party tool vendors. On-chip in-system debug capabilities have been added, allowing tools to provide an integrated development environment including editor, macro assembler, debugger, and programmer. Un-obtrusive in-system programming is provided through the OSC pins. There is no need for a bon-out chip, so the user does not have to worry about the potential variations in electrical characteristics of a bond-out chip and the actual chip used in the target applications. the user can test and revise the fully debugged code in the actual SX, in the actual application, and get to production much faster.

1.5 Applications

Emerging applications and advances in existing ones require higher performance while maintaining low cost and fast time-to-production.

The device provides solutions for many familiar applications such as process controllers, electronic appliances/tools, security/monitoring systems, consumer automotive, sound generation, motor control, and personal communication devices. In addition, the device is suitable for applications that require DSP-like capabilities, such as closed-loop servo control (digital filters), digital answering machines, voice notation, interactive toys, and magnetic-stripe readers.

Furthermore, the growing Virtual Peripheral library features new components, such as the Internet Protocol stack, and communication interfaces, that allow design engineers to embed Internet connectivity into all of their products at extremely low cost and very little effort.

3.0 PORT DESCRIPTIONS

The device contains a 4-bit I/O port (Port A) and two 8-bit I/O ports (Port B, Port C). Port A provides symmetrical drive capability. Each port has three associated 8-bit registers (Direction, Data, TTL/CMOS Select, and Pull-Up Enable) to configure each port pin as Hi-Z input or output, to select TTL or CMOS voltage levels, and to enable/disable the weak pull-up resistor. The upper four bits of the registers associated with Port A are not used. The least significant bit of the registers corresponds to the least significant port pin. To access these registers, an appropriate value must be written into the MODE register.

Upon power-up, all bits in these registers are initialized to "1".

The associated registers allow for each port bit to be individually configured under software control as shown below:

Table 3-1. Port Configuration

Data Direction Registers: RA, RB, RC		TTL/CMOS Select Registers: LVL_A, LVL_B, LVL_C		Pullup Enable Registers: PLP_A, PLP_B, PLP_C	
0	1	0	1	0	1
Output	Hi-Z Input	CMOS	TTL	Enable	Disable

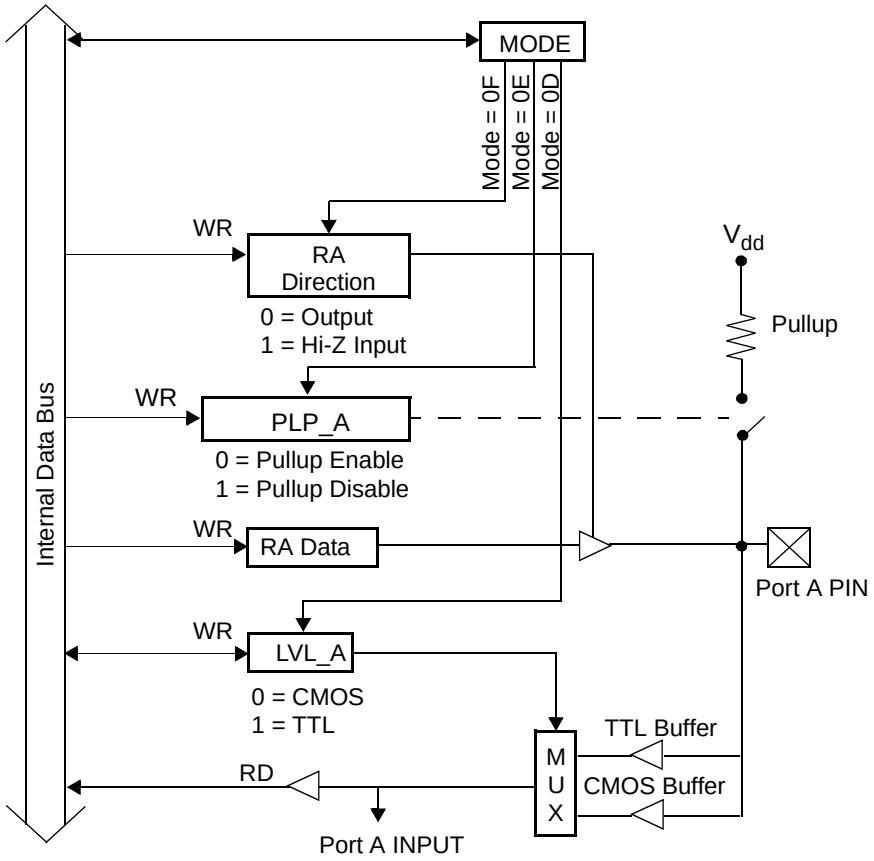


Figure 3-1. Port A Configuration

3.1 Reading and Writing the Ports

The three ports are memory-mapped into the data memory address space. To the CPU, the three ports are available as the RA, RB, and RC file registers at data memory addresses 05h, 06h, and 07h, respectively.

Writing to a port data register sets the voltage levels of the corresponding port pins that have been configured to operate as outputs. Reading from a register reads the voltage levels of the corresponding port pins that have been configured as inputs.

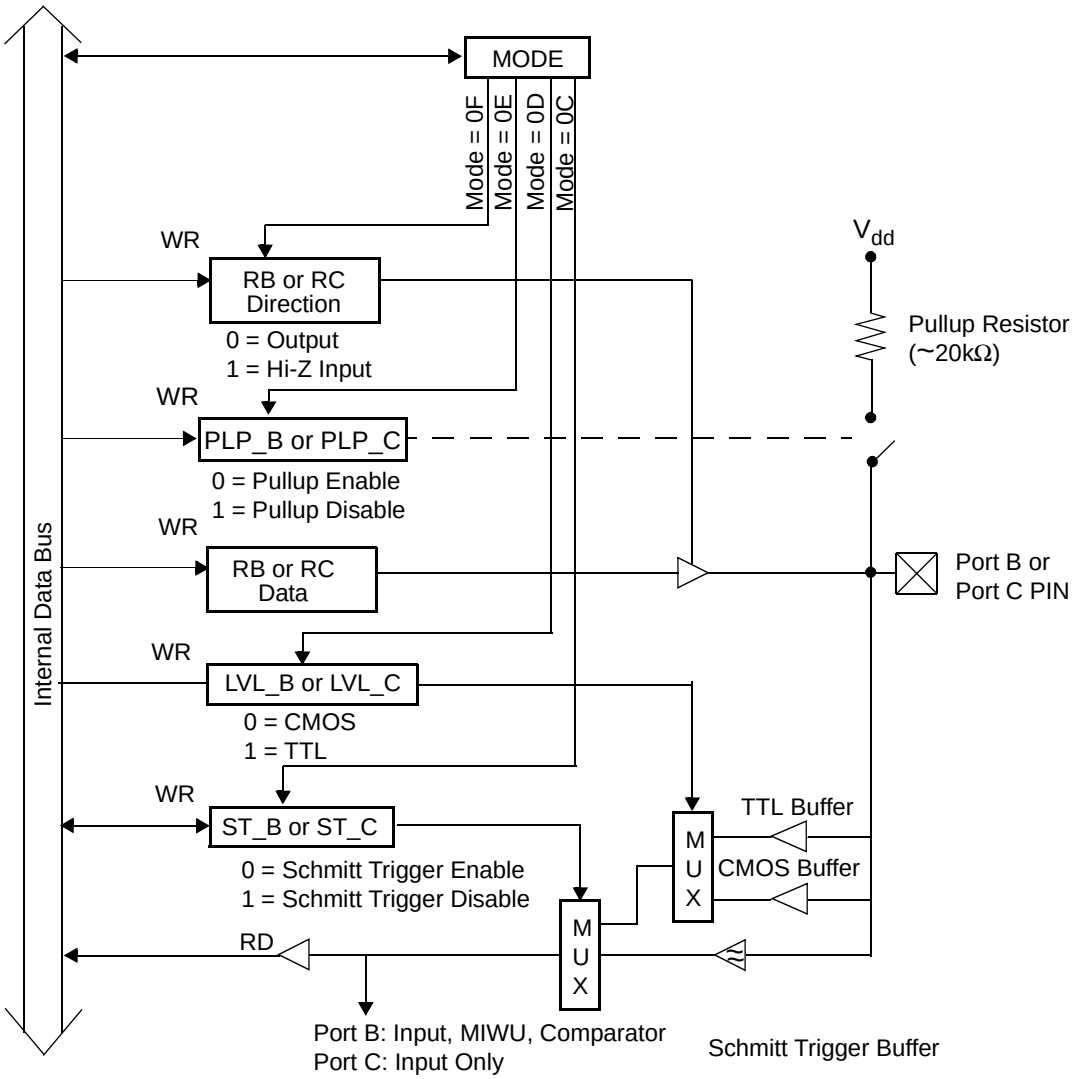


Figure 3-2. Port B, Port C Configuration

For example, suppose all four Port A pins are configured as outputs and with RA0 and RA1 to be high, and RA2 and RA3 to be low:

```
mov   W,#$03    ;load W with the value 03h
                ;(bits 0 and 1 high)
mov   $05,W     ;write 03h to Port A data
                ;register
```

The second “mov” instruction in this example writes the Port A data register (RA), which controls the output levels of the four Port A pins, RA0 through RA3. Because Port A has only four I/O pins, only the four least significant bits of this register are used. The four high-order register bits are “don’t care” bits. Port B and Port C are both eight bits wide, so the full widths of the RB and RC registers are used.

When a write is performed to a bit position for a port that has been configured as an input, a write to the port data register is still performed, but it has no immediate effect on the pin. If later that pin is configured to operate as an output, it will reflect the value that has been written to the data register.

When a read is performed from a bit position for a port, the operation is actually reading the voltage level on the pin itself, not necessarily the bit value stored in the port data register. This is true whether the pin is configured to operate as an input or an output. Therefore, with the pin configured to operate as an input, the data register contents have no effect on the value that you read. With the pin configured to operate as an output, what is read generally matches what has been written to the register.

3.1.1 Read-Modify-Write Considerations

Caution must be exercised when performing two successive read-modify-write instructions (SETB or CLRB operations) on I/O port pin. Input data used for an instruction must be valid *during* the time the instruction is executed, and the output result from an instruction is valid only *after* that instruction completes its operation. Unexpected results from successive read-modify-write operations on I/O pins can occur when the device is running at high speeds. Although the device has an internal write-back section to prevent such conditions, it is still recommended that the user program include a NOP instruction as a buffer between successive read-modify-write instructions performed on I/O pins of the same port.

Also note that reading an I/O port is actually reading the pins, not the output data latches. That is, if the pin output driver is enabled and driven high while the pin is held low externally, the port pin will read low.

3.2 Port Configuration

Each port pin offers the following configuration options:

- data direction
- input voltage levels (TTL or CMOS)
- pullup type (pullup resistor enable or disable)
- Schmitt trigger input (for Port B and Port C only)

Port B offers the additional option to use the port pins for the Multi-Input Wakeup/Interrupt function and/or the analog comparator function.

Port configuration is performed by writing to a set of control registers associated with the port. A special-purpose instruction is used to write these control registers:

- mov !RA,W (move W to Port A control register)
- mov !RB,W (move W to Port B control register)
- mov !RC,W (move W to Port C control register)

Each one of these instructions writes a port control register for Port A, Port B, or Port C. There are multiple control registers for each port. To specify which one you want to access, you use another register called the MODE register.

3.2.1 MODE Register

The MODE register controls access to the port configuration registers. Because the MODE register is not memory-mapped, it is accessed by the following special-purpose instructions:

- mov M, #lit (move literal to MODE register)
- mov M,W (move W to MODE register)
- mov W,M (move MODE register to W)

The value contained in the MODE register determines which port control register is accessed by the “mov !rx,W” instruction as indicated in Table 3-3. MODE register values not listed in the table are reserved for future expansion and should not be used. Therefore, the MODE register should always contain a value from 08h to 0Fh. Upon reset, the MODE register is initialized to 0Fh, which enables access to the port direction registers.

After a value is written to the MODE register, that setting remains in effect until it is changed by writing to the MODE register again. For example, you can write the value 0Eh to the MODE register just once, and then write to each of the three pullup configuration registers using the three “mov !rx,W” instructions.

Table 3-3. MODE Register and Port Control Register Access

MODE Reg.	mov !RA,W	mov !RB,W	mov !RC,W
08h	not used	CMP_B	not used
09h	not used	WKPND_B	not used
0Ah	not used	WKED_B	not used
0Bh	not used	WKEN_B	not used
0Ch	not used	ST_B	ST_C
0Dh	LVL_A	LVL_B	LVL_C
0Eh	PLP_A	PLP_B	PLP_C
0Fh	RA Direction	RB Direction	RC Direction

The following code example shows how to program the pullup control registers.

```
mov  M,#$0E   ;MODE=0Eh to access port pullup
              ;registers

mov  W,#$03   ;W = 0000 0011
mov  !RA,W    ;disable pullups for A0 and A1

mov  W,#$FF   ;W = 1111 1111
mov  !RB,W    ;disable all pullups for B0-B7

mov  W,#$00   ;W = 0000 0000
mov  !RC,W    ;enable all pullups for C0-C7
```

First the MODE register is loaded with 0Eh to select access to the pullup control registers (PLP_A, PLP_B, and PLP_C). Then the MOV !rx,W instructions are used to specify which port pins are to be connected to the internal pullup resistors. Setting a bit to 1 disconnects the corresponding pullup resistor, and clearing a bit to 0 connects the corresponding pullup resistor.

3.2.2 Port Configuration Registers

The port configuration registers that you control with the MOV !rx,W instruction operate as described below.

RA, RB, and RC Data Direction Registers (MODE=0Fh)

Each register bit sets the data direction for one port pin. Set the bit to 1 to make the pin operate as a high-impedance input. Clear the bit to 0 to make the pin operate as an output.

4.3 OPTION Register

RTW	RTE _IE	RTS	RTE _ES	PSA	PS2	PS1	PS0

Bit 7 **Bit 0**

When the OPTIONX bit in the FUSE word is cleared, bits 7 and 6 of the OPTION register function as described below.

When the OPTIONX bit is set, bits 7 and 6 of the OPTION register read as ‘1’s.

RTW RTCC/W register selection:
0 = Register 01h addresses W
1 = Register 01h addresses RTCC

RTE_IE RTCC edge interrupt enable:
0 = RTCC roll-over interrupt is enabled
1 = RTCC roll-over interrupt is disabled

RTS RTCC increment select:
0 = RTCC increments on internal instruction cycle
1 = RTCC increments upon transition on RTCC pin

RTE_ES RTCC edge select:
0 = RTCC increments on low-to-high transitions
1 = RTCC increments on high-to-low transitions

PSA Prescaler Assignment:
0 = Prescaler is assigned to RTCC, with divide rate determined by PS0-PS2 bits
1 = Prescaler is assigned to WDT, and divide rate on RTCC is 1:1

PS2-PS0 Prescaler divider (see Table 4-2)

Table 4-2. Prescaler Divider Ratios

PS2, PS1, PS0	RTCC Divide Rate	Watchdog Timer Divide Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1:128	1:64
111	1:256	1:128

Upon reset, all bits in the OPTION register are set to 1.

6.0 MEMORY ORGANIZATION

6.1 Program Memory

The program memory is organized as 2K, 12-bit wide words. The program memory words are addressed sequentially by a binary program counter. The program counter starts at zero. If there is no branch operation, it will increment to the maximum value possible for the device and roll over and begin again.

Internally, the program memory has a semi-transparent page structure. A page is composed of 512 contiguous program memory words. The lower nine bits of the program counter are zeros at the first address of a page and ones at the last address of a page. This page structure has no effect on the program counter. The program counter will freely increment through the page boundaries.

6.1.1 Program Counter

The program counter contains the 11-bit address of the instruction to be executed. The lower eight bits of the program counter are contained in the PC register (02h) while the upper bits come from the upper three bits of the STATUS register (PA0, PA1, PA2). This is necessary to cause jumps and subroutine calls *across* program memory page boundaries. Prior to the execution of a branch operation, the user program must initialize the upper bits of the STATUS register to cause a branch to the desired page. An alternative method is to use the PAGE instruction, which automatically causes branch to the desired page, based on the value specified in the operand field. Upon reset, the program counter is initialized with 07FFh.

6.1.2 Subroutine Stack

The subroutine stack consists of eight 11-bit save registers. A physical transfer of register contents from the program counter to the stack or vice versa, and within the stack, occurs on all operations affecting the stack, primarily calls and returns. The stack is physically and logically separate from data RAM. The program cannot read or write the stack.

6.2 Data Memory

The data memory consists of 136 bytes of RAM, organized as eight banks of 16 registers plus eight registers which are not banked. Both banked and non-banked memory locations can be addressed directly or indirectly using the FSR (File Select Register). The special-function registers are mapped into the data memory.

6.2.1 File Select Register (04h)

Instructions that specify a register as the operand can only express five bits of register address. This means that only registers 00h to 1Fh can be accessed. The File Select Register (FSR) provides the ability to access registers beyond 1Fh.

Figure 6-1 shows how FSR can be used to address RAM locations. The three high-order bits of FSR select one of eight SRAM banks to be accessed. The five low-order bits select one of 32 SRAM locations within the selected bank. For the lower 16 addresses, Bank 0 is always accessed, irrespective of the three high-order bits. Thus, RAM register addresses 00h through 0Fh are “global” in that they can always be accessed, regardless of the contents of the FSR.

The entire data memory (including the dedicated-function registers) consists of the lower 16 bytes of Bank 0 and the upper 16 bytes of Bank 0 through Bank 7, for a total of (1+8)*16 = 144 bytes. Eight of these bytes are for the function registers, leaving 136 general-purpose memory locations. In the 18-pin SX packages, register RC is not used, which makes address 07h available as an additional general-purpose memory location.

Below is an example of how to write to register 10h in Bank 4:

```
mov     FSR,#$90    ;Select Bank 4 by
                    ;setting FSR<7:5>
mov     $10,#$64    ;load register 10h with
                    ;the literal 64h
```

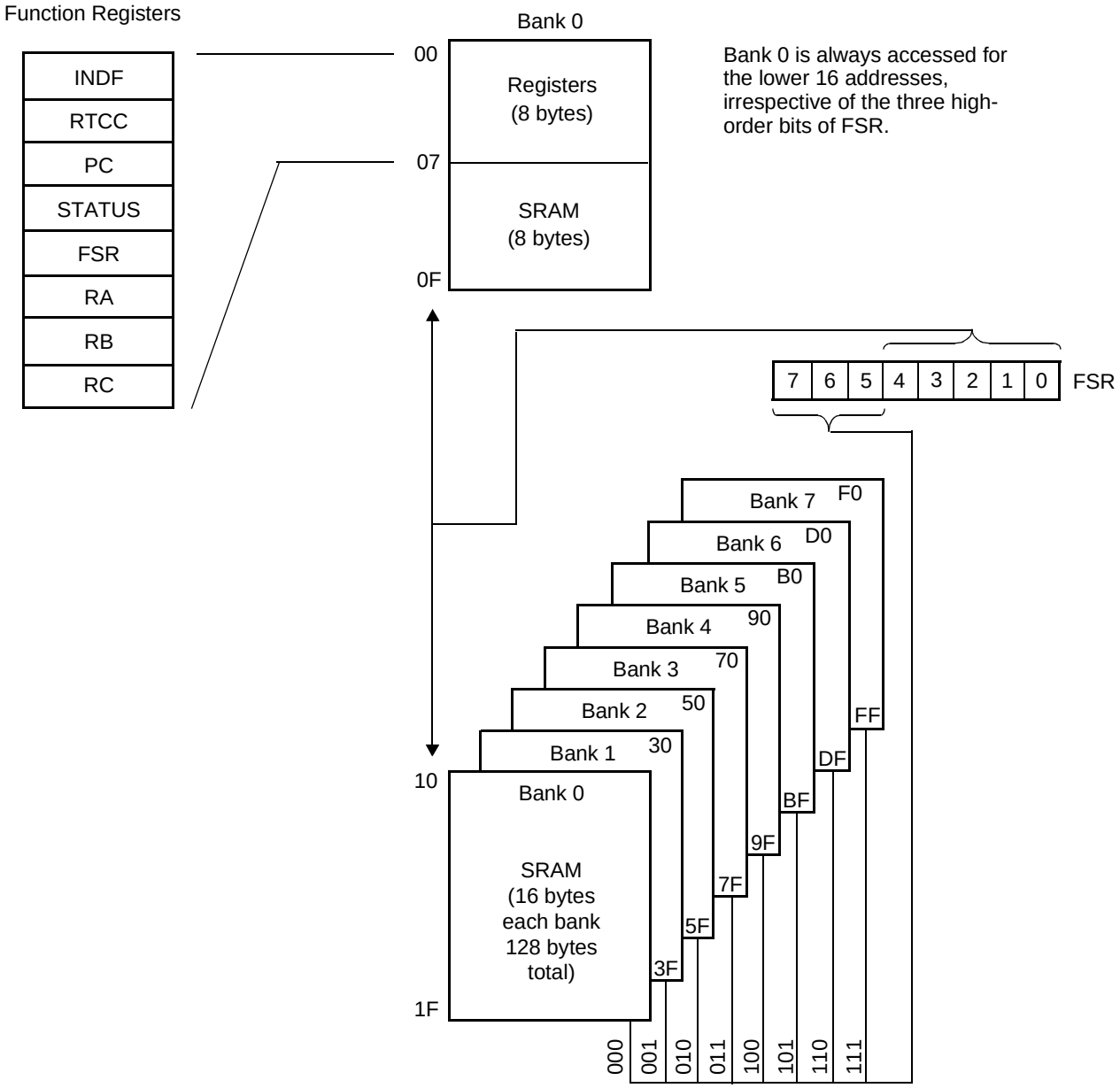


Figure 6-1. Data Memory Organization

7.0 POWER DOWN MODE

The power down mode is entered by executing the SLEEP instruction.

In power down mode, only the Watchdog Timer (WDT) is active. If the Watchdog Timer is enabled, upon execution of the SLEEP instruction, the Watchdog Timer is cleared, the TO (time out) bit is set in the STATUS register, and the PD (power down) bit is cleared in the STATUS register.

There are three different ways to exit from the power down mode: a timer overflow signal from the Watchdog Timer (WDT), a valid transition on any of the Multi-Input Wakeup pins (Port B pins), or through an external reset input on the MCLR pin.

To achieve the lowest possible power consumption, the Watchdog Timer should be disabled and the device should exit the power down mode through the Multi-Input Wakeup (MIWU) pins or an external reset.

7.1 Multi-Input Wakeup

Multi-Input Wakeup is one way of causing the device to exit the power down mode. Port B is used to support this feature. The WKEN_B register (Wakeup Enable Register) allows any Port B pin or combination of pins to cause the wakeup. Clearing a bit in the WKEN_B register enables the wakeup on the corresponding Port B pin. If multi-input wakeup is selected to cause a wakeup, the trigger condition on the selected pin can be either rising edge (low to high) or falling edge (high to low). The WKED_B register (Wakeup Edge Select) selects the desired transition edge. Setting a bit in the WKED_B register selects the falling edge on the corresponding Port B. Clearing the bit selects the rising edge. The WKEN_B and WKED_B registers are set to FFh upon reset.

Once a valid transition occurs on the selected pin, the WKPND_B register (Wakeup Pending Register) latches the transition in the corresponding bit position. A logic ‘1’ indicates the occurrence of the selected trigger edge on the corresponding Port B pin.

Upon exiting the power down mode, the Multi-Input Wakeup logic causes program counter to branch to the maximum program memory address (same as reset).

Figure 7-1 shows the Multi-Input Wakeup block diagram.

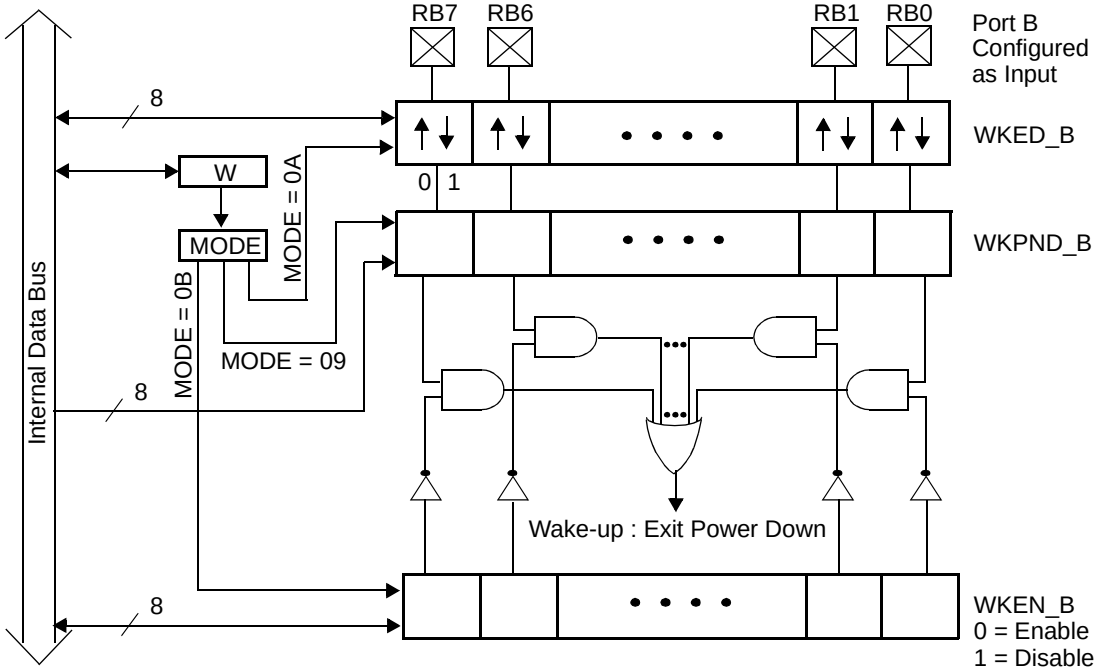


Figure 7-1. Multi-Input Wakeup Block Diagram

Table 9-2. External Component Selection for Murata Ceramic Resonators (Vdd=5.0V)

FOSC2:FOSC0	Resonator Frequency	Resonator Part Number	C1	C2	R_F	R_S
011	4 MHz	CSA4.00MG	30 pF	30 pF	1MΩ	0 Ω
011	4 MHz	CST4.00MGW	Internal (30 pF)	Internal (30 pF)	1 MΩ	0 Ω
011	4 MHz	CSTCC4.00G0H6	Internal (47 pF)	Internal (47 pF)	1 MΩ	0 Ω
011	8 MHz	CSA8.00MTZ	30 pF	30 pF	1 MΩ	0 Ω
011	8 MHz	CST8.00MTW	Internal (30 pF)	Internal 30 pF)	1 MΩ	0 Ω
011	8 MHz	CSTCC8.00MG0H6	Internal (47 pF)	Internal 47pF)	1 MΩ	0 Ω
011	20 MHz	CSA20.00MXZ040	5 pF	5 pF	1 MΩ	0 Ω
011	20 MHz	CST20.00MXW0H1	Internal (5 pF)	Internal (5 pF)	1 MΩ	0 Ω
011	20 MHz	CSACV20.00MXJ040	5 pF	5 pF	22 kΩ	0 Ω
011	20 MHz	CSTCV20.00MXJ0H1	Internal (5 pF)	Internal (5 pF)	22 kΩ	0 Ω
100	33 MHz	CSA33.00MXJ040	5 pF	5 pF	1 MΩ	0 Ω
100	33 MHz	CST33.00MXW040	Internal (5 pF)	Internal (5 pF)	1 MΩ	0 Ω
100	33 MHz	CSACV33.00MXJ040	5 pF	5 pF	1 MΩ	0 Ω
100	33 MHz	CSTCV33.00MXJ040	Internal (5 pF)	Internal (5 pF)	1 MΩ	0 Ω
101	50 MHz	CSA50.00MXZ040	15 pF	15 pF	10 kΩ	0 Ω
101	50 MHz	CST50.00MXW0H3	Internal (15 pF)	Internal (15 pF)	10 kΩ	0Ω
101	50 MHz	CSACV50.00MXJ040	15 pF	15 pF	10 kΩ	0 Ω
101	50 MHz	CSTCV50.00MXJ0H3	Internal (15 pF)	Internal (15 pF)	10 kΩ	0 Ω

9.2 External RC Mode

The external RC oscillator mode provides a cost-effective approach for applications that do not require a precise operating frequency. In this mode, the RC oscillator frequency is a function of the supply voltage, the resistor (R) and capacitor (C) values, and the operating temperature. In addition, the oscillator frequency will vary from unit to unit due to normal manufacturing process variations. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low C values. The external R and C component tolerances contribute to oscillator frequency variation as well.

Figure 9-3 shows the external RC connection diagram. The recommended R value is from 3kΩ to 100kΩ. For R values below 2.2kΩ, the oscillator may become unstable, or may stop completely. For very high R values (such as 1 MΩ), the oscillator becomes sensitive to noise, humidity, and leakage.

Although the oscillator will operate with no external capacitor (C = 0pF), it is recommended that you use values above 20 pF for noise immunity and stability. With no or small external capacitance, the oscillation frequency can vary significantly due to variation in PCB trace or package lead frame capacitances.

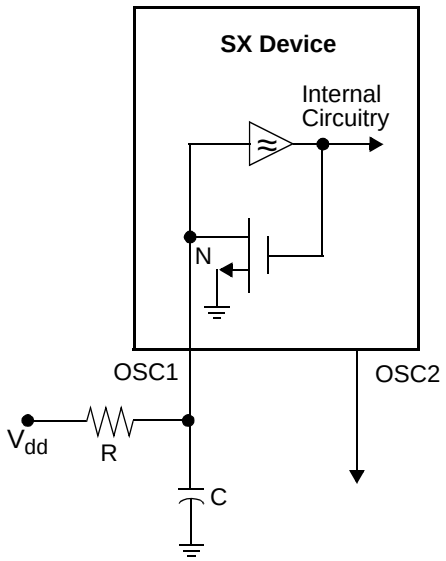


Figure 9-3. RC Oscillator Mode

9.3 Internal RC Mode

The internal RC mode uses an internal oscillator, so the device does not need any external components. At 4 MHz, the internal oscillator provides typically +/–8% accuracy over the allowed temperature range. The internal clock frequency can be divided down to provide one of eight lower-frequency choices by selecting the desired value in the FUSE Word register. The frequency range is from 31.25 KHz to 4 MHz. The default operating frequency of the internal RC oscillator may not be 4 MHz. This is due to the fact that the SX device requires trimming to obtain 4 MHz operation. The parts shipped out of the factory are not trimmed. The device relies on the programming tool provided by the third party vendors to support trimming.

10.0 REAL TIME CLOCK (RTCC)/WATCHDOG TIMER

The device contains an 8-bit Real Time Clock/Counter (RTCC) and an 8-bit Watchdog Timer (WDT). An 8-bit programmable prescaler extends the RTCC to 16 bits. If the prescaler is not used for the RTCC, it can serve as a postscaler for the Watchdog Timer. Figure 10-1 shows the RTCC and WDT block diagram.

10.1 RTCC

RTCC is an 8-bit real-time timer that is incremented once each instruction cycle or from a transition on the RTCC pin. The on-board prescaler can be used to extend the RTCC counter to 16 bits.

The RTCC counter can be clocked by the internal instruction cycle clock or by an external clock source presented at the RTCC pin.

To select the internal clock source, bit 5 of the OPTION register should be cleared. In this mode, RTCC is incremented at each instruction cycle unless the prescaler is selected to increment the counter.

To select the external clock source, bit 5 of the OPTION register must be set. In this mode, the RTCC counter is incremented with each valid signal transition at the RTTC pin. By using bit 4 of the OPTION register, the transition can be programmed to be either a falling edge or rising edge. Setting the control bit selects the falling edge to increment the counter. Clearing the bit selects the rising edge.

The RTCC generates an interrupt as a result of an RTCC rollover from 0FF to 000. There is no interrupt pending bit to indicate the overflow occurrence. The RTCC register must be sampled by the program to determine any overflow occurrence.

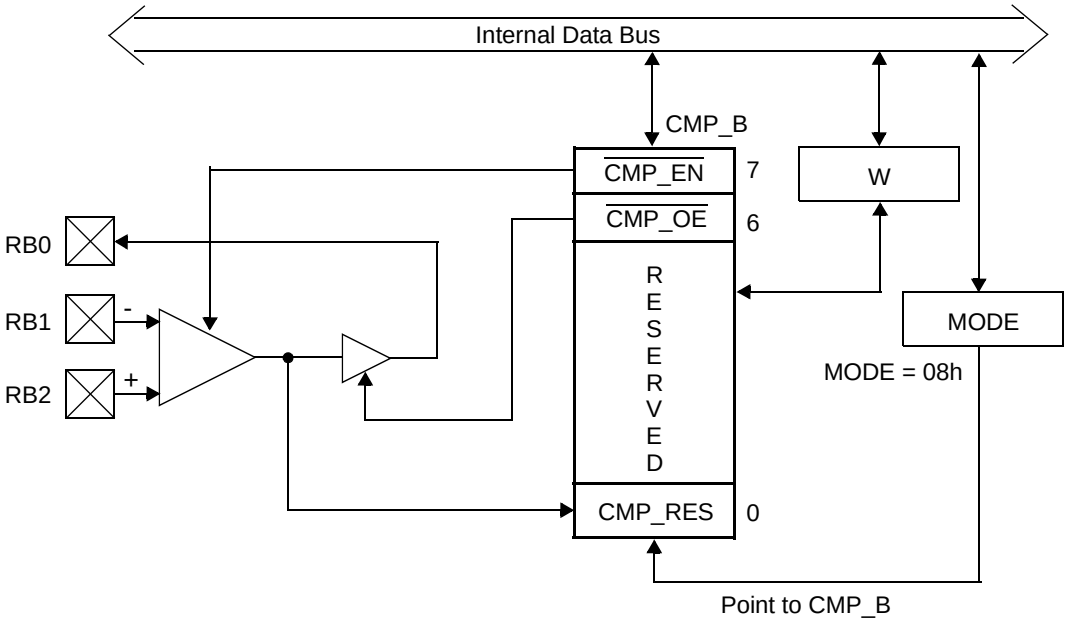


Figure 11-1. Comparator Block Diagram

16.1 Equivalent Assembler Mnemonics

Some assemblers support additional instruction mnemonics that are special cases of existing instructions or alternative mnemonics for standard ones. For example, an assembler might support the mnemonic “CLC” (clear carry), which is interpreted the same as the instruction “clrb $03.0” (clear bit 0 in the STATUS register). Some of the commonly supported equivalent assembler mnemonics are described in Table 16-2.

Table 16-2. Equivalent Assembler Mnemonics

Syntax	Description	Equivalent	Cycles
CLC	Clear Carry bit	CLRB $03.0	1
CLZ	Clear Zero bit	CLRB $03.2	1
JMP W	Jump Indirect W	MOV $02,W	4 or 3 (note 1)
JMP PC+W	Jump Indirect W Relative	ADD $02,W	4 or 3 (note 1)
MODE imm4	Move Immediate to MODE Register	MOV M,#lit	1
NOT W	Complement W	XOR W,#$FF	1
SC	Skip if Carry bit Set	SB $03.0	1 or 2 (note 2)
SKIP	Skip Next Instruction	SNB $02.0 or SB $02.0	4 or 2 (note 3)

Note 1: The JMP W or JMP PC+W instruction takes 4 cycles in the “compatible” clocking mode or 3 cycles in the “turbo” clocking mode.

Note 2: The SC instruction takes 1 cycle if the tested condition is false or 2 cycles if the tested condition is true.

Note 3: The assembler converts the SKIP instruction into a SNB or SB instruction that tests the least significant bit of the program counter, choosing SNB or SB so that the tested condition is always true. The instruction takes 4 cycles in the “compatible” clocking mode or 2 cycles in the “turbo” clocking mode.

17.2 DC Characteristics

SX20/28AC at 75MHz(Temp Range: 0°C <= Ta <= +70°C)

SX20/28AC at 50MHz (Temp Range: -40°C <= Ta <= +85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{dd}	Supply Voltage (Note 1)	F_{osc}= 32 MHz F_{osc}= 50 MHz F_{osc}= 75 MHz	2.7 3.0 4.5	- - -	5.5 5.5 5.5	V V V
S_{Vdd}	V_{dd} rise rate (Note 1)		0.05	-	-	V/ms
I_{dd}	Supply Current, active	V_{dd} = 5.0V, F_{osc} = 75 MHz (External OSC) V_{dd} = 5.0V, F_{osc} = 50 MHz (Crystal) V_{dd} = 5.0V, F_{osc} = 4 MHz (Crystal) V_{dd} = 2.7V, F_{osc} = 20 MHz (Crystal)	- - - -	100 77 7.5 17	105 82 8 18	mA mA mA mA
I_{pd}	Supply Current, power down	V_{dd} = 3.0V, WDT enabled (before timeout) V_{dd} = 3.0V, WDT disabled V_{dd} = 4.5V, WDT enabled V_{dd} = 4.5V, WDT disabled	-	10 1.0	20 9.0 110 100	µA µA µA µA
V_{ih}, V_{il}	Input Levels $\overline{MCLR}$, OSC1, RTCC Logic High Logic Low All Other Inputs CMOS Logic High Logic Low TTL Logic High Logic Low		 0.8V_{dd} V_{ss} 0.7V_{dd} V_{ss} 2.0 V_{ss}		 V_{dd} 0.2V_{dd} V_{dd} 0.3V_{dd} V_{dd} 0.8	 V V V V V V
I_{il}	Input Leakage Current	V_{in} = V_{dd} or V_{ss}	-1.0		+1.0	µA
I_{ip}	Weak Pullup Current	V_{dd} = 5.5V, V_{in} = 0V V_{dd} = 3.0V, V_{in} = 0V	100 25		190 50	µA µA
V_{oh}	Output High Voltage Ports B, C Port A	 Ioh = 20mA, Vdd = 4.5V Ioh = 12mA, Vdd = 3.0V Ioh = 30mA, Vdd = 4.5 Ioh = 20mA, Vdd = 3.0V	 Vdd-0.7 Vdd-0.7 Vdd-0.7 Vdd-0.7		 	 V V V V
V_{ol}	Output Low Voltage All Ports	Iol = 30mA, Vdd = 4.5V Iol = 20mA, Vdd = 3.0V			0.6 0.6	V V

Note 1: Vdd must start rising from Vss to ensure proper Power-On-Reset when relying on the internal Power-On-Reset circuitry.

17.3 AC Characteristics

SX20/28AC at 75MHz(Temp Range: 0°C <= Ta <= +70°C)

SX20/28AC at 50MHz (Temp Range: -40°C <= Ta <= +85°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
F_{osc}	External CLKIN Frequency	DC	-	32 1.0 4.0 10 24 50 75	KHz MHz MHz MHz MHz MHz MHz	LP1 LP2 RC XT1 XT2 HS1/HS2/HS3 HS3
	Oscillator Frequency	DC 0.032 DC 0.032 1.0 1.0 1.0	-	32 1.0 4.0 10.0 24.0 50 75	KHz MHz MHz MHz MHz MHz MHz	LP1 LP2 RC XT1 XT2 HS1/HS2/HS3 HS3
T_{osc}	External CLKIN Period	31.25 1.0 250 100 41.7 20 13.3	-	-	µs µs ns ns ns ns	LP1 LP2 RC XT1 XT2 HS1/HS2/HS3
	Oscillator Period	31.25 1.0 250 0.1 41.7 20 13.3	-	- 31.25 - 31.25 1000.0 1000.0 -	µs µs µs µs ns ns ns	LP1 LP2 RC XT1 XT2 HS1/HS2/HS3 HS3
T_{osL}, T_{osH}	Clock in (OSC1) Low or High Time	2.0 50 8.0 5.3	-	-	µs ns ns ns	LP1/LP2 XT1/XT2 HS1/HS2/HS3 HS3

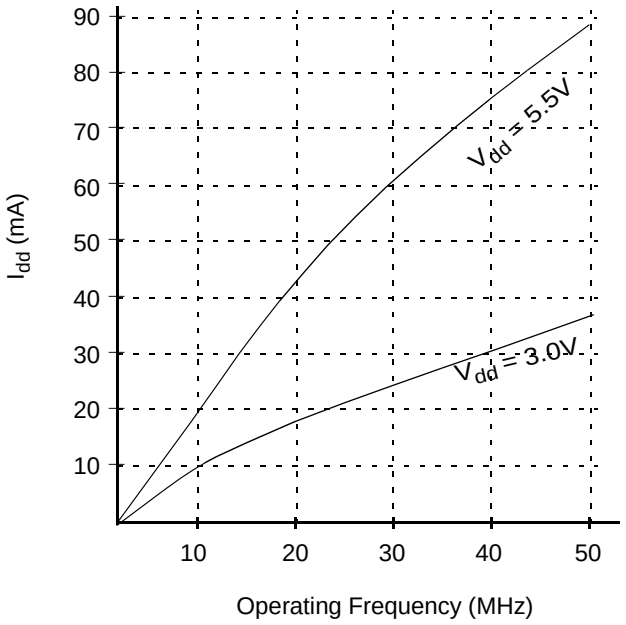
Note: Data in the Typical (“TYP”) column is at 25°C unless otherwise stated.

17.4 Comparator DC and AC Specifications (50 MHz and 75 MHz Operation)

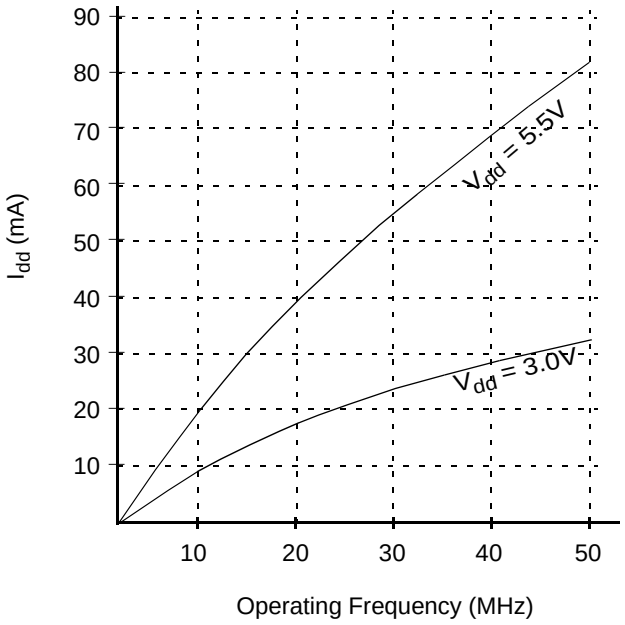
Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	0.4V < Vin < Vdd – 1.5V		+/- 10	+/- 25	mV
Input Common Mode Voltage Range		0.4		Vcc – 1.3	V
Voltage Gain			300k		V/V
DC Supply Current (enabled)	Vdd = 5.5V			120	µA
Response Time	$V_{overdrive}$ = 25mV			250	ns

17.5 Typical Performance Characteristics (25°C)

Active Supply Current Vs Operating Frequency (Crystal Clock)



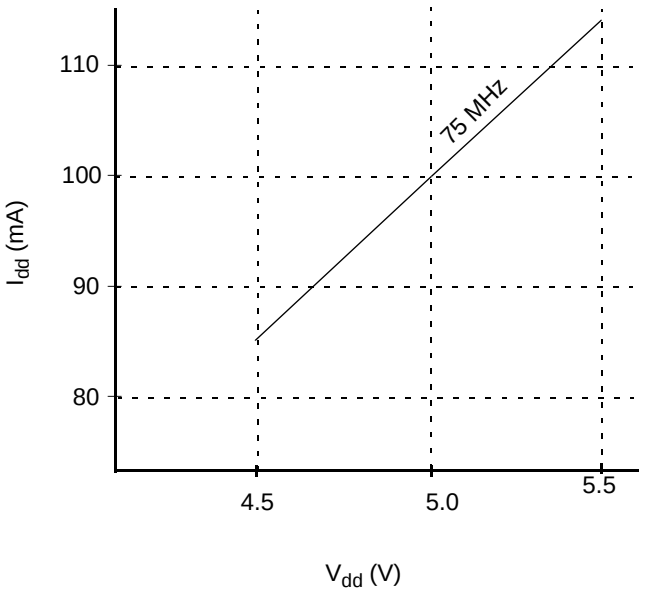
Active Supply Current Vs Operating Frequency (External Clock)



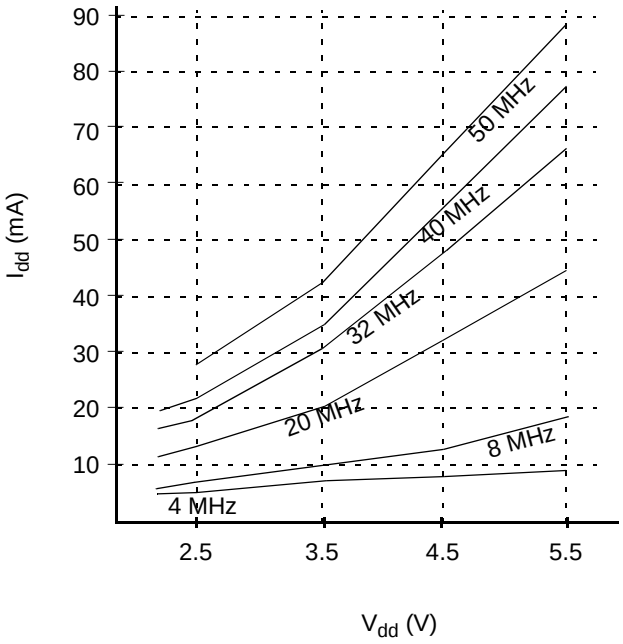
17.7 Typical Performance Characteristics (Continued)

Active Supply Current Vs Operating Frequency (External Clock)

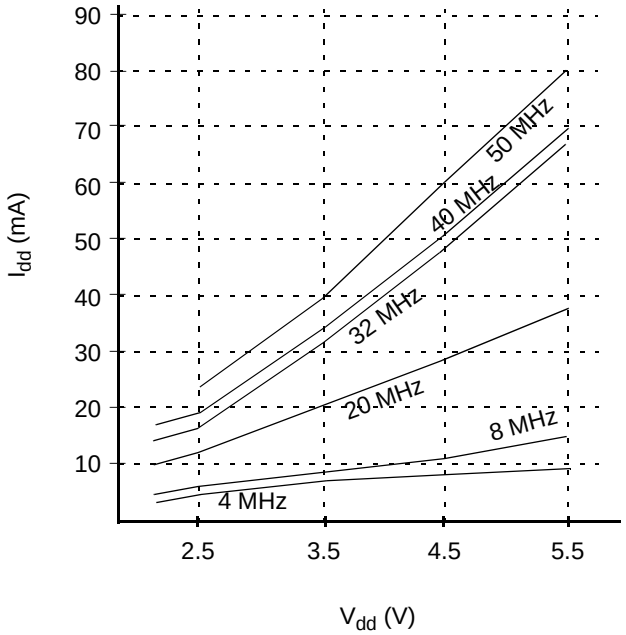
SX18AC75/SX20AC75/SX28AC75



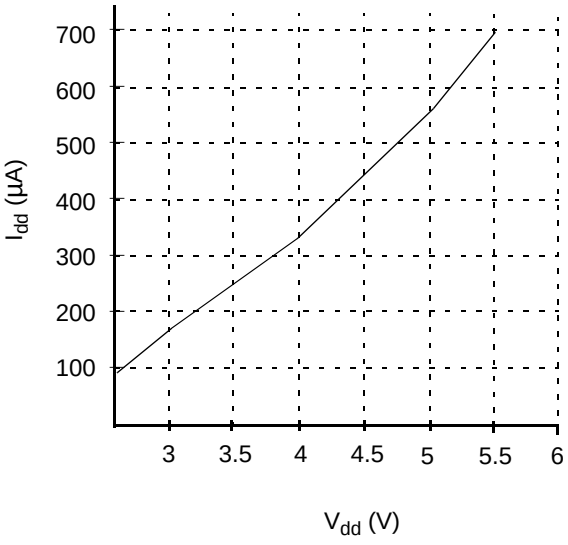
Active Supply Current Vs V_{dd} (Crystal Clock)



Active Supply Current Vs V_{dd} (External Clock)



Active Supply Current Vs V_{dd} (32 kHz Crystal Clock)



SX28AC/DP