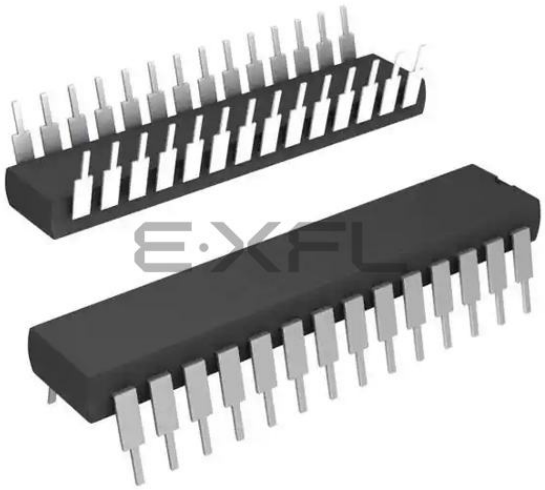


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	8-Bit
Speed	75MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	136 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/parallax/sx28ac-dp-g

Table of Contents

1.2 Key Features

50 MIPS Performance

- SX20AC/SX28AC: DC - 75 MHz
- SX20AC/SX28AC: 13.3 ns instruction cycle, 39.9 ns internal interrupt response
- 1 instruction per clock (branches 3)

EE/FLASH Program Memory and SRAM Data Memory

- Access time of < 13.3 ns provides single cycle access
- EE/Flash rated for > 10,000 rewrite cycles
- 2048 Words EE/Flash program memory
- 136x8 bits SRAM data memory

CPU Features

- Compact instruction set
- All instructions are single cycle except branch
- Eight-level push/pop hardware stack for subroutine linkage
- Fast table lookup capability through run-time readable code (IREAD instruction)
- Totally predictable program execution flow for hard real-time applications

Fast and Deterministic Interrupt

- Jitter-free 3-cycle internal interrupt response
- Hardware context save/restore of key resources such as PC, W, STATUS, and FSR within the 3-cycle interrupt response time
- External wakeup/interrupt capability on Port B (8 pins)

Flexible I/O

- All pins individually programmable as I/O
- Inputs are TTL or CMOS level selectable
- All pins have selectable internal pull-ups
- Selectable Schmitt Trigger inputs on Ports B, and C
- All outputs capable of sourcing/sinking 30 mA
- Port A outputs have symmetrical drive
- Analog comparator support on Port B (RB0 OUT, RB1 IN-, RB2 IN+)
- Selectable I/O operation synchronous to the oscillator clock

Hardware Peripheral Features

- One 8-bit Real Time Clock/Counter (RTCC) with programable 8-bit prescaler
- Watchdog Timer (shares the RTCC prescaler)
- Analog comparator
- Brown-out detector
- Multi-Input Wakeup logic on 8 pins
- Internal RC oscillator with configurable rate from 31.25 kHz to 4 MHz
- Power-On-Reset

Packages

- 20-pin SSOP, 28-pin DIP/SSOP

Programming and Debugging Support

- On- chip in-system programming support with serial and parallel interfaces
- In-system serial programming via oscillator pins
- On-chip in-System debugging support logic
- Real-time emulation, full program debug, and integrated development environment offered by third party tool vendors

2.3 Part Numbering

Table 2-1. Ordering Information

Device	Pins	I/O	Operating Frequency (MHz)	EE/Flash (Words)	RAM (Bytes)	Operating Temp. (°C)
SX20AC/SS	20	12	50	2K	136	-40°C to +85°C
SX20AC/SS	20	12	75	2K	136	0°C to +70°C
SX28AC/DP	28	20	50	2K	136	-40°C to +85°C
SX28AC/DP	28	20	75	2K	136	0°C to +70°C
SX28AC/SS	28	20	50	2K	136	-40°C to +85°C
SX28AC/SS	28	20	75	2K	136	0°C to +70°C

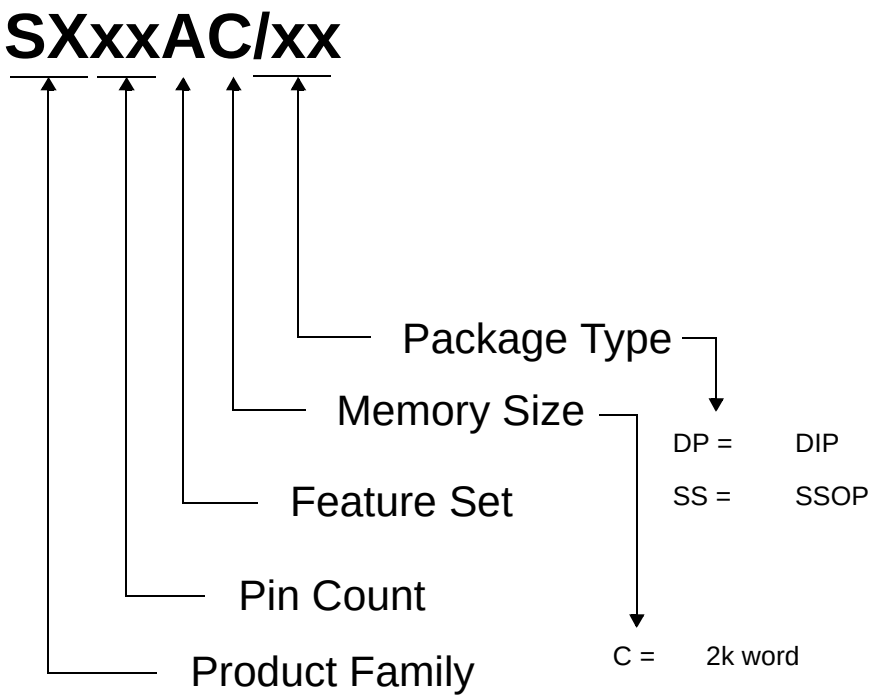


Figure 2-1. Part Number Reference Guide

3.0 PORT DESCRIPTIONS

The device contains a 4-bit I/O port (Port A) and two 8-bit I/O ports (Port B, Port C). Port A provides symmetrical drive capability. Each port has three associated 8-bit registers (Direction, Data, TTL/CMOS Select, and Pull-Up Enable) to configure each port pin as Hi-Z input or output, to select TTL or CMOS voltage levels, and to enable/disable the weak pull-up resistor. The upper four bits of the registers associated with Port A are not used. The least significant bit of the registers corresponds to the least significant port pin. To access these registers, an appropriate value must be written into the MODE register.

Upon power-up, all bits in these registers are initialized to "1".

The associated registers allow for each port bit to be individually configured under software control as shown below:

Table 3-1. Port Configuration

Data Direction Registers: RA, RB, RC		TTL/CMOS Select Registers: LVL_A, LVL_B, LVL_C		Pullup Enable Registers: PLP_A, PLP_B, PLP_C	
0	1	0	1	0	1
Output	Hi-Z Input	CMOS	TTL	Enable	Disable

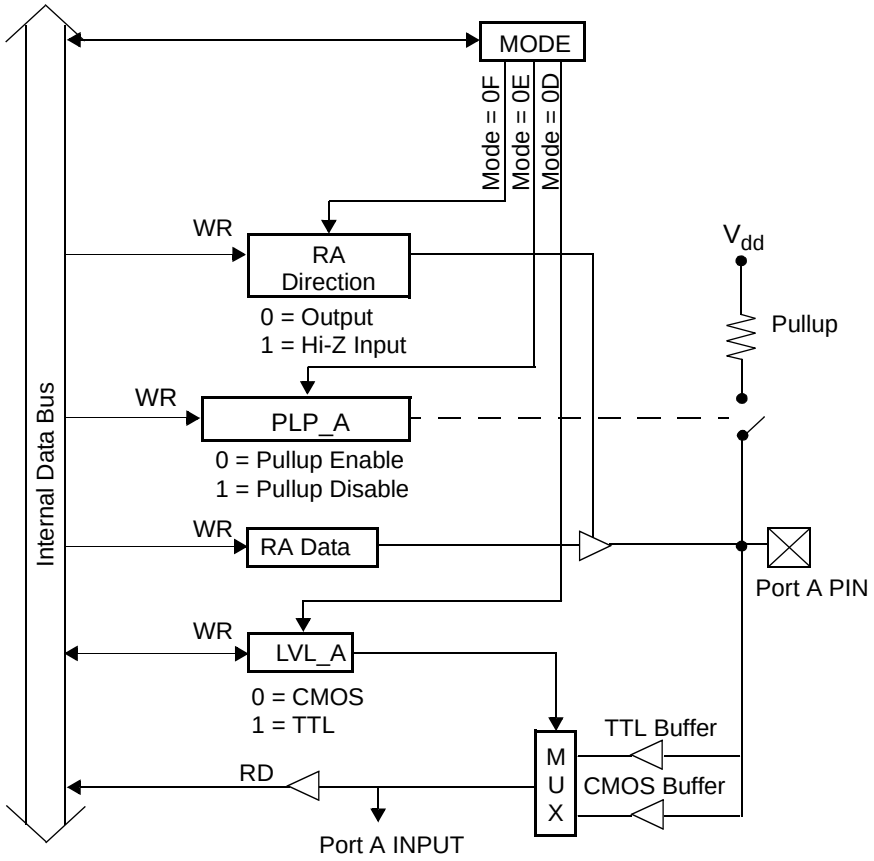


Figure 3-1. Port A Configuration

3.1 Reading and Writing the Ports

The three ports are memory-mapped into the data memory address space. To the CPU, the three ports are available as the RA, RB, and RC file registers at data memory addresses 05h, 06h, and 07h, respectively.

Writing to a port data register sets the voltage levels of the corresponding port pins that have been configured to operate as outputs. Reading from a register reads the voltage levels of the corresponding port pins that have been configured as inputs.

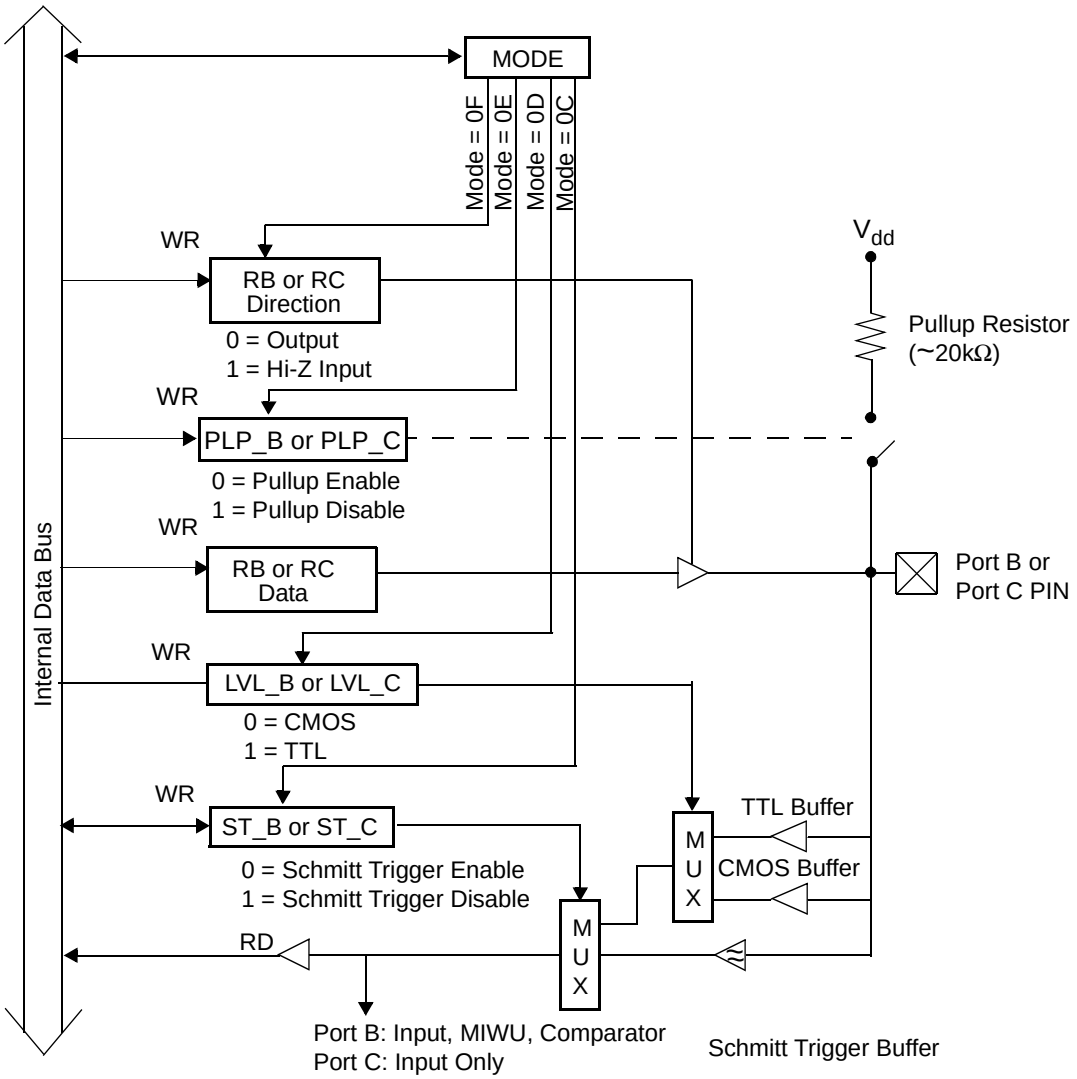


Figure 3-2. Port B, Port C Configuration

For example, suppose all four Port A pins are configured as outputs and with RA0 and RA1 to be high, and RA2 and RA3 to be low:

```
mov   W,#$03    ;load W with the value 03h
                ;(bits 0 and 1 high)
mov   $05,W     ;write 03h to Port A data
                ;register
```

The second “mov” instruction in this example writes the Port A data register (RA), which controls the output levels of the four Port A pins, RA0 through RA3. Because Port A has only four I/O pins, only the four least significant bits of this register are used. The four high-order register bits are “don’t care” bits. Port B and Port C are both eight bits wide, so the full widths of the RB and RC registers are used.

When a write is performed to a bit position for a port that has been configured as an input, a write to the port data register is still performed, but it has no immediate effect on the pin. If later that pin is configured to operate as an output, it will reflect the value that has been written to the data register.

When a read is performed from a bit position for a port, the operation is actually reading the voltage level on the pin itself, not necessarily the bit value stored in the port data register. This is true whether the pin is configured to operate as an input or an output. Therefore, with the pin configured to operate as an input, the data register contents have no effect on the value that you read. With the pin configured to operate as an output, what is read generally matches what has been written to the register.

4.0 SPECIAL-FUNCTION REGISTERS

The CPU uses a set of special-function registers to control the operation of the device.

The CPU registers include an 8-bit working register (W), which serves as a pseudo accumulator. It holds the second operand of an instruction, receives the literal in immediate type instructions, and also can be program-selected as the destination register.

A set of 31 file registers serves as the primary accumulator. One of these registers holds the first operand of an instruction and another can be program-selected as the destination register. The first eight file registers include the Real-Time Clock/Counter register (RTCC), the lower eight bits of the 11-bit Program Counter (PC), the 8-bit STATUS register, three port control registers for Port A, Port B, Port C, the 8-bit File Select Register (FSR), and INDF used for indirect addressing.

The five low-order bits of the FSR register select one of the 31 file registers in the indirect addressing mode. Calling for the file register located at address 00h (INDF) in any of the file-oriented instructions selects indirect addressing, which uses the FSR register. It should be noted that the file register at address 00h is not a physically implemented register. The CPU also contains an 8-level, 11-bit hardware push/pop stack for subroutine linkage.

Table 4-1. Special-Function Registers

Addr	Name	Function
00h	INDF	Used for indirect addressing
01h	RTCC	Real Time Clock/Counter
02h	PC	Program Counter (low byte)
03h	STATUS	Holds Status bits of ALU
04h	FSR	File Select Register
05h	RA	Port RA Control register
06h	RB	Port RB Control register
07h	RC*	Port RC Control register

*In the SX18 package, Port C is not used, and address 07h is available as a general-purpose RAM location.

4.1 PC Register (02h)

The PC register holds the lower eight bits of the program counter. It is accessible at run time to perform branch operations.

4.2 STATUS Register (03h)

The STATUS register holds the arithmetic status of the ALU, the page select bits, and the reset state. The STATUS register is accessible during run time, except that bits PD and TO are read-only. It is recommended that only SETB and CLRB instructions be used on this register. Care should be exercised when writing to the STATUS register as the ALU status bits are updated upon completion of the write operation, possibly leaving the STATUS register with a result that is different than intended.

PA2	PA1	PA0	TO	PD	Z	DC	C
Bit 7							**Bit 0**

Bit 7-5: Page select bits PA2:PA0

000 = Page 0 (000h – 01FFh)

001 = Page 1 (200h – 03FFh)

010 = Page 2 (400h – 05FFh)

011 = Page 3 (600h – 07FFh)

Bit 4: Time Out bit, TO

1 = Set to 1 after power up and upon execution of CLRWDT or SLEEP instructions

0 = A watchdog time-out occurred

Bit 3: Power Down bit, PD

1= Set to a 1 after power up and upon execution of the CLRWDT instruction

0 = Cleared to a ‘0’ upon execution of SLEEP instruction

Bit 2: Zero bit, Z

1 = Result of math operation is zero

0 = Result of math operation is non-zero

Bit 1: Digit Carry bit, DC

After Addition:

1 = A carry from bit 3 occurred

0 = No carry from bit 3 occurred

After Subtraction:

1 = No borrow from bit 3 occurred

0 = A borrow from bit 3 occurred

Bit 0: Carry bit, C

After Addition:

1 = A carry from bit 7 of the result occurred

0 = No carry from bit 7 of the result occurred

After Subtraction:

1 = No borrow from bit 7 of the result occurred

0 = A borrow from bit 7 of the result occurred

Rotate (RR or RL) Instructions:

The carry bit is loaded with the low or high order bit, respectively. When CF bit is cleared, Carry bit works as input for ADD and SUB instructions.

7.0 POWER DOWN MODE

The power down mode is entered by executing the SLEEP instruction.

In power down mode, only the Watchdog Timer (WDT) is active. If the Watchdog Timer is enabled, upon execution of the SLEEP instruction, the Watchdog Timer is cleared, the TO (time out) bit is set in the STATUS register, and the PD (power down) bit is cleared in the STATUS register.

There are three different ways to exit from the power down mode: a timer overflow signal from the Watchdog Timer (WDT), a valid transition on any of the Multi-Input Wakeup pins (Port B pins), or through an external reset input on the MCLR pin.

To achieve the lowest possible power consumption, the Watchdog Timer should be disabled and the device should exit the power down mode through the Multi-Input Wakeup (MIWU) pins or an external reset.

7.1 Multi-Input Wakeup

Multi-Input Wakeup is one way of causing the device to exit the power down mode. Port B is used to support this feature. The WKEN_B register (Wakeup Enable Register) allows any Port B pin or combination of pins to cause the wakeup. Clearing a bit in the WKEN_B register enables the wakeup on the corresponding Port B pin. If multi-input wakeup is selected to cause a wakeup, the trigger condition on the selected pin can be either rising edge (low to high) or falling edge (high to low). The WKED_B register (Wakeup Edge Select) selects the desired transition edge. Setting a bit in the WKED_B register selects the falling edge on the corresponding Port B. Clearing the bit selects the rising edge. The WKEN_B and WKED_B registers are set to FFh upon reset.

Once a valid transition occurs on the selected pin, the WKPND_B register (Wakeup Pending Register) latches the transition in the corresponding bit position. A logic ‘1’ indicates the occurrence of the selected trigger edge on the corresponding Port B pin.

Upon exiting the power down mode, the Multi-Input Wakeup logic causes program counter to branch to the maximum program memory address (same as reset).

Figure 7-1 shows the Multi-Input Wakeup block diagram.

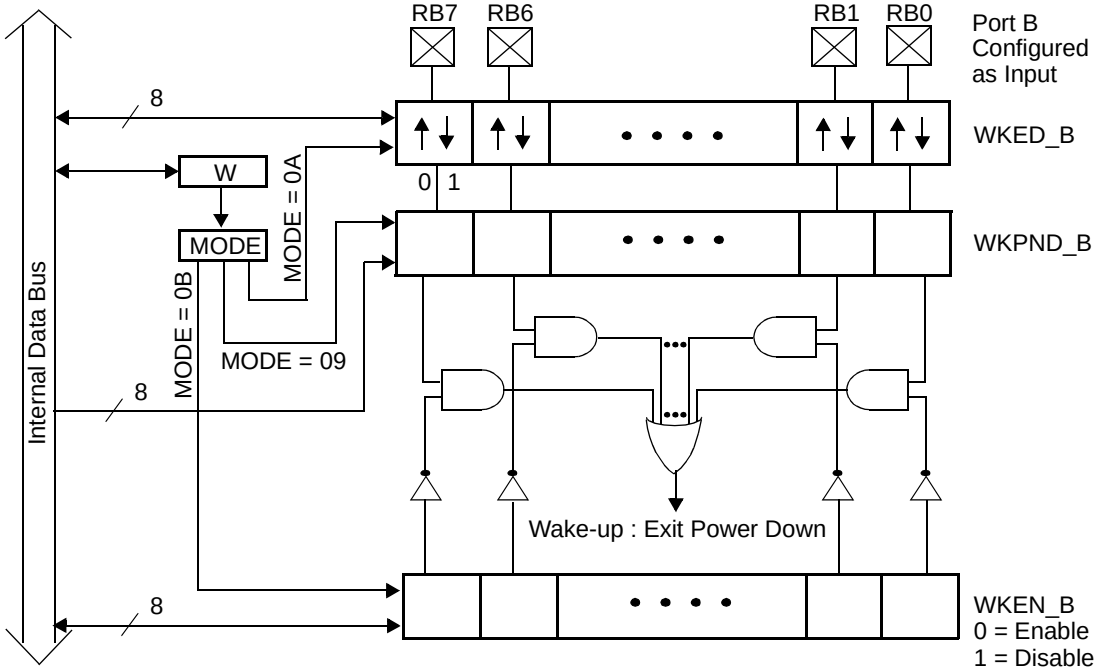


Figure 7-1. Multi-Input Wakeup Block Diagram

7.2 Port B MIWU/Interrupt Configuration

The WKPND_B register comes up with a random value upon reset. The user program must clear the register prior to enabling the wake-up condition or interrupts. The proper initialization sequence is:

1. Select the desired edge (through WKED_B register).
2. Clear the WKPND_B register.
3. Enable the Wakeup condition (through WKEN_B register).

Below is an example of how to read the WKPND_B register to determine which Port B pin caused the wakeup or interrupt, and to clear the WKPND_B register:

```
mov   M,#$09
clr   W
mov   !RB,W    ;W contains WKPND_B
               ;contents of W exchanged
               ;with contents of WKPND_B
```

The final “mov” instruction in this example performs an exchange of data between the working register (W) and the WKPND_B register. This exchange occurs only with Port B accesses. Otherwise, the “mov” instruction does not perform an exchange, but only moves data from the source to the destination.

Here is an example of a program segment that configures the RB0, RB1, and RB2 pins to operate as Multi-Input Wakeup/Interrupt pins, sensitive to falling edges:

```
mov M,#$0F  ;prepare to write port data
            ;direction registers
mov W,#$07  ;load W with the value 07h
mov !RB,W   ;configure RB0-RB2 to be inputs

mov M,#$0A  ;prepare to write WKED_B
            ;(edge) register
            ;W contains the value 07h
mov !RB,W   ;configure RB0-RB2 to sense
            ;falling edges
mov M,#$09  ;prepare to access WKPND_B
            ;(pending) register
mov W,#$00  ;clear W
mov !RB,W   ;clear all wakeup pending bits

mov M,#$0B  ;prepare to write WKEN_B (enable)
            ;register
mov W,#$F8h ;load W with the value F8h
mov !RB,W   ;enable RB0-RB2 to operate as
            ;wakeup inputs
```

To prevent false interrupts, the enabling step (clearing bits in WKEN_B) should be done as the last step in a sequence of Port B configuration steps. After this program segment is executed, the device can receive interrupts on the RB0, RB1, and RB2 pins. If the device is put into the power down mode (by executing the SLEEP instruction), the device can then receive wakeup signals on those same pins.

Table 9-2. External Component Selection for Murata Ceramic Resonators (Vdd=5.0V)

FOSC2:FOSC0	Resonator Frequency	Resonator Part Number	C1	C2	R_F	R_S
011	4 MHz	CSA4.00MG	30 pF	30 pF	1MΩ	0 Ω
011	4 MHz	CST4.00MGW	Internal (30 pF)	Internal (30 pF)	1 MΩ	0 Ω
011	4 MHz	CSTCC4.00G0H6	Internal (47 pF)	Internal (47 pF)	1 MΩ	0 Ω
011	8 MHz	CSA8.00MTZ	30 pF	30 pF	1 MΩ	0 Ω
011	8 MHz	CST8.00MTW	Internal (30 pF)	Internal 30 pF)	1 MΩ	0 Ω
011	8 MHz	CSTCC8.00MG0H6	Internal (47 pF)	Internal 47pF)	1 MΩ	0 Ω
011	20 MHz	CSA20.00MXZ040	5 pF	5 pF	1 MΩ	0 Ω
011	20 MHz	CST20.00MXW0H1	Internal (5 pF)	Internal (5 pF)	1 MΩ	0 Ω
011	20 MHz	CSACV20.00MXJ040	5 pF	5 pF	22 kΩ	0 Ω
011	20 MHz	CSTCV20.00MXJ0H1	Internal (5 pF)	Internal (5 pF)	22 kΩ	0 Ω
100	33 MHz	CSA33.00MXJ040	5 pF	5 pF	1 MΩ	0 Ω
100	33 MHz	CST33.00MXW040	Internal (5 pF)	Internal (5 pF)	1 MΩ	0 Ω
100	33 MHz	CSACV33.00MXJ040	5 pF	5 pF	1 MΩ	0 Ω
100	33 MHz	CSTCV33.00MXJ040	Internal (5 pF)	Internal (5 pF)	1 MΩ	0 Ω
101	50 MHz	CSA50.00MXZ040	15 pF	15 pF	10 kΩ	0 Ω
101	50 MHz	CST50.00MXW0H3	Internal (15 pF)	Internal (15 pF)	10 kΩ	0Ω
101	50 MHz	CSACV50.00MXJ040	15 pF	15 pF	10 kΩ	0 Ω
101	50 MHz	CSTCV50.00MXJ0H3	Internal (15 pF)	Internal (15 pF)	10 kΩ	0 Ω

10.2 Watchdog Timer

The watchdog logic consists of a Watchdog Timer which shares the same 8-bit programmable prescaler with the RTCC. The prescaler actually serves as a postscaler if used in conjunction with the WDT, in contrast to its use as a prescaler with the RTCC.

10.3 The Prescaler

The 8-bit prescaler may be assigned to either the RTCC or the WDT through the PSA bit (bit 3 of the OPTION register). Setting the PSA bit assigns the prescaler to the WDT. If assigned to the WDT, the WDT clocks the prescaler and the prescaler divide rate is selected by the PS0, PS1, and PS2 bits located in the OPTION register. Clearing the PSA bit assigns the prescaler to the RTCC. Once assigned to the RTCC, the prescaler clocks the RTCC and the divide rate is selected by the PS0, PS1, and PS2 bits in the OPTION register. The prescaler is not mapped into the data memory, so run-time access is not possible.

The prescaler cannot be assigned to both the RTCC and WDT simultaneously.

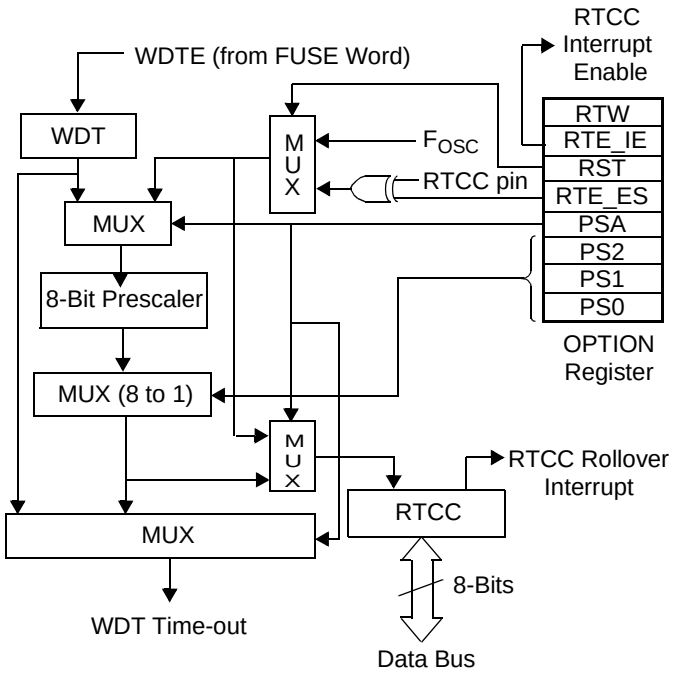


Figure 10-1. RTCC and WDT Block Diagram

11.0 COMPARATOR

The device contains an on-chip differential comparator. Ports RB0-RB2 support the comparator. Ports RB1 and RB2 are the comparator negative and positive inputs, respectively, while Port RB0 serves as the comparator output pin. To use these pins in conjunction with the comparator, the user program must configure Ports RB1 and RB2 as inputs and Port RB0 as an output. The CMP_B register is used to enable the comparator, to read the output of the comparator internally, and to enable the output of the comparator to the comparator output pin.

The comparator enable bits are set to “1” upon reset, thus disabling the comparator. To avoid drawing additional current during the power down mode, the comparator should be disabled before entering the power down mode. Here is an example of how to setup the comparator and read the CMP_B register.

```
mov  M,#$08   ;set MODE register to access
              ;CMP_B
mov  W,#$00   ;clear W
mov  !RB,W    ;enable comparator and its
              ;output
...           ;delay after enabling
              ;comparator for response
mov  M,#$08   ;set MODE register to access
              ;CMP_B
mov  W,#$00   ;clear W
mov  !RB,W    ;enable comparator and its
              ;output and also read CMP_B
              ;(exchange W and CMB_B)
and  W,#$01   ;set/clear Z bit based on
              ;comparator result
snb  $03.2    ;test Z bit in STATUS reg
              ;(0 => RB2<RB1)
jmp  rb2_hi   ;jump only if RB2>RB1
...
```

The final “mov” instruction in this example performs an exchange of data between the working register (W) and the CMP_B register. This exchange occurs only with Port B accesses. Otherwise, the “mov” instruction does not perform an exchange, but only moves data from the source to the destination.

Figure 11-1 shows the comparator block diagram.

CMP_B - Comparator Enable/Status Register

$\overline{\text{CMP\_EN}}$	$\overline{\text{CMP\_OE}}$	Reserved	CMP_RES
Bit 7	Bit 6	Bits 5–1	Bit 0

CMP_RES	Comparator result: 1 for RB2>RB1 or 0 for RB2<RB1. Comparator must be enabled (CMP_EN = 0) to read the result. The result can be read whether or not the CMP_OE bit is cleared.
$\overline{\text{CMP\_OE}}$	When cleared to 0, enables the comparator output to the RB0 pin.
$\overline{\text{CMP\_EN}}$	When cleared to 0, enables the comparator.

Figure 12-3 shows the on-chip Power-On Reset sequence where the MCLR and V_{dd} pins are tied together. The V_{dd} signal is stable before the DRT time-out period expires. In this case, the device will receive a proper reset. However, Figure 12-4 depicts a situation where V_{dd} rises too slowly. In this scenario, the DRT will time-out prior to V_{dd} reaching a valid operating voltage level (V_{dd} min). This means the device will come out of reset and start operating with the supply voltage not at a valid level. In this situation, it is recommended that you use the external RC circuit shown in Figure 12-5. The RC delay should exceed the time period it takes V_{dd} to reach a valid operating voltage

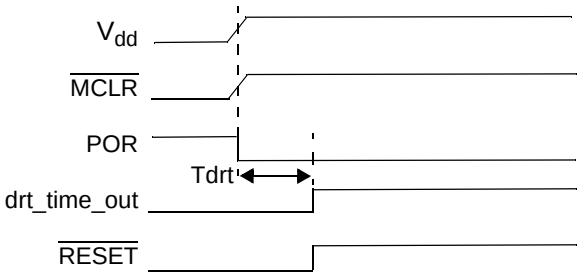


Figure 12-3. Time-out Sequence on Power-up (MCLR tied to V_{dd}): Fast V_{dd} Rise Time

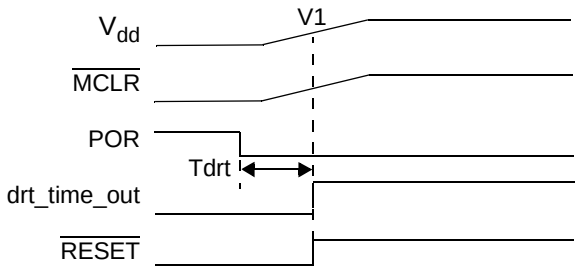


Figure 12-4. Time-out Sequence on Power-up (MCLR tied to V_{dd}): Slow Rise Time

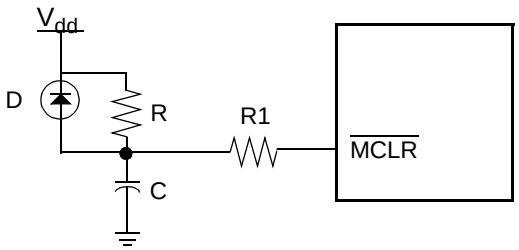


Figure 12-5. External Power-On Reset Circuit (For Slow V_{dd} Power-up)

Note 1: The external Power-On Reset circuit is required only if V_{dd} power-up is too slow. The diode D helps discharge the capacitor quickly when V_{dd} powers down.

Note 2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specifications.

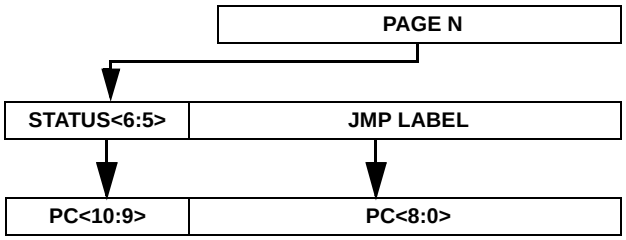
Note 3: R1 = 100Ω to 1kΩ will limit any current flowing into MCLR from external capacitor C. This helps prevent MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

13.0 BROWN-OUT DETECTOR

The on-chip brown-out detection circuitry resets the device when V_{dd} dips below the specified brown-out voltage. The device is held in reset as long as V_{dd} stays below the brown-out voltage. The device will come out of reset when V_{dd} rises above the brown-out voltage. The brown-out level is preset to approximately 4.2V at the factory. The brown-out circuit can be disabled through BOR0 and BOR1 bits contained in the FUSEX Word register.

15.10.2 Page Jump Operation

When a JMP instruction is executed and the intended destination is on a different page, the page select bits must be initialized with appropriate values to point to the desired page before the jump occurs. This can be done easily with SETB and CLRB instructions or by writing a value to the STATUS register. The device also has the PAGE instruction, which automatically selects the page in a single-cycle execution.



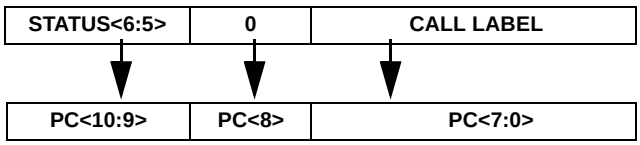
Note: “N” must be 0, 1, 2, or 3.

15.10.3 Call Operation

The following happens when a CALL instruction is executed:

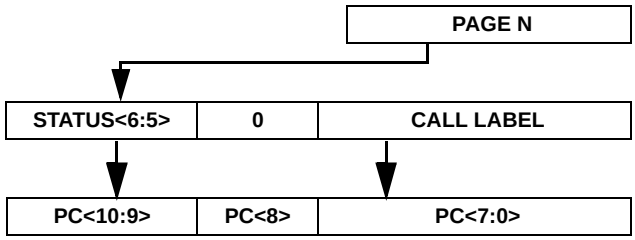
- The current value of the program counter is incremented and pushed onto the top of the stack.
- The lower eight bits of the label address are copied into the lower eight bits of the program counter.
- The ninth bit of the Program Counter is cleared to zero.
- The page select bits (in STATUS register) are copied into the upper two bits of the Program Counter.

This means that the call destination must *start* in the lower half of any page. For example, 00h-0FFh, 200h-2FFh, 400h-4FFh, etc.



15.10.4 Page Call Operation

When a subroutine that resides on a different page is called, the page select bits must contain the proper values to point to the desired page before the call instruction is executed. This can be done easily using SETB and CLRB instructions or writing a value to the STATUS register. The device also has the PAGE instruction, which automatically selects the page in a single-cycle execution.



Note:“N” must be 0, 1, 2, or 3.

15.11 Return Instructions

The device has several instructions for returning from subroutines and interrupt service routines. The return from subroutine instructions are RET (return without affecting W), RETP (same as RET but affects PA1:PA0), RETI (return from interrupt), RETIW (return and add W to RTCC), and RETW #literal (return and place literal in W). The literal serves as an immediate data value from memory. This instruction can be used for table lookup operations. To do table lookup, the table must contain a string of RETW #literal instructions. The first instruction just in front of the table calculates the offset into the table. The table can be used as a result of a CALL.

15.13 Comparison and Conditional Branch Instructions

The instruction set includes instructions such as DECSZ fr (decrement file register and skip if zero), INCSZ fr (increment file register and skip if zero), SNB bit (bit test file register and skip if bit clear), and SB bit (bit test file register and skip if bit set). These instructions will cause the next instruction to be skipped if the tested condition is true. If a skip instruction is immediately followed by a PAGE or BANK instruction (and the tested condition is true) then two instructions are skipped and the operation consumes three cycles. This is useful for conditional branching to another page where a PAGE instruction precedes a JMP. If several PAGE and BANK instructions immediately follow a skip instruction then they are all skipped plus the next instruction and a cycle is consumed for each.

15.14 Logical Instruction

The instruction set contain a full complement of the logical instructions (AND, OR, Exclusive OR), with the W register and a selected memory location (using either direct or indirect addressing) serving as the two operands.

15.15 Shift and Rotate Instructions

The instruction set includes instructions for left or right rotate-through-carry.

15.16 Complement and SWAP

The device can perform one's complement operation on the file register (fr) and W register. The MOV W,<>fr instruction performs nibble-swap on the fr and puts the value into the W register.

15.17 Key to Abbreviations and Symbols

Symbol	Description
W	Working register
fr	File register (memory-mapped register in the range of 00h to FFh)
PC	Lower eight bits of program counter (file register 02h)
STATUS	STATUS register (file register 03h)
FSR	File Select Register (file register 04h)
C	Carry bit in STATUS register (bit 0)
DC	Digit Carry bit in STATUS register (bit 1)
Z	Zero bit in STATUS register (bit 2
PD	Power Down bit in STATUS register (bit 3)
TO	Watchdog Timeout bit in STATUS register (bit 4)
PA2:PA0	Page select bits in STATUS register (bits 7:5)
OPTION	OPTION register (not memory-mapped)
WDT	Watchdog Timer register (not memory-mapped)
MODE	MODE register (not memory-mapped)
rx	Port control register pointer (RA, RB, or RC)
!	Non-memory-mapped register designator
f	File register address bit in opcode
k	Constant value bit in opcode
n	Numerical value bit in opcode
b	Bit position selector bit in opcode
.	File register / bit selector separator in assembly language instruction
#	Immediate literal designator in assembly language instruction
lit	Literal value in assembly language instruction
addr8	8-bit address in assembly language instruction
addr9	9-bit address in assembly language instruction
addr12	12-bit address in assembly language instruction
/	Logical 1's complement
|	Logical OR
^	Logical exclusive OR
&	Logical AND
<>	Swap high and low nibbles (4-bit segments)
<<	Rotate left through carry bit
>>	Rotate right through carry bit
- -	Decrement file register
++	Increment file register

16.0 INSTRUCTION SET SUMMARY TABLE

Table 16-1 lists all of the instructions, organized by category. For each instruction, the table shows the instruction mnemonic (as written in assembly language), a brief description of what the instruction does, the number of instruction cycles required for execution, the binary opcode, and the status bits affected by the instruction.

The "Cycles" column typically shows a value of 1, which means that the overall throughput for the instruction is one per clock cycle. In some cases, the exact number of cycles depends on the outcome of the instruction (such as the test-and-skip instructions) or the clocking mode (Compatible or Turbo). In those cases, all possible numbers of cycles are shown in the table.

The instruction execution time is derived by dividing the oscillator frequency by either one (Turbo mode) or four (Compatible mode). The divide-by factor is selected through the FUSE Word register.

Table 16-1. The SX Instruction Set

Mnemonic, Operands	Description	Cycles (Compatible)	Cycles (Turbo)	Opcode	Bits Affected
Logical Operations					
AND fr, W	AND of fr and W into fr (fr = fr & W)	1	1	0001 011f ffff	Z
AND W, fr	AND of W and fr into W (W = W & fr)	1	1	0001 010f ffff	Z
AND W,#lit	AND of W and Literal into W (W = W & lit)	1	1	1110 kkkk kkkk	Z
NOT fr	Complement of fr into fr (fr = fr ^ FFh)	1	1	0010 011f ffff	Z
OR fr,W	OR of fr and W into fr (fr = fr | W)	1	1	0001 001f ffff	Z
OR W,fr	OR of W and fr into fr (W = W | fr)	1	1	0001 000f ffff	Z
OR W,#lit	OR of W and Literal into W (W = W | lit)	1	1	1101 kkkk kkkk	Z
XOR fr,W	XOR of fr and W into fr (fr = fr ^ W)	1	1	0001 101f ffff	Z
XOR W,fr	XOR of W and fr into W (W = W ^ fr)	1	1	0001 100f ffff	Z
XOR W,#lit	XOR of W and Literal into W (W = W ^ lit)	1	1	1111 kkkk kkkk	Z
Arithmetic and Shift Operations					
ADD fr,W	Add W to fr (fr = fr + W); carry bit is added if $\overline{CF}$ bit in FUSEX register is cleared to 0	1	1	0001 111f ffff	C, DC, Z
ADD W,fr	Add fr to W (W = W + fr); carry bit is added if $\overline{CF}$ bit in FUSEX register is cleared to 0	1	1	0001 110f ffff	C, DC, Z
CLR fr	Clear fr (fr = 0)	1	1	0000 011f ffff	Z
CLR W	Clear W (W = 0)	1	1	0000 0100 0000	Z
CLR !WDT	Clear Watchdog Timer, clear prescaler if assigned to the Watchdog (TO = 1, PD = 1)	1	1	0000 0000 0100	TO, PD
DEC fr	Decrement fr (fr = fr - 1)	1	1	0000 111f ffff	Z
DECSZ fr	Decrement fr and Skip if Zero (fr = fr - 1 and skip next instruction if result is zero)	1 or 2 (skip)	1 or 2 (skip)	0010 111f ffff	none
INC fr	Increment fr (fr = fr + 1)	1	1	0010 101f ffff	Z
INCSZ fr	Increment fr and Skip if Zero (fr = fr + 1 and skip next instruction if result is zero)	1 or 2 (skip)	1 or 2 (skip)	0011 111f ffff	none
RL fr	Rotate fr Left through Carry (fr = << fr)	1	1	0011 011f ffff	C
RR fr	Rotate fr Right through Carry (fr = >> fr)	1	1	0011 001f ffff	C
SUB fr,W	Subtract W from fr (fr = fr - W); complement of the carry bit is subtracted if $\overline{CF}$ bit in FUSEX register is cleared to 0	1	1	0000 101f ffff	C, DC, Z
SWAP fr	Swap High/Low Nibbles of fr (fr = <> fr)	1	1	0011 101f ffff	none

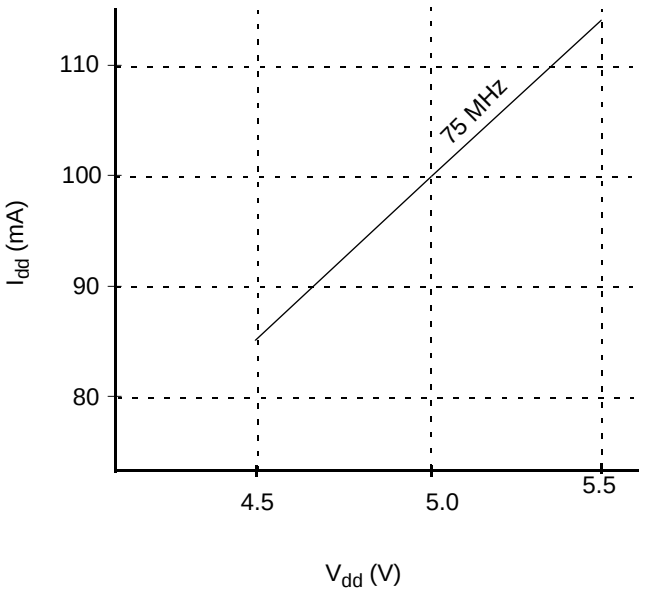
Table 16-1. The SX Instruction Set (Continued)

Mnemonic, Operands	Description	Cycles (Compatible)	Cycles (Turbo)	Opcode	Bits Affected
Bitwise Operations					
CLRB fr.bit	Clear Bit in fr (fr.bit = 0)	1	1	0100 bbbf ffff	none
SB fr.bit	Test Bit in fr and Skip if Set (test fr.bit and skip next instruction if bit is 1)	1 or 2 (skip)	1 or 2 (skip)	0111 bbbf ffff	none
SETB fr.bit	Set Bit in fr (fr.bit = 1)	1	1	0101 bbbf ffff	none
SNB fr.bit	Test Bit in fr and Skip if Clear (test fr.bit and skip next instruction if bit is 0)	1 or 2 (skip)	1 or 2 (skip)	0110 bbbf ffff	none
Data Movement Instructions					
MOV fr,W	Move W to fr (fr = W)	1	1	0000 001f ffff	none
MOV W,fr	Move fr to W (W = fr)	1	1	0010 000f ffff	Z
MOV W,fr-W	Move (fr-W) to W (W = fr - W); complement of carry bit is subtracted if CF bit in FUSEX register is cleared to 0	1	1	0000 100f ffff	C, DC, Z
MOV W,#lit	Move Literal to W (W = lit)	1	1	1100 kkkk kkkk	none
MOV W,/fr	Move Complement of fr to W (W = fr ^ FFh)	1	1	0010 010f ffff	Z
MOV W,--fr	Move (fr-1) to W (W = fr - 1)	1	1	0000 110f ffff	Z
MOV W,++fr	Move (fr+1) to W (W = fr + 1)	1	1	0010 100f ffff	Z
MOV W,<<fr	Rotate fr Left through Carry and Move to W (W = << fr)	1	1	0011 010f ffff	C
MOV W,>>fr	Rotate fr Right through Carry and Move to W (W = >> fr)	1	1	0011 000f ffff	C
MOV W,<>fr	Swap High/Low Nibbles of fr and move to W (W = <> fr)	1	1	0011 100f ffff	none
MOV W,M	Move MODE Register to W (W = MODE), high nibble is cleared	1	1	0000 0100 0010	none
MOVSZ W,--fr	Move (fr-1) to W and Skip if Zero (W = fr -1 and skip next instruction if result is zero)	1 or 2 (skip)	1 2 (skip)	0010 110f ffff	none
MOVSZ W,++fr	Move (fr+1) to W and Skip if Zero (W = fr + 1 and skip next instruction if result is zero)	1 or 2 (skip)	1 2 (skip)	0011 110f ffff	none
MOV M,W	Move W to MODE Register (MODE = W)	1	1	0000 0100 0011	none
MOV M,#lit	Move Literal to MODE Register (MODE = lit)	1	1	0000 0101 kkkk	none
MOV !rx,W	Move W to Port Rx Control Register:rx <=> W (exchange W and WKPND_B or CMP_B) *or* rx = W (move W to rx for all other port control registers)	1	1	0000 0000 0fff	none
MOV !OPTION, W	Move W to OPTION Register (OPTION = W)	1	1	0000 0000 0010	none
TEST fr	Test fr for Zero (fr = fr to set or clear Z bit)	1	1	0010 001f ffff	Z

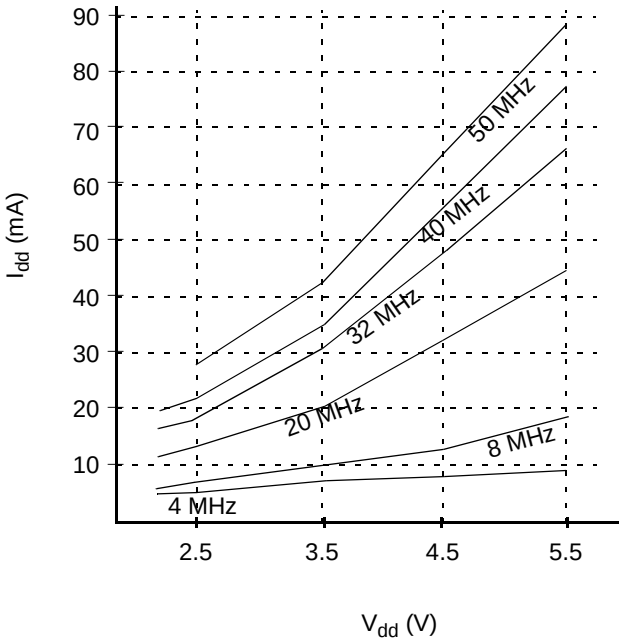
17.7 Typical Performance Characteristics (Continued)

Active Supply Current Vs Operating Frequency (External Clock)

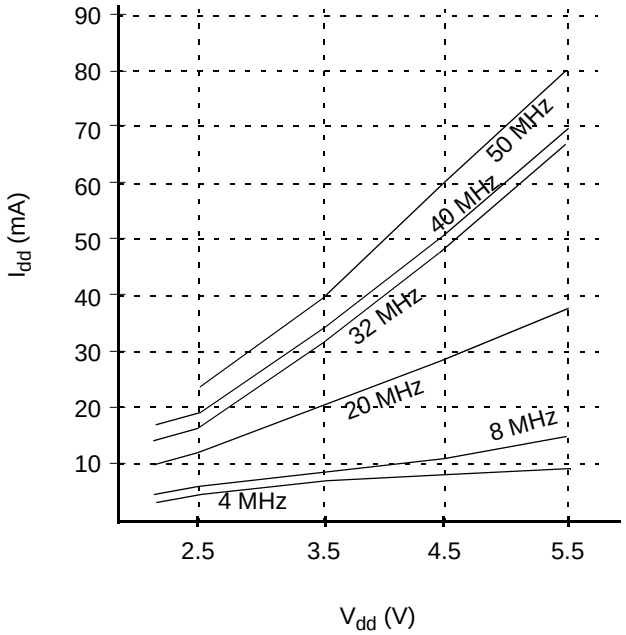
SX18AC75/SX20AC75/SX28AC75



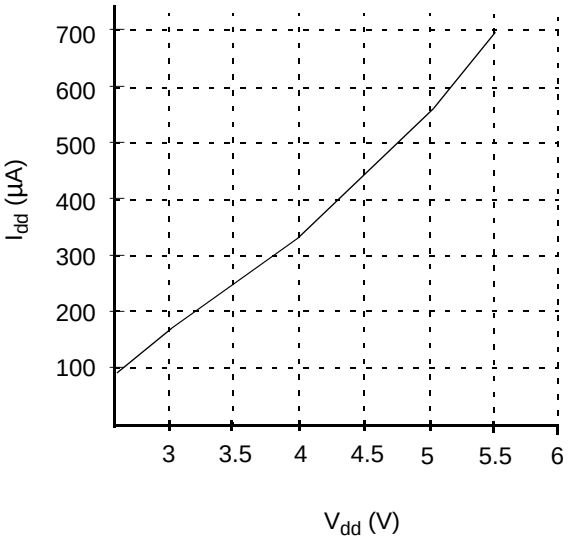
Active Supply Current Vs V_{dd} (Crystal Clock)



Active Supply Current Vs V_{dd} (External Clock)

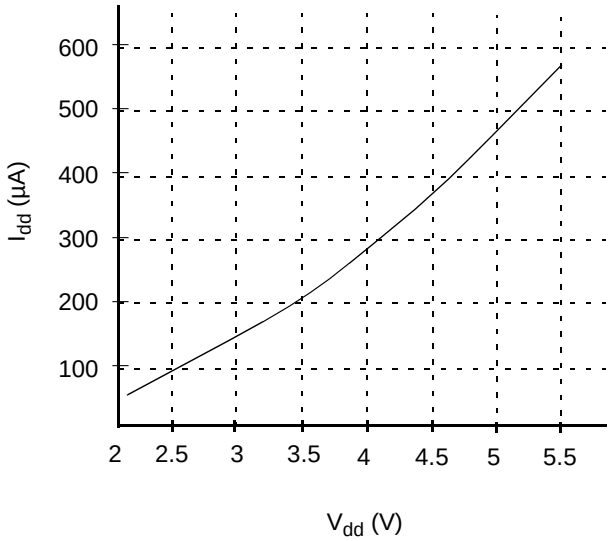


Active Supply Current Vs V_{dd} (32 kHz Crystal Clock)

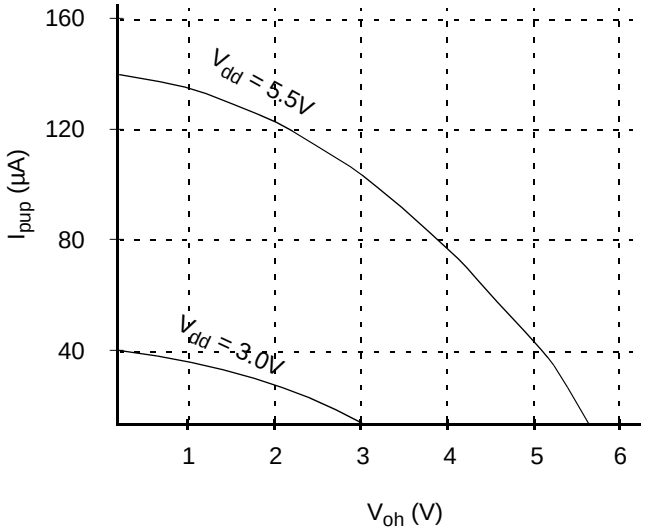


17.7 Typical Performance Characteristics (25°C)

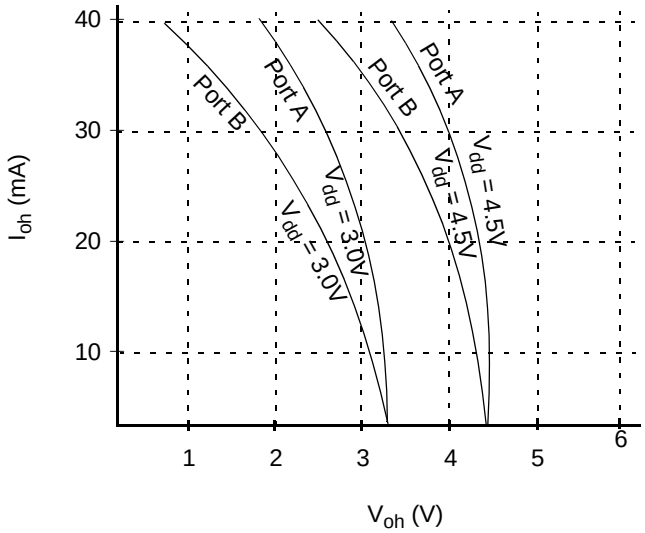
Active Supply Current Vs V_{dd} (32 kHz External Clock)



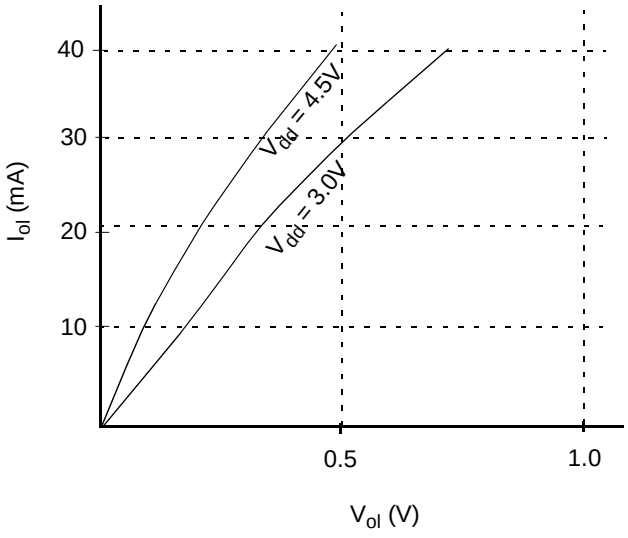
Port A/B/C Weak Pull-Up Source Current



Port A/B/C Source Current

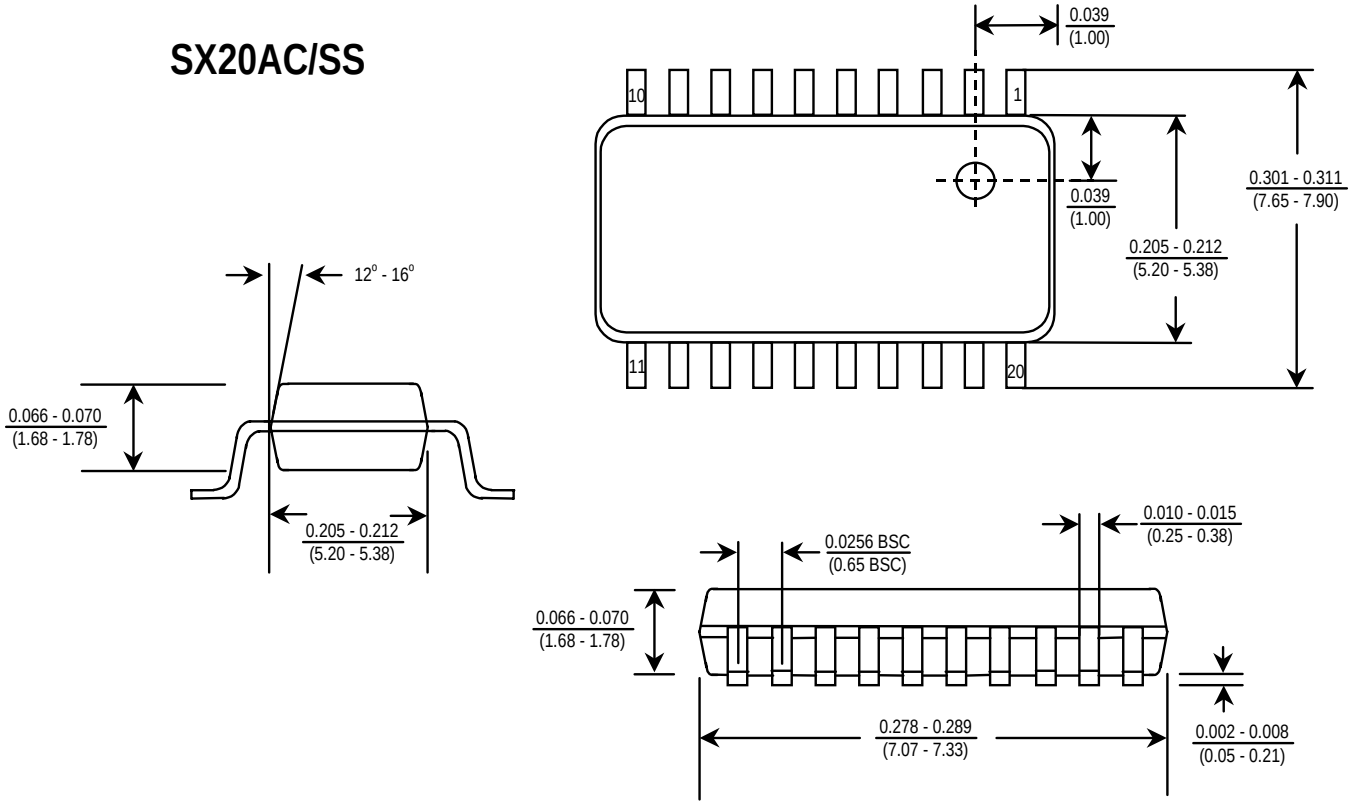


Port A/B/C Sink Current

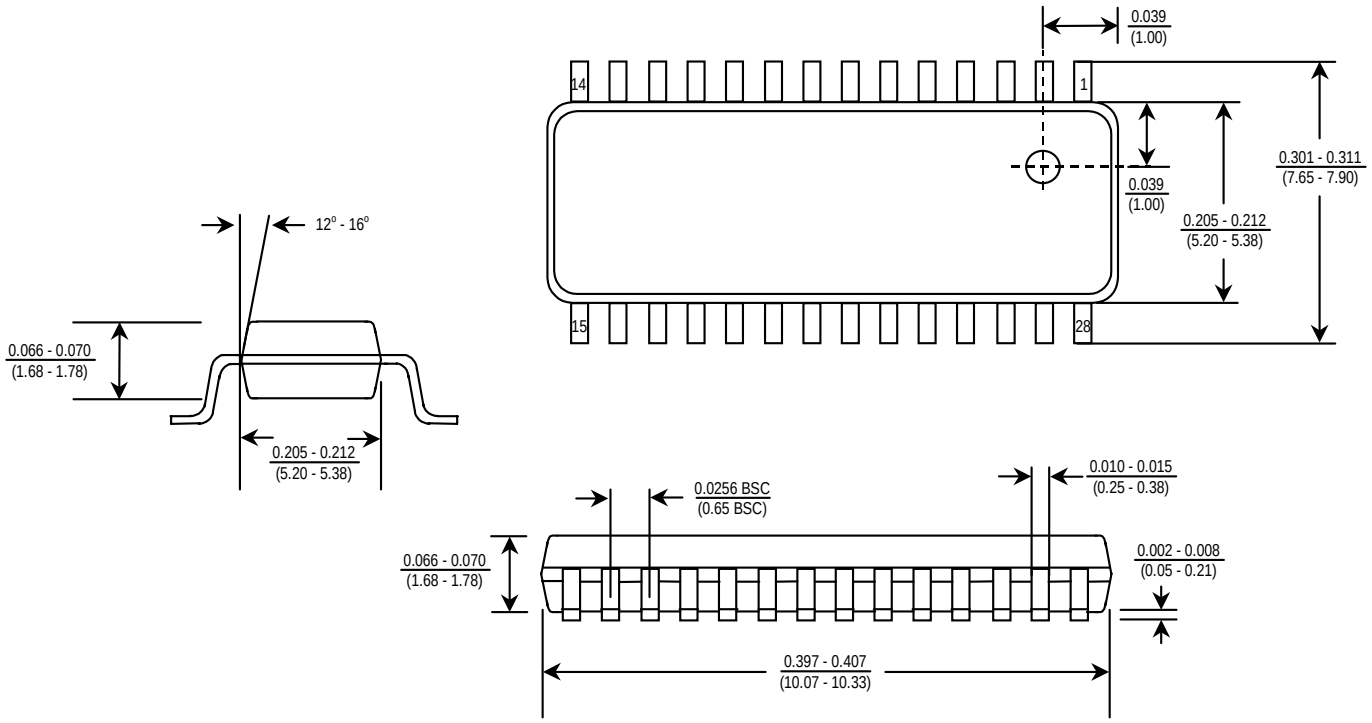


18.0 PACKAGE DIMENSIONS (DIMENSIONS ARE IN INCHES/(MILLIMETERS)

SX20AC/SS



SX28AC/SS



SX28AC/DP