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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4244pva-442">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4244pva-442</a>

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## Functional Overview

### CPU and Memory Subsystem

#### CPU

The Cortex-M0 CPU in PSoC 4200 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG; the debug configuration used for PSoC 4200 has four break-point (address) comparators and two watchpoint (data) comparators.

#### Flash

The PSoC 4200 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4200 flash supports the following flash protection modes at the Memory subsystem level.

**Open:** No Protection. Factory default mode that the product is shipped in.

**Protected:** User may change from Open to Protected. This mode disables Debug interface accesses. The mode can be set back to Open but only after completely erasing the flash.

**Kill:** User may change from Open to Kill. This mode disables all Debug accesses. The part cannot be erased externally thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrevocable mode.

In addition, Row level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

#### SRAM

SRAM memory is retained during Hibernate.

#### SROM

A supervisory ROM that contains boot and configuration routines is provided.

## System Resources

### Power System

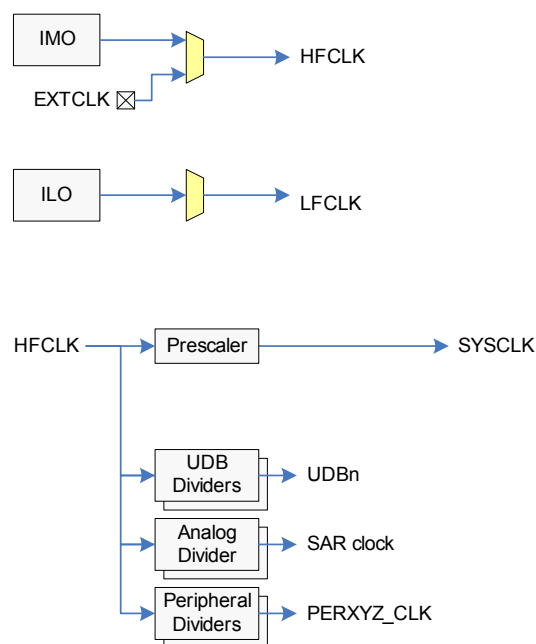
The power system is described in detail in the section [Power on page 11](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). PSoC 4200 operates with a single external supply over the range of 1.71 V to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

### Clock System

The PSoC 4200 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4200 consists of the IMO and the ILO internal oscillators and provision for an external clock.

**Figure 1. PSoC 4200 MCU Clocking Architecture**



The HFCLK signal can be divided down (see [PSoC 4200 MCU Clocking Architecture](#)) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4200, each with 16-bit divide capability; this allows eight to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator. When UDB-generated Pulse Interrupts are used, SYSCLK must equal HFCLK.

### Opamp (CTBm Block)

PSoC 4200 has an opamp with Comparator mode which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamp is designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

### Temperature Sensor

PSoC 4200 has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress supplied software that includes calibration and linearization.

### Low-power Comparators

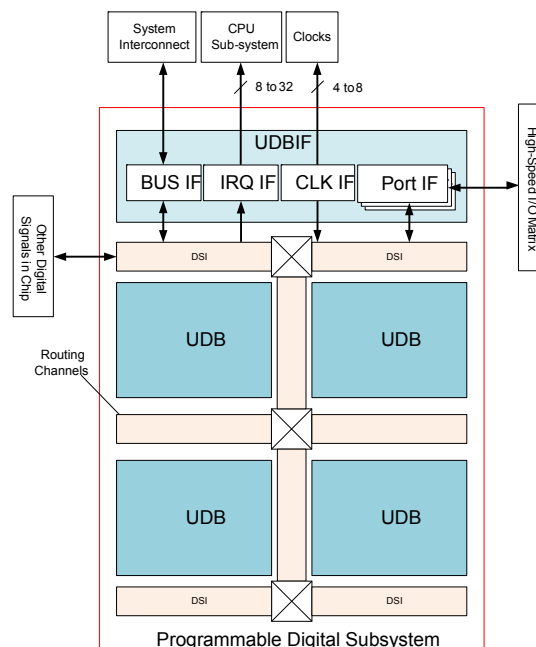
PSoC 4200 has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

## Programmable Digital

### Universal Digital Blocks (UDBs) and Port Interfaces

PSoC 4200 has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

**Figure 3. UDB Array**

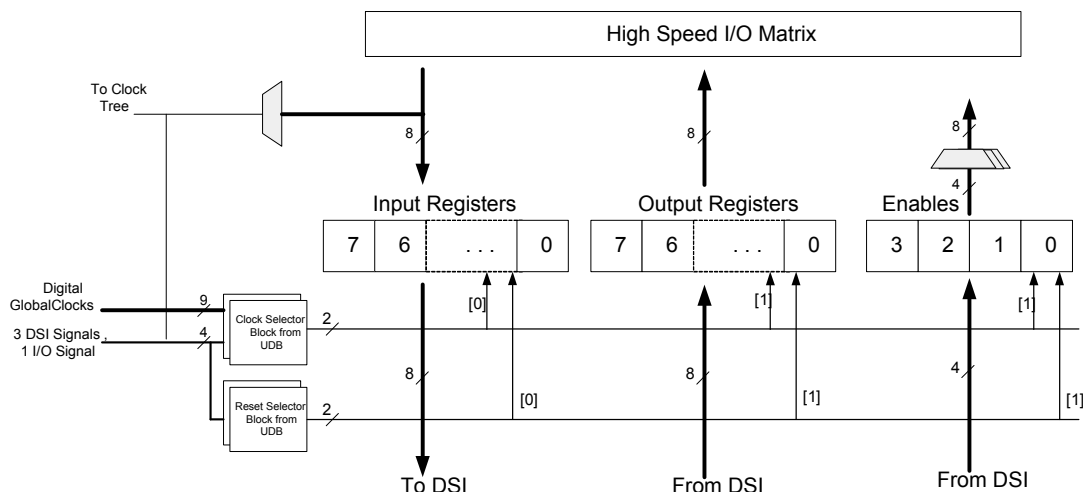


UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs (see Figure 4).

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs retain the ability to connect to any pin on the chip through the DSI.

**Figure 4. Port Interface**



## Fixed Function Digital

### Timer/Counter/PWM Block

The Timer/Counter/PWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

### Serial Communication Blocks (SCB)

PSoC 4200 has two SCBs, which can each implement an I<sup>2</sup>C, UART, SPI, or LIN Slave interface.

**I<sup>2</sup>C Mode:** The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes. The I<sup>2</sup>C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. Required Rise and Fall times for different I<sup>2</sup>C speeds are guaranteed by using appropriate pull-up resistor values depending on V<sub>DD</sub>, Bus Capacitance, and resistor tolerance. For detailed information on how to calculate the optimum pull-up resistor value for your design, please refer to the UM10204 I<sup>2</sup>C bus specification and user manual, the newest revision is available at [www.nxp.com](http://www.nxp.com).

PSoC 4200 is not completely compliant with the I<sup>2</sup>C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system.
- Fast-mode Plus has an I<sub>OL</sub> specification of 20 mA at a V<sub>OL</sub> of 0.4 V. The GPIO cells can sink a maximum of 8 mA I<sub>OL</sub> with a V<sub>OL</sub> maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I<sup>2</sup>C Master, it interposes an IDLE state between NACK and Repeated Start; the I<sup>2</sup>C spec defines Bus free as following a Stop condition so other Active Masters do

not intervene but a Master that has just become activated may start an Arbitration cycle.

- When the SCB is in I<sup>2</sup>C Slave mode, and Address Match on External Clock is enabled (EC\_AM = 1) along with operation in the internally clocked mode (EC\_OP = 0), then its I<sup>2</sup>C address must be even.

**UART Mode:** This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated. Note that hardware handshaking is not supported. This is not commonly used and can be implemented with a UDB-based UART in the system, if required.

**SPI Mode:** The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and also supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

**LIN Slave Mode:** The LIN Slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN slave is compliant with LIN v1.3 and LIN v2.1/2.2 specification standards. It is certified by C&S GmbH based on the standard protocol and data link layer conformance tests. LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40-meter cable length. PSoC Creator software supports up to two LIN slave interfaces in the PSoC 4 device, providing built-in application programming interfaces (APIs) based on the LIN specification standard.

## GPIO

PSoC 4200 has 24 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4200).

## Special Function Peripherals

### *LCD Segment Drive*

PSoC 4200 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

### *CapSense*

CapSense is supported on all pins in PSoC 4200 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used. (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

## Pinouts

The following is the pin-list for PSoC 4200. Port 2 comprises of the high-speed Analog inputs for the SAR Mux. P1.7 is the optional external input and bypass for the SAR reference. Ports 3 and 4 contain the Digital Communication channels. All pins support CSD CapSense and Analog Mux Bus connections.

Pins		28-SSOP		Alternate Functions for Pins					Pin Description
Name	Type	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
VSSD	Power	DN	–	–	–	–	–	–	Digital Ground
P2.2	GPIO	5	P2.2	sarmux.2	–	–	–	–	Port 2 Pin 2: gpio, lcd, csd, sarmux
P2.3	GPIO	6	P2.3	sarmux.3	–	–	–	–	Port 2 Pin 3: gpio, lcd, csd, sarmux
P2.4	GPIO	7	P2.4	sarmux.4	tcpwm0_p[1]	–	–	–	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
P2.5	GPIO	8	P2.5	sarmux.5	tcpwm0_n[1]	–	–	–	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
P2.6	GPIO	9	P2.6	sarmux.6	tcpwm1_p[1]	–	–	–	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
P2.7	GPIO	10	P2.7	sarmux.7	tcpwm1_n[1]	–	–	–	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
P3.0	GPIO	11	P3.0	–	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
P3.1	GPIO	12	P3.1	–	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
P3.2	GPIO	13	P3.2	–	tcpwm1_p[0]	–	swd_io	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
P3.3	GPIO	14	P3.3	–	tcpwm1_n[0]	–	swd_clk	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
P4.0	GPIO	15	P4.0	–	–	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
P4.1	GPIO	16	P4.1	–	–	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
P4.2	GPIO	17	P4.2	csd_c_mod	–	–	–	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
P4.3	GPIO	18	P4.3	csd_c_sh_tan_k	–	–	–	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
P0.0	GPIO	19	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
P0.1	GPIO	20	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
P0.2	GPIO	21	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
P0.3	GPIO	22	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
P0.6	GPIO	23	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
P0.7	GPIO	24	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
XRES	XRES	25	XRES	–	–	–	–	–	Chip reset, active low
VCCD	Power	26	VCCD	–	–	–	–	–	Regulated supply, connect to 1 µF cap or 1.8 V
VDDD	Power	27	VDDD	–	–	–	–	–	Common power supply (Analog and Digital) 1.8 V–5.5 V
VSSA	Power	28(DN)	VSS	–	–	–	–	–	Analog Ground
P1.0	GPIO	1	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
P1.1	GPIO	2	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
P1.2	GPIO	3	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
P1.7	GPIO	4	P1.7	ctb.oa1.inp_ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

### Notes:

1. tcpwm\_p and tcpwm\_n refer to tcpwm non-inverted and inverted outputs respectively.
2. P3.2 and P3.3 are SWD pins after boot (reset).

### Descriptions of the Pin functions are as follows:

**VDDD:** Power supply for both analog and digital sections (where there is no  $V_{DDA}$  pin).

**VDDA:** Analog  $V_{DD}$  pin where package pins allow; shorted to  $V_{DDD}$  otherwise.

**VSSA:** Analog ground pin where package pins allow; shorted to VSS otherwise

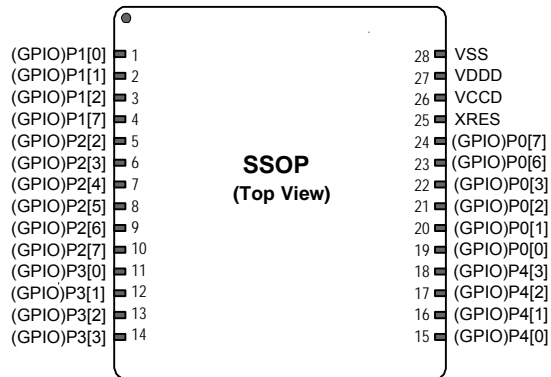
**VSS:** Ground pin.

**VCCD:** Regulated Digital supply (1.8 V  $\pm$ 5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following package is supported: 28-pin SSOP.

**Figure 5. 28-pin SSOP pinout**



## Development Support

The PSoC 4200 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit [www.cypress.com/go/psoc4](http://www.cypress.com/go/psoc4) to find out more.

### Documentation

A suite of documentation supports the PSoC 4200 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide:** A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets:** The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes:** PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC

motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual:** The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at [www.cypress.com/psoc4](http://www.cypress.com/psoc4).

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200 family is part of a development tool ecosystem. Visit us at [www.cypress.com/go/psoccreator](http://www.cypress.com/go/psoccreator) for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

**Table 3. DC Specifications** (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID25A	I <sub>DD20A</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on. 12 MHz	–	1.7	2.2	mA	V <sub>DD</sub> = 1.71 V to 5.5 V
Deep Sleep Mode, V <sub>DD</sub> = 1.8 V to 3.6V (Regulator on)							
SID31	I <sub>DD26</sub>	I <sup>2</sup> C wakeup and WDT on	–	1.3	–	μA	T = 25 °C
SID32	I <sub>DD27</sub>	I <sup>2</sup> C wakeup and WDT on	–	–	45	μA	T = 85 °C
Deep Sleep Mode, V <sub>DD</sub> = 3.6 V to 5.5 V							
SID34	I <sub>DD29</sub>	I <sup>2</sup> C wakeup and WDT on	–	1.5	15	μA	Typ at 25 °C Max at 85 °C
Deep Sleep Mode, V <sub>DD</sub> = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I <sub>DD32</sub>	I <sup>2</sup> C wakeup and WDT on	–	1.7	–	μA	T = 25 °C
SID38	I <sub>DD33</sub>	I <sup>2</sup> C wakeup and WDT on	–	–	60	μA	T = 85 °C
Deep Sleep Mode, +105 °C							
SID33Q	I <sub>DD28Q</sub>	I <sup>2</sup> C wakeup and WDT on. Regulator Off.	–	–	135	μA	V <sub>DD</sub> = 1.71 V to 1.89 V
SID34Q	I <sub>DD29Q</sub>	I <sup>2</sup> C wakeup and WDT on	–	–	180	μA	V <sub>DD</sub> = 1.8 V to 3.6 V
SID35Q	I <sub>DD30Q</sub>	I <sup>2</sup> C wakeup and WDT on	–	–	140	μA	V <sub>DD</sub> = 3.6 V to 5.5 V
Hibernate Mode, V <sub>DD</sub> = 1.8 V to 3.6 V (Regulator on)							
SID40	I <sub>DD35</sub>	GPIO & Reset active	–	150	–	nA	T = 25 °C
SID41	I <sub>DD36</sub>	GPIO & Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, V <sub>DD</sub> = 3.6 V to 5.5 V							
SID43	I <sub>DD38</sub>	GPIO & Reset active	–	150	–	nA	T = 25 °C
Hibernate Mode, V <sub>DD</sub> = 1.71 V to 1.89 V (Regulator bypassed)							
SID46	I <sub>DD41</sub>	GPIO & Reset active	–	150	–	nA	T = 25 °C
SID47	I <sub>DD42</sub>	GPIO & Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, +105 °C							
SID42Q	I <sub>DD37Q</sub>	Regulator Off	–	–	19.4	μA	V <sub>DD</sub> = 1.71 V to 1.89 V
SID43Q	I <sub>DD38Q</sub>		–	–	17	μA	V <sub>DD</sub> = 1.8 V to 3.6 V
SID44Q	I <sub>DD39Q</sub>		–	–	16	μA	V <sub>DD</sub> = 3.6 V to 5.5 V
Stop Mode							
SID304	I <sub>DD43A</sub>	Stop Mode current; V <sub>DD</sub> = 3.3 V	–	20	80	nA	Typ at 25 °C Max at 85 °C
		Stop Mode current; V <sub>DD</sub> = 5.5 V	–	20	750	nA	Typ at 25 °C Max at 85 °C
Stop Mode, +105 °C							
SID304Q	I <sub>DD43AQ</sub>	Stop Mode current; V <sub>DD</sub> = 3.6 V	–	–	5645	nA	
XRES current							
SID307	I <sub>DD_XR</sub>	Supply current while XRES asserted	–	2	5	mA	

**Table 9. Opamp Specifications** (continued)

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V	6	–	–	V/ $\mu$ sec	
SID299	T_op_wake	From disable to enable, no external RC dominating	–	300	–	$\mu$ sec	
	Comp_mode	Comparator mode; 50 mV drive, $T_{rise} = T_{fall}$ (approx.)	–	–	–		
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	Guaranteed by Design
SID300	T <sub>PD1</sub>	Response time; power = high	–	150	–	nsec	
SID301	T <sub>PD2</sub>	Response time; power = medium	–	400	–	nsec	
SID302	T <sub>PD3</sub>	Response time; power = low	–	2000	–	nsec	
SID303	Vhyst_op	Hysteresis	–	10	–	mV	

### Comparator

**Table 10. Comparator DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	V <sub>OFFSET2</sub>	Input offset voltage, Common Mode voltage range from 0 to $V_{DD}-1$	–	–	$\pm 4$	mV	
SID85A	V <sub>OFFSET3</sub>	Input offset voltage. Ultra low-power mode ( $V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C)	–	$\pm 12$	–	mV	
SID86	V <sub>HYST</sub>	Hysteresis when enabled, Common Mode voltage range from 0 to $V_{DD}-1$ .	–	10	35	mV	Guaranteed by characterization
SID87	V <sub>ICM1</sub>	Input common mode voltage in normal mode	0	–	$V_{DDD} - 0.1$	V	Modes 1 and 2.
SID247	V <sub>ICM2</sub>	Input common mode voltage in low power mode ( $V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C)	0	–	$V_{DDD}$	V	
SID247A	V <sub>ICM3</sub>	Input common mode voltage in ultra low power mode	0	–	$V_{DDD} - 1.15$	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq 2.7$ V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	$V_{DDD} < 2.7$ V. Guaranteed by characterization
SID89	I <sub>CMP1</sub>	Block current, normal mode	–	–	400	$\mu$ A	Guaranteed by characterization
SID248	I <sub>CMP2</sub>	Block current, low power mode	–	–	100	$\mu$ A	Guaranteed by characterization
SID259	I <sub>CMP3</sub>	Block current, ultra low power mode ( $V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C)	–	6	28	$\mu$ A	Guaranteed by characterization
SID90	Z <sub>CMP</sub>	DC input impedance of comparator	35	–	–	M $\Omega$	Guaranteed by characterization

**Table 11. Comparator AC Specifications**

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T <sub>RESP1</sub>	Response time, normal mode	–	–	110	ns	50 mV overdrive
SID258	T <sub>RESP2</sub>	Response time, low power mode	–	–	200	ns	50 mV overdrive
SID92	T <sub>RESP3</sub>	Response time, ultra low power mode (V <sub>DDD</sub> ≥ 2.2 V for Temp < 0 °C, V <sub>DDD</sub> ≥ 1.8 V for Temp > 0 °C)	–	–	15	µs	200 mV overdrive

### Temperature Sensor

**Table 12. Temperature Sensor Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	T <sub>SENSACC</sub>	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

### SAR ADC

**Table 13. SAR ADC DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	8		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference. Guaranteed by characterization
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V <sub>REF</sub> . Guaranteed by characterization
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

### LCD Direct Drive

**Table 19. LCD Direct Drive DC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I <sub>LCDLOW</sub>	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	C <sub>LCDCAP</sub>	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD <sub>OFFSET</sub>	Long-term segment offset	–	20	–	mV	
SID157	I <sub>LCDOP1</sub>	PWM Mode current. 5-V bias. 24-MHz IMO. 25 °C	–	0.6	–	mA	32 × 4 segments. 50 Hz
SID158	I <sub>LCDOP2</sub>	PWM Mode current. 3.3-V bias. 24-MHz IMO. 25 °C	–	0.5	–	mA	32 × 4 segments. 50 Hz

**Table 20. LCD Direct Drive AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F <sub>LCD</sub>	LCD frame rate	10	50	150	Hz	

**Table 21. Fixed UART DC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I <sub>UART1</sub>	Block current consumption at 100 Kbits/sec	–	–	55	μA	
SID161	I <sub>UART2</sub>	Block current consumption at 1000 Kbits/sec	–	–	312	μA	

**Table 22. Fixed UART AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID162	F <sub>UART</sub>	Bit rate	–	–	1	Mbps

### Memory

**Table 27. Flash DC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V <sub>PE</sub>	Erase and program voltage	1.71	–	5.5	V	

**Table 28. Flash AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T <sub>ROWWRITE</sub> <sup>[3]</sup>	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes. –40 °C ≤ T <sub>A</sub> ≤ 85 °C
			–	–	26	ms	Row (block) = 128 bytes. –40 °C ≤ T <sub>A</sub> ≤ 105 °C
SID175	T <sub>ROWERASE</sub> <sup>[3]</sup>	Row erase time	–	–	13	ms	
SID176	T <sub>ROWPROGRAM</sub> <sup>[3]</sup>	Row program time after erase	–	–	7	ms	–40 °C ≤ T <sub>A</sub> ≤ 85 °C
			–	–	13	ms	–40 °C ≤ T <sub>A</sub> ≤ 105 °C
SID178	T <sub>BULKERASE</sub> <sup>[3]</sup>	Bulk erase time (32 KB)	–	–	35	ms	
SID180	T <sub>DEVPROG</sub> <sup>[3]</sup>	Total device program time	–	–	7	seconds	Guaranteed by characterization
SID181	F <sub>END</sub>	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F <sub>RET</sub>	Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F <sub>RETQ</sub>	Flash retention. T <sub>A</sub> ≤ 105 °C, 10K P/E cycles, ≤ three years at T <sub>A</sub> ≥ 85 °C.	10	20	–		Guaranteed by characterization.

**Note**

- It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

**Table 32. Voltage Monitors AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID212	T <sub>MONTRIP</sub>	Voltage monitor trip time	–	–	1	μs	Guaranteed by characterization

SWD Interface

**Table 33. SWD Interface Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F <sub>SWDCLK1</sub>	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F <sub>SWDCLK2</sub>	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T <sub>SWDI_SETUP</sub>	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T <sub>SWDI_HOLD</sub>	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T <sub>SWDO_VALID</sub>	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T <sub>SWDO_HOLD</sub>	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

**Table 34. IMO DC Specifications**

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I <sub>IMO1</sub>	IMO operating current at 48 MHz	–	–	1000	μA	
SID219	I <sub>IMO2</sub>	IMO operating current at 24 MHz	–	–	325	μA	
SID220	I <sub>IMO3</sub>	IMO operating current at 12 MHz	–	–	225	μA	
SID221	I <sub>IMO4</sub>	IMO operating current at 6 MHz	–	–	180	μA	
SID222	I <sub>IMO5</sub>	IMO operating current at 3 MHz	–	–	150	μA	

**Table 35. IMO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F <sub>IMOTOL1</sub>	Frequency variation from 3 to 48 MHz	–	–	±2	%	+3% if T <sub>A</sub> > 85 °C and IMO frequency < 24 MHz
SID226	T <sub>STARTIMO</sub>	IMO startup time	–	–	12	μs	
SID227	T <sub>JITRMSIMO1</sub>	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	T <sub>JITRMSIMO2</sub>	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	T <sub>JITRMSIMO3</sub>	RMS Jitter at 48 MHz	–	139	–	ps	

### Internal Low-Speed Oscillator

**Table 36. ILO DC Specifications**

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I <sub>ILO1</sub>	ILO operating current at 32 kHz	–	0.3	1.05	μA	Guaranteed by characterization
SID233	I <sub>ILOLEAK</sub>	ILO leakage current	–	2	15	nA	Guaranteed by design

**Table 37. ILO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	T <sub>STARTILO1</sub>	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	T <sub>ILODUTY</sub>	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	F <sub>ILOTRIM1</sub>	32 kHz trimmed frequency	15	32	50	kHz	Max. ILO frequency is 70 kHz if T <sub>A</sub> > 85 °C

**Table 38. External Clock Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V <sub>DD/2</sub>	45	–	55	%	Guaranteed by characterization

**Table 39. UDB AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
<b>Datapath performance</b>							
SID249	F <sub>MAX-TIMER</sub>	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	
SID250	F <sub>MAX-ADDER</sub>	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	
SID251	F <sub>MAX_CRC</sub>	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	
<b>PLD Performance in UDB</b>							
SID252	F <sub>MAX_PLD</sub>	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	
<b>Clock to Output Performance</b>							
SID253	T <sub>CLK_OUT_UDB1</sub>	Prop. delay for clock in to data out at 25 °C, Typ.	–	15	–	ns	
SID254	T <sub>CLK_OUT_UDB2</sub>	Prop. delay for clock in to data out, Worst case.	–	25	–	ns	

**Table 40. Block Specs**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID256*	T <sub>WS48</sub> *	Number of wait states at 48 MHz	1	–	–		CPU execution from Flash. Guaranteed by characterization
SID257	T <sub>WS24</sub> *	Number of wait states at 24 MHz	0	–	–		CPU execution from Flash. Guaranteed by characterization
SID260	V <sub>REFSAR</sub>	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of V <sub>bg</sub> (1.024 V). Guaranteed by characterization
SID262	T <sub>CLKSWITCH</sub>	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	Guaranteed by design

\* Tws48 and Tws24 are guaranteed by Design

**Table 41. UDB Port Adaptor Specifications**

(Based on LPC Component Specs, Guaranteed by Characterization -10-pF load, 3-V V<sub>DDIO</sub> and V<sub>DDD</sub>)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID263	T <sub>LCLKDO</sub>	LCLK to output delay	–	–	18	ns	
SID264	T <sub>DINLCLK</sub>	Input setup time to LCLK rising edge	–	–	7	ns	
SID265	T <sub>DINLCLKHLD</sub>	Input hold time from LCLK rising edge	5	–	–	ns	
SID266	T <sub>LCLKHIZ</sub>	LCLK to output tristated	–	–	28	ns	
SID267	T <sub>FLCLK</sub>	LCLK frequency	–	–	33	MHz	
SID268	T <sub>LCLKDUTY</sub>	LCLK duty cycle (percentage high)	40	–	60	%	

## Ordering Information

The PSoC 4200 part numbers and features are listed in the following table.

**Table 42. PSoC 4200 Family Ordering Information**

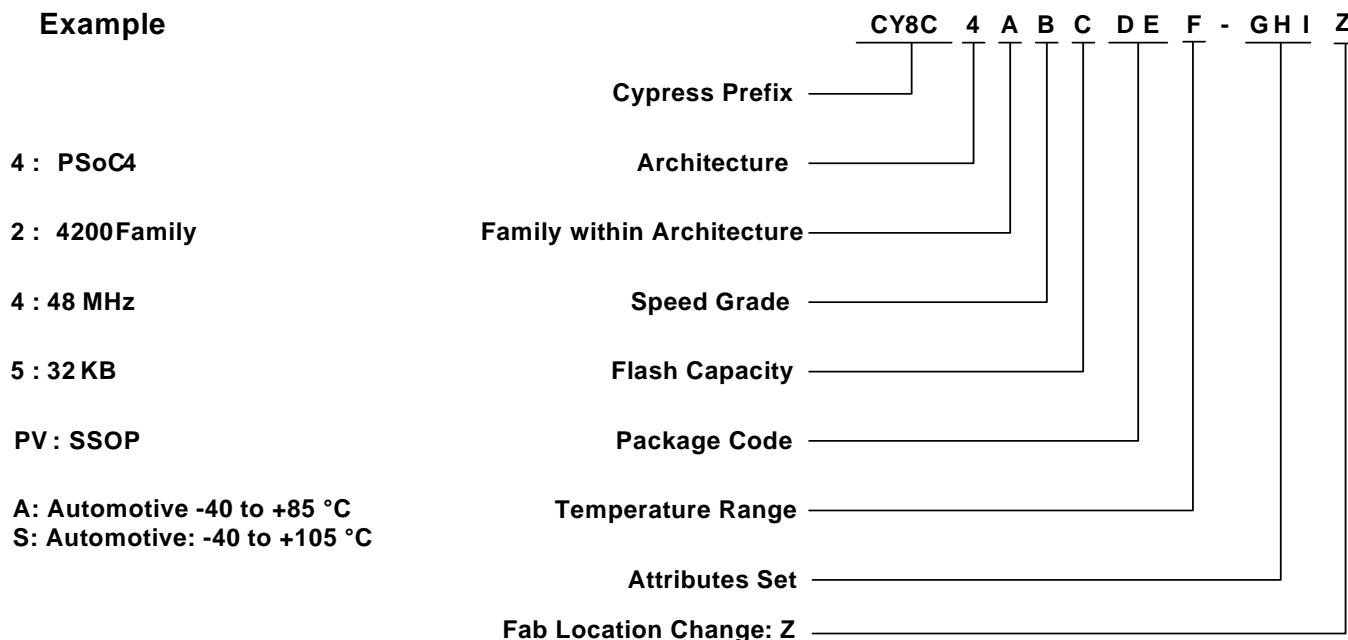
Family	MPN	Features												Package	Operating Temperature	
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm)	CapSense	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	GPIO	28-SSOP	-40 to +85 °C (A grade)	-40 to +105 °C (S grade)
4200	CY8C4244PVA-442Z	48	16	4	2	1	✓	✓	1 Msps	2	4	2	24	✓	✓	–
	CY8C4245PVA-452Z	48	32	4	4	0	–	✓	–	0	4	2	24	✓	✓	–
	CY8C4245PVA-482Z	48	32	4	4	1	✓	✓	1 Msps	2	4	2	24	✓	✓	–
	CY8C4244PVS-442Z	48	16	4	2	1	✓	✓	1 Msps	2	4	2	24	✓	–	✓
	CY8C4245PVS-452Z	48	32	4	4	0	–	✓	–	0	4	2	24	✓	–	✓
	CY8C4245PVS-482Z	48	32	4	4	1	✓	✓	1 Msps	2	4	2	24	✓	–	✓

## Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, ..., 9, A,B, ..., Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-GHI where the fields are defined as follows.

### Example



## Acronyms

**Table 47. Acronyms Used in this Document**

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

**Table 47. Acronyms Used in this Document** *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I <sup>2</sup> C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

**Table 47. Acronyms Used in this Document** *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC <sup>®</sup>	Programmable System-on-Chip <sup>™</sup>
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

**Table 47. Acronyms Used in this Document** *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

## Document Conventions

### Units of Measure

**Table 48. Units of Measure**

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femtofarad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msp	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt