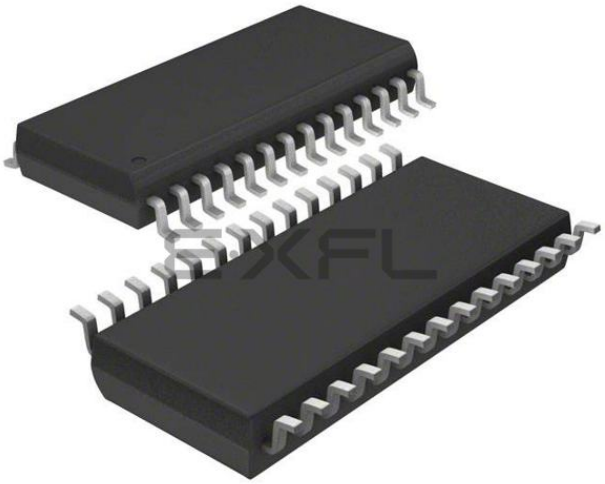

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4244pva-442t

Contents

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in PSoC 4200 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG; the debug configuration used for PSoC 4200 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4200 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4200 flash supports the following flash protection modes at the Memory subsystem level.

Open: No Protection. Factory default mode that the product is shipped in.

Protected: User may change from Open to Protected. This mode disables Debug interface accesses. The mode can be set back to Open but only after completely erasing the flash.

Kill: User may change from Open to Kill. This mode disables all Debug accesses. The part cannot be erased externally thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrecvocable mode.

In addition, Row level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

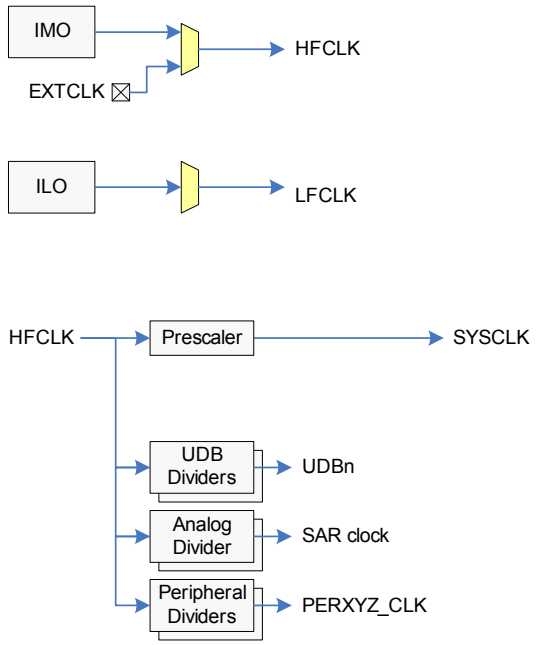
The power system is described in detail in the section Power on page 11. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). PSoC 4200 operates with a single external supply over the range of 1.71 V to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4200 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4200 consists of the IMO and the ILO internal oscillators and provision for an external clock.

Figure 1. PSoC 4200 MCU Clocking Architecture



The HFCLK signal can be divided down (see PSoC 4200 MCU Clocking Architecture) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4200, each with 16-bit divide capability; this allows eight to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator. When UDB-generated Pulse Interrupts are used, SYSCLK must equal HFCLK.

Opamp (CTBm Block)

PSoC 4200 has an opamp with Comparator mode which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamp is designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Temperature Sensor

PSoC 4200 has one on-chip temperature sensor This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress supplied software that includes calibration and linearization.

Low-power Comparators

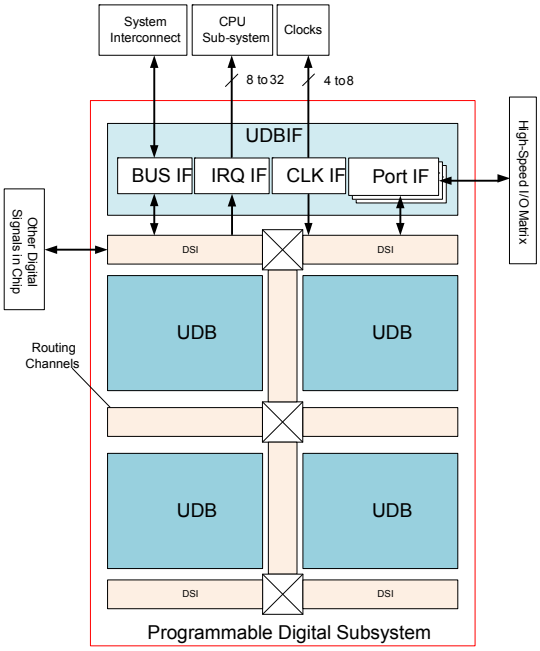
PSoC 4200 has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

Programmable Digital

Universal Digital Blocks (UDBs) and Port Interfaces

PSoC 4200 has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

Figure 3. UDB Array

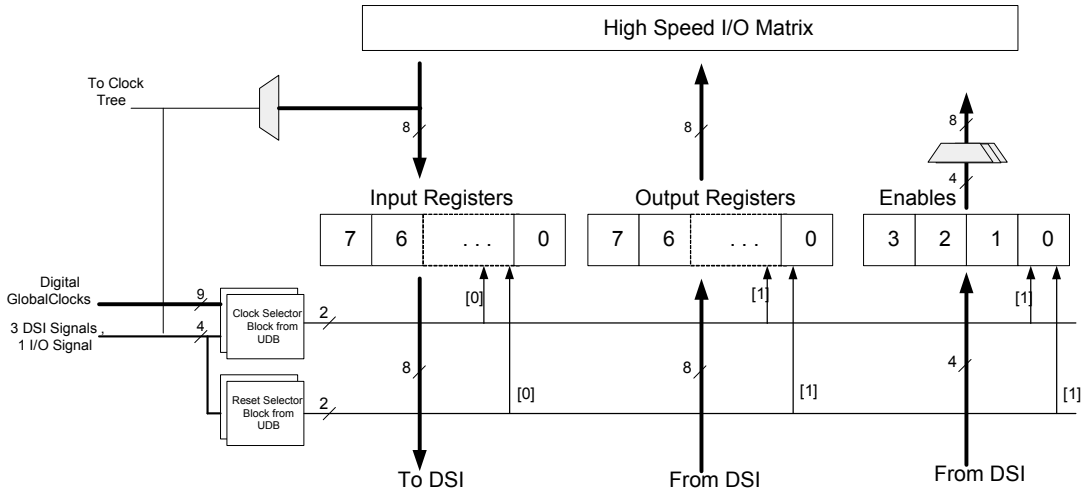


UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs (see Figure 4).

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs retain the ability to connect to any pin on the chip through the DSI.

Figure 4. Port Interface



Fixed Function Digital

Timer/Counter/PWM Block

The Timer/Counter/PWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

Serial Communication Blocks (SCB)

PSoC 4200 has two SCBs, which can each implement an I^2C, UART, SPI, or LIN Slave interface.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes. The I^2C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. Required Rise and Fall times for different I^2C speeds are guaranteed by using appropriate pull-up resistor values depending on V_{DD}, Bus Capacitance, and resistor tolerance. For detailed information on how to calculate the optimum pull-up resistor value for your design, please refer to the UM10204 I^2C bus specification and user manual, the newest revision is available at www.nxp.com.

PSoC 4200 is not completely compliant with the I^2C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8 mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I^2C Master, it interposes an IDLE state between NACK and Repeated Start; the I^2C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in I^2C Slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its I^2C address must be even.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated. Note that hardware handshaking is not supported. This is not commonly used and can be implemented with a UDB-based UART in the system, if required.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and also supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

LIN Slave Mode: The LIN Slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN slave is compliant with LIN v1.3 and LIN v2.1/2.2 specification standards. It is certified by C&S GmbH based on the standard protocol and data link layer conformance tests. LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40-meter cable length. PSoC Creator software supports up to two LIN slave interfaces in the PSoC 4 device, providing built-in application programming interfaces (APIs) based on the LIN specification standard.

GPIO

PSoC 4200 has 24 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

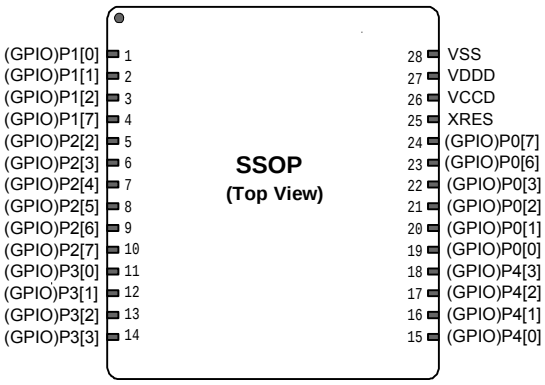
VSS: Ground pin.

VCCD: Regulated Digital supply (1.8 V ±5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following package is supported: 28-pin SSOP.

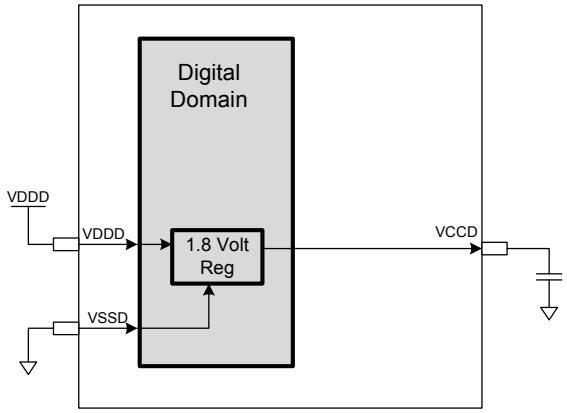
Figure 5. 28-pin SSOP pinout



Power

The following power system diagram shows the minimum set of power supply pins as implemented for PSoC 4200. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DDA} input. There are separate regulators for the Deep Sleep and Hibernate (lowered power supply and retention) modes. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

Figure 6. PSoC 4 Power Supply



The PSoC 4200 family allows two distinct modes of power supply operation: Unregulated External Supply, and Regulated External Supply modes.

Unregulated External Supply

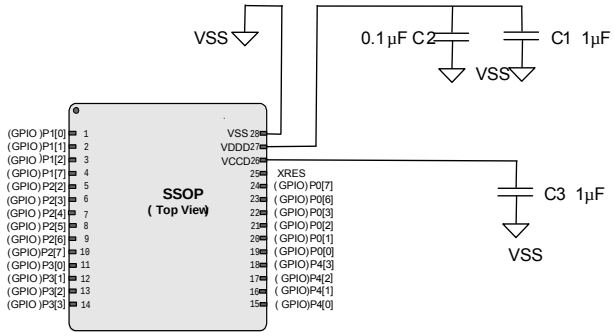
In this mode, the PSoC 4200 is powered by an External Power Supply that can be anywhere in the range of 1.8 to 5.5V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5V and works down to 1.8V. In this mode, the internal regulator of the PSoC 4200 supplies the internal logic and the VCCD output of the PSoC 4200 must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better).

Bypass capacitors must be used from VDDD to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 µF range in parallel with a smaller capacitor (0.1 µF for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Table 1. Example of a bypass scheme

Power Supply	Bypass Capacitors
VDDD–VSS	0.1 µF ceramic capacitor (C2) plus bulk capacitor 1 to 10 µF (C1). Total Capacitance may be greater than 10 µF.
VCCD–VSS	1 µF ceramic capacitor at the VCCD pin (C3)
VREF–VSS (optional)	The internal bandgap may be bypassed with a 1 µF to 10 µF capacitor. Total capacitance may be greater than 10 µF.

Figure 7. 28-pin SSOP Example



Regulated External Supply

In this mode, PSoC 4200 is powered by an external power supply that must be within the range of 1.71 to 1.89 V (1.8 ± 5%); note that this range needs to include power supply ripple too. In this mode, VCCD, and VDDD pins are all shorted together and bypassed. The internal regulator is disabled in firmware.

Table 3. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID25A	I_{DD20A}	I^2C wakeup, WDT, and Comparators on. 12 MHz	–	1.7	2.2	mA	V_{DD} = 1.71 V to 5.5 V
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	1.3	–	µA	T = 25 °C
SID32	I_{DD27}	I^2C wakeup and WDT on	–	–	45	µA	T = 85 °C
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	1.5	15	µA	Typ at 25 °C Max at 85 °C
Deep Sleep Mode, V_{DD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	1.7	–	µA	T = 25 °C
SID38	I_{DD33}	I^2C wakeup and WDT on	–	–	60	µA	T = 85 °C
Deep Sleep Mode, +105 °C							
SID33Q	I_{DD28Q}	I^2C wakeup and WDT on. Regulator Off.	–	–	135	µA	V_{DD} = 1.71 V to 1.89 V
SID34Q	I_{DD29Q}	I^2C wakeup and WDT on	–	–	180	µA	V_{DD} = 1.8 V to 3.6 V
SID35Q	I_{DD30Q}	I^2C wakeup and WDT on	–	–	140	µA	V_{DD} = 3.6 V to 5.5 V
Hibernate Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID40	I_{DD35}	GPIO & Reset active	–	150	–	nA	T = 25 °C
SID41	I_{DD36}	GPIO & Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, V_{DD} = 3.6 V to 5.5 V							
SID43	I_{DD38}	GPIO & Reset active	–	150	–	nA	T = 25 °C
Hibernate Mode, V_{DD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID46	I_{DD41}	GPIO & Reset active	–	150	–	nA	T = 25 °C
SID47	I_{DD42}	GPIO & Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, +105 °C							
SID42Q	I_{DD37Q}	Regulator Off	–	–	19.4	µA	V_{DD} = 1.71 V to 1.89 V
SID43Q	I_{DD38Q}		–	–	17	µA	V_{DD} = 1.8 V to 3.6 V
SID44Q	I_{DD39Q}		–	–	16	µA	V_{DD} = 3.6 V to 5.5 V
Stop Mode							
SID304	I_{DD43A}	Stop Mode current; V_{DD} = 3.3 V	–	20	80	nA	Typ at 25 °C Max at 85 °C
		Stop Mode current; V_{DD} = 5.5 V	–	20	750	nA	Typ at 25 °C Max at 85 °C
Stop Mode, +105 °C							
SID304Q	I_{DD43AQ}	Stop Mode current; V_{DD} = 3.6 V	–	–	5645	nA	
XRES current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	

Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60		3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60		3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout;1.7 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout;1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

XRES

Table 7. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 8. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Analog Peripherals

Opamp

Table 9. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I_{DD_HI}	Power = high	–	1100	1850	µA	
SID270	I_{DD_MED}	Power = medium	–	550	950	µA	
SID271	I_{DD_LOW}	Power = low	–	150	350	µA	
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	VDDA – 0.2	V	
SID282	V_{CM}	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	VDDA – 0.2	V	
	V_{OUT}	$V_{DDA} \geq 2.7$ V	–	–	–		
SID283	V_{OUT_1}	Power = high, Iload=10 mA	0.5	–	VDDA – 0.5	V	
SID284	V_{OUT_2}	Power = high, Iload=1 mA	0.2	–	VDDA – 0.2	V	
SID285	V_{OUT_3}	Power = medium, Iload=1 mA	0.2	–	VDDA – 0.2	V	
SID286	V_{OUT_4}	Power = low, Iload=0.1mA	0.2	–	VDDA – 0.2	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/C	High mode. $T_A \leq 85$ °C.
SID290Q	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–15	±3	15	µV/C	High mode. $T_A \leq 105$ °C
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Low mode
SID291	CMRR	DC	70	80	–	dB	VDDD = 3.6 V
SID292	PSRR	At 1 kHz, 100 mV ripple	70	85	–	dB	VDDD = 3.6 V
	Noise		–	–	–	–	
SID293	V_{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	µVrms	
SID294	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID295	V_{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	
SID296	V_{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	

Table 11. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T_{RESP1}	Response time, normal mode	–	–	110	ns	50 mV overdrive
SID258	T_{RESP2}	Response time, low power mode	–	–	200	ns	50 mV overdrive
SID92	T_{RESP3}	Response time, ultra low power mode (V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C)	–	–	15	µs	200 mV overdrive

Temperature Sensor

Table 12. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 13. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	8		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference. Guaranteed by characterization
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}. Guaranteed by characterization
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

CSD

Table 15. CSD Block Specification

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
CSD Specification							
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in High range	–	612	–	µA	
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in Low range	–	306	–	µA	
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in High range	–	304.8	–	µA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in Low range	–	152.4	–	µA	

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Timer/Counter/PWM

Table 16. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

I^2C

Table 17. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	

Table 18. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	

LCD Direct Drive

Table 19. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	
SID157	I_{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO. 25 °C	–	0.6	–	mA	32 × 4 segments. 50 Hz
SID158	I_{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO. 25 °C	–	0.5	–	mA	32 × 4 segments. 50 Hz

Table 20. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	

Table 21. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	
SID161	I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	

Table 22. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID162	F_{UART}	Bit rate	–	–	1	Mbps

Table 32. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	Guaranteed by characterization

SWD Interface

Table 33. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 34. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	
SID220	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	
SID221	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	
SID222	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	

Table 35. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	±3% if T_A > 85 °C and IMO frequency < 24 MHz
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12	µs	
SID227	$T_{JITRMSIMO1}$	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	$T_{JITRMSIMO2}$	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	$T_{JITRMSIMO3}$	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator

Table 36. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by design

Table 37. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency	15	32	50	kHz	Max. ILO frequency is 70 kHz if T_A > 85 °C

Table 38. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	Guaranteed by characterization

Table 39. UDB AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Datapath performance							
SID249	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	
SID250	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	
SID251	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	
PLD Performance in UDB							
SID252	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	
Clock to Output Performance							
SID253	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typ.	–	15	–	ns	
SID254	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case.	–	25	–	ns	

Table 40. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID256*	T_{WS48}*	Number of wait states at 48 MHz	1	–	–		CPU execution from Flash. Guaranteed by characterization
SID257	T_{WS24}*	Number of wait states at 24 MHz	0	–	–		CPU execution from Flash. Guaranteed by characterization
SID260	V_{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of Vbg (1.024 V). Guaranteed by characterization
SID262	$T_{CLKSWITCH}$	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	Guaranteed by design
* Tws48 and Tws24 are guaranteed by Design							

Table 41. UDB Port Adaptor Specifications

(Based on LPC Component Specs, Guaranteed by Characterization -10-pF load, 3-V V_{DDIO} and V_{DDD})

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID263	T_{LCLKDO}	LCLK to output delay	–	–	18	ns	
SID264	$T_{DINLCLK}$	Input setup time to LCLCK rising edge	–	–	7	ns	
SID265	$T_{DINLCLKHLD}$	Input hold time from LCLK rising edge	5	–	–	ns	
SID266	$T_{LCLKHIZ}$	LCLK to output tristated	–	–	28	ns	
SID267	T_{FLCLK}	LCLK frequency	–	–	33	MHz	
SID268	$T_{LCLKDUTY}$	LCLK duty cycle (percentage high)	40	–	60	%	

The field values are listed in the following table.

Table 43. Field Values

Field	Description	Values	Meaning
CY8C	Cypress prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	1	4100 Family
		2	4200 Family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	4	16 KB
		5	32 KB
DE	Package code	PV	SSOP
F	Temperature range	A/S	Automotive
GHI	Attributes code	000-999	Code of feature set in specific family
Z	Fab location change		

Packaging

Table 44. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	For A grade devices	–40	25.00	85	°C
T_A	Operating ambient temperature	For S grade devices	–40	25.00	105	°C
T_J	Operating junction temperature	For A grade devices	–40	–	100	°C
T_J	Operating junction temperature	For S grade devices	–40	–	120	°C
T_{JA}	Package θ_{JA} (28-pin SSOP)		–	66.58	–	°C/W
T_{JC}	Package θ_{JC} (28-pin SSOP)		–	46.28	–	°C/W

Table 45. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
28-pin SSOP	260 °C	30 seconds

Table 46. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
28-pin SSOP	MSL 3

PSoC4 CAB Libraries with Schematics Symbols and PCB Footprints are on the Cypress web site at http://www.cypress.com/cad-resources/psoc-4-cad-libraries?source=search&cat=technical_documents

Table 47. Acronyms Used in this Document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

Table 47. Acronyms Used in this Document *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 48. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femtofarad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

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