Welcome to E-XFL.COM

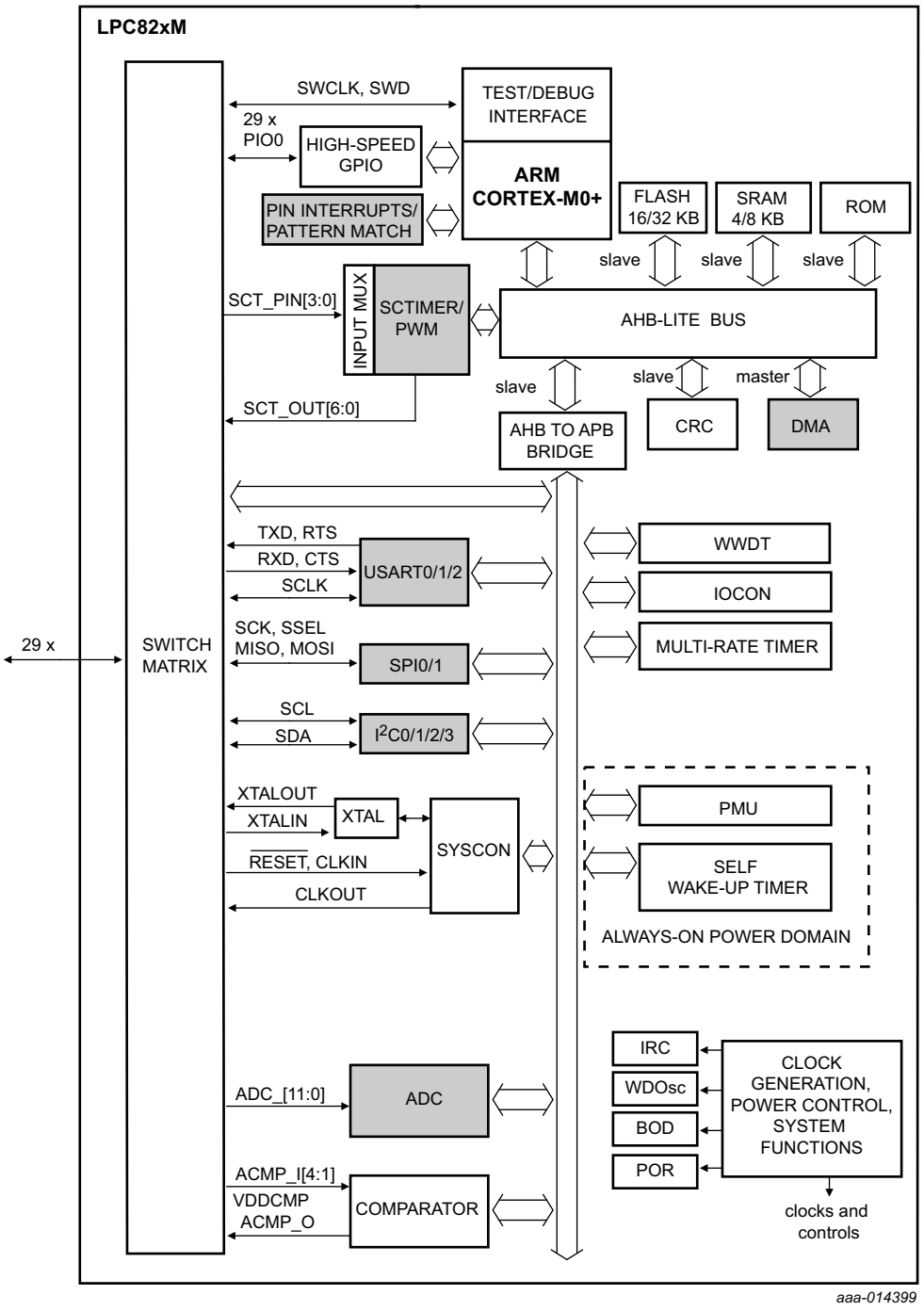
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc822m101jdh20j

6. Block diagram



Gray-shaded blocks show peripherals that can provide hardware triggers or fixed DMA requests for DMA transfers.

Fig 3. LPC82x block diagram

- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC82x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Supports NMI.

8.6.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.7 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 3 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 9 “LPC82x clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.9 for details.

8.8.1 Standard I/O pad configuration

Figure 7 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.

- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

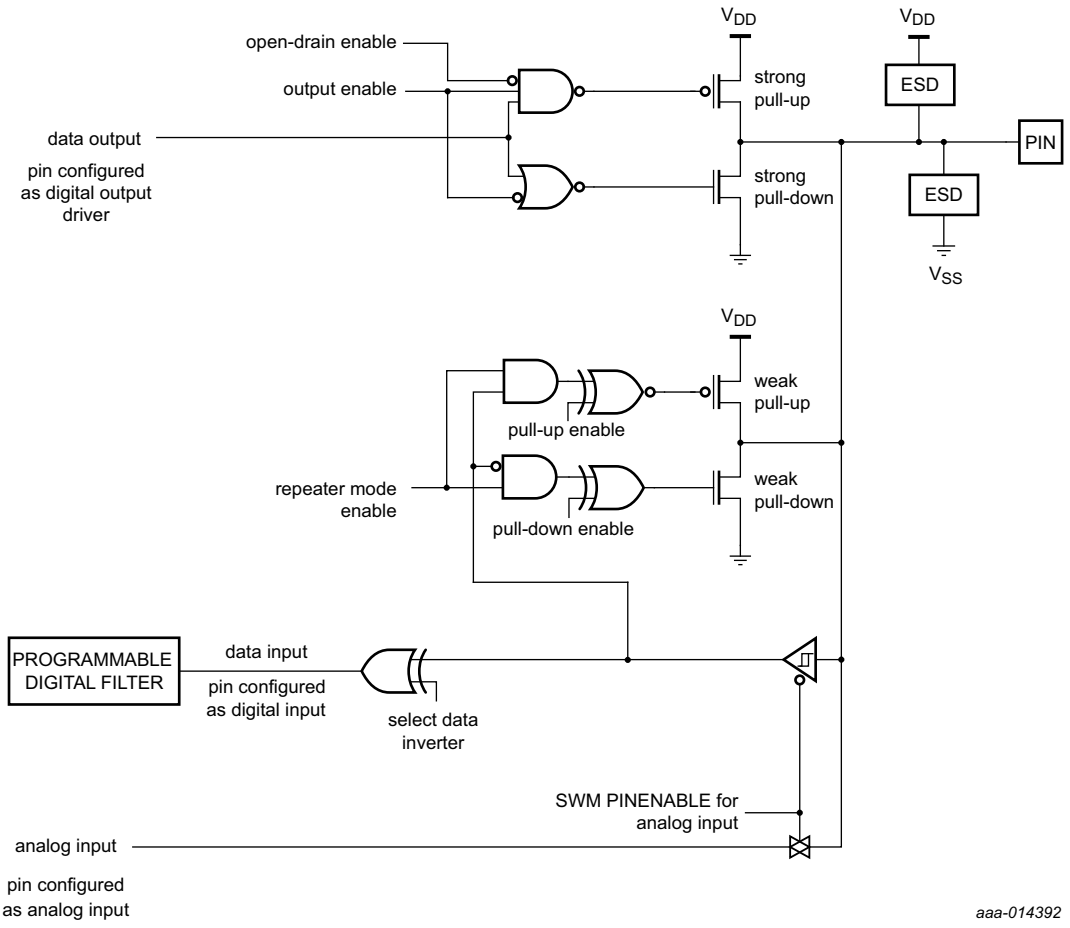


Fig 7. Standard I/O pad configuration

8.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.17 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.17.1 Features

- 31-bit interrupt timer
- Four channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

8.18 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

8.18.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) is generated by the dedicated watchdog oscillator (WDOSC).

8.19 Self-Wake-up Timer (WKT)

The self-wake-up timer is a 32-bit, loadable down counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur prior to entering a reduced power mode.

8.19.1 Features

- 32-bit loadable down counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports three clock sources: an external clock on the WKTCLKIN pin, the low-power oscillator, and the IRC. The low-power oscillator is located in the always-on power domain, so it can be used as the clock source in Deep power-down mode.

8.23.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP. For details, see the *LPC82x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION	
	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

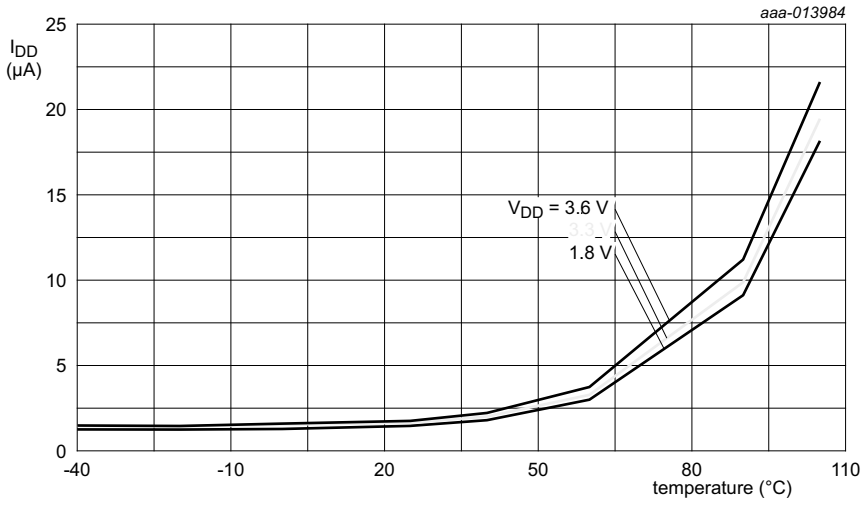
In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled. For details, see the *LPC82x user manual*.

8.23.4 APB interface

The APB peripherals are located on one APB bus.

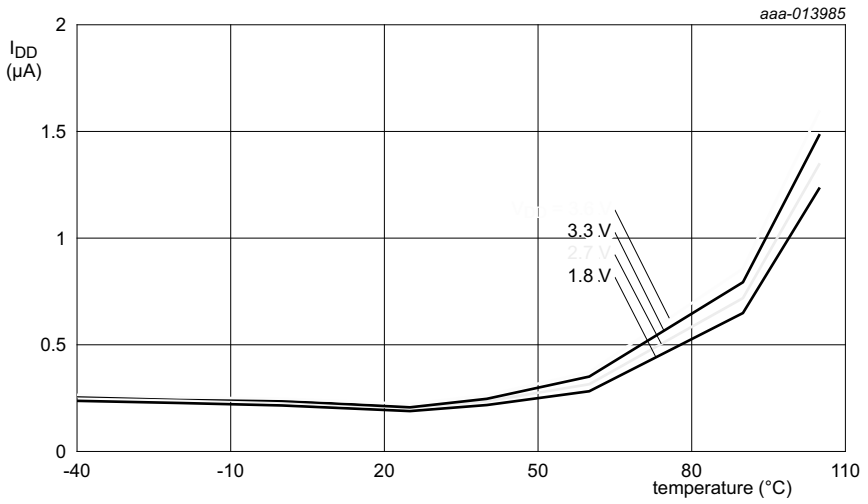
8.23.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0+ to the flash memory, the main static RAM, the CRC, the DMA, the ROM, and the APB peripherals.



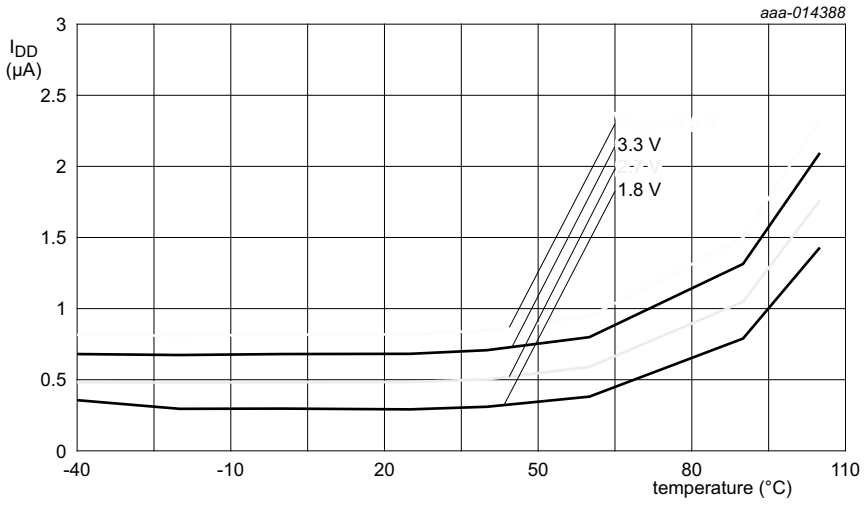
Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 17. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



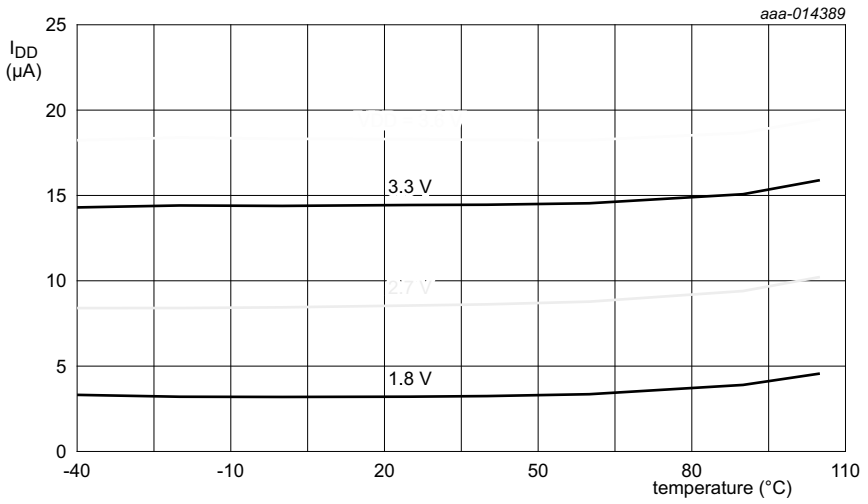
WKT not running.

Fig 18. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



WKT running with external 32 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

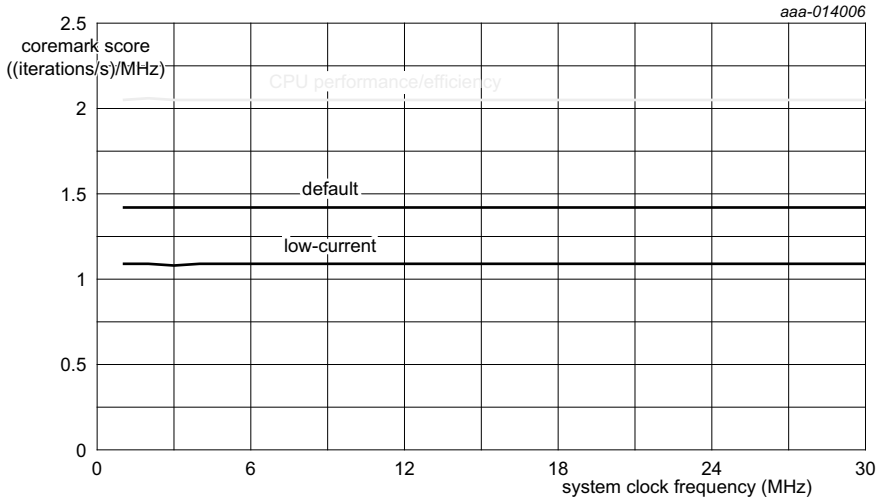
Fig 21. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 32 kHz input clock)



WKT running with external 1 MHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 22. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 1 MHz input clock)

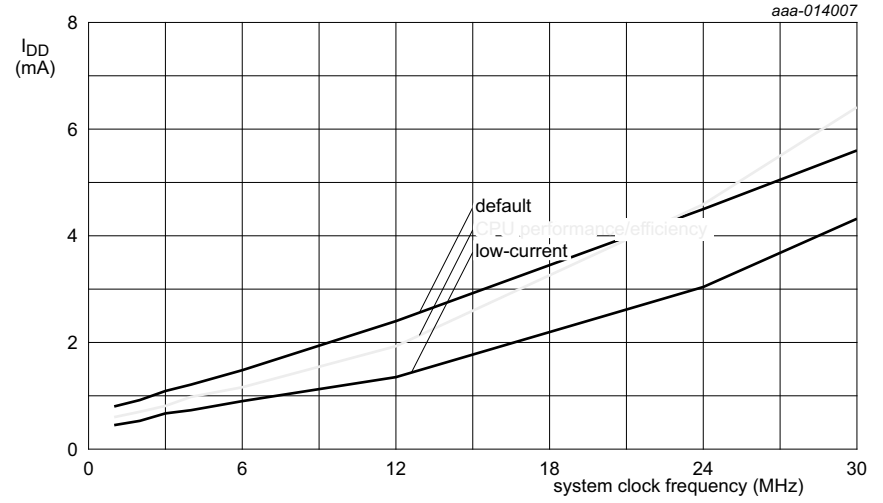
11.5 CoreMark data



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; BOD disabled; internal pull-up resistors enabled. Measured with Keil uVision 5.10.

1 MHz - 6 MHz: external clock; IRC, PLL disabled.12 MHz: IRC enabled; PLL disabled. 24 MHz: IRC enabled; PLL enabled.30 MHz: system oscillator enabled; PLL enabled.

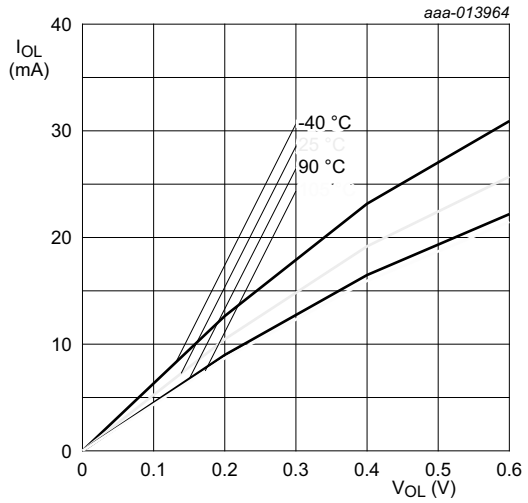
Fig 23. CoreMark score



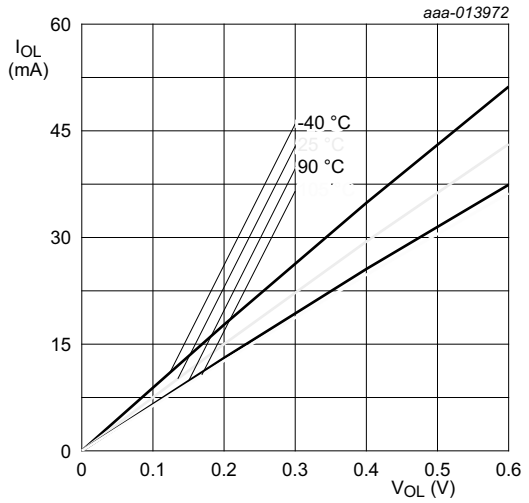
Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; BOD disabled; internal pull-up resistors enabled. Measured with Keil uVision 5.10.

1 MHz - 6 MHz: external clock; IRC, PLL disabled.12 MHz: IRC enabled; PLL disabled.24 MHz: IRC enabled; PLL enabled.30 MHz: system oscillator enabled; PLL enabled.

Fig 24. Active mode: CoreMark power consumption I_{DD}

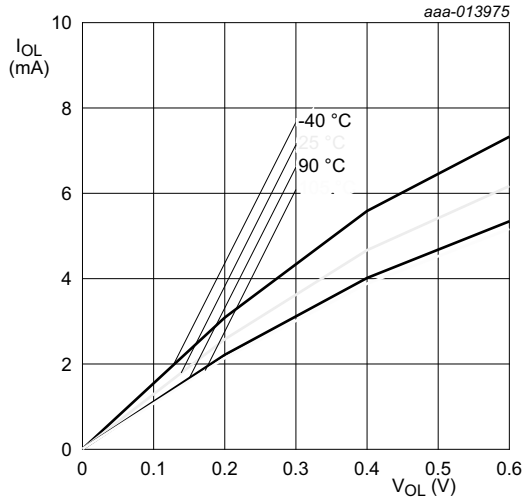


Conditions: V_{DD} = 1.8 V; on pins PIO0_10 and PIO0_11.

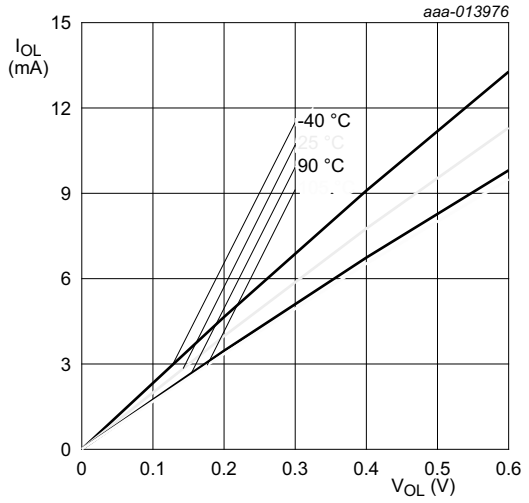


Conditions: V_{DD} = 3.3 V; on pins PIO0_10 and PIO0_11.

Fig 26. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_12.



Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_12.

Fig 27. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

12. Dynamic characteristics

12.1 Power-up ramp conditions

Table 11. Power-up characteristics

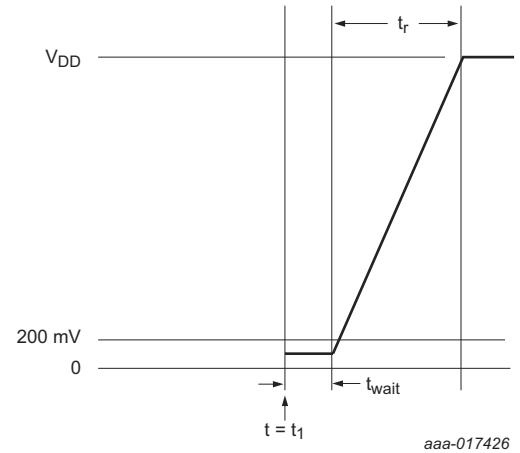
T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < V_I ≤ 200 mV	[1][3]	0	-	500	ms
t_{wait}	wait time		[1][2][3]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}	[3]	0	-	200	mV

[1] See Figure 31.

[2] The wait time specifies the time the power supply must be at levels below 200 mV before ramping up. See the LPC82x errata sheet.

[3] Based on characterization, not tested in production.



Condition: 0 < V_I ≤ 200 mV at start of power-up (t = t_1)

Fig 31. Power-up ramp

12.2 Flash/EEPROM memory

Table 12. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles

12.4 Internal oscillators

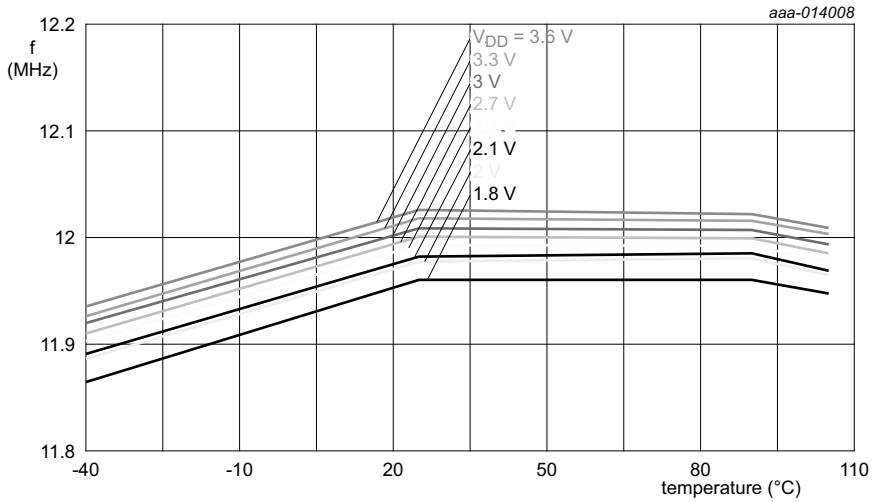
Table 14. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.82	12	12.18	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1.5 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1.5 % accuracy specification for voltages below 2.7 V.

Fig 33. Typical Internal RC oscillator frequency versus temperature

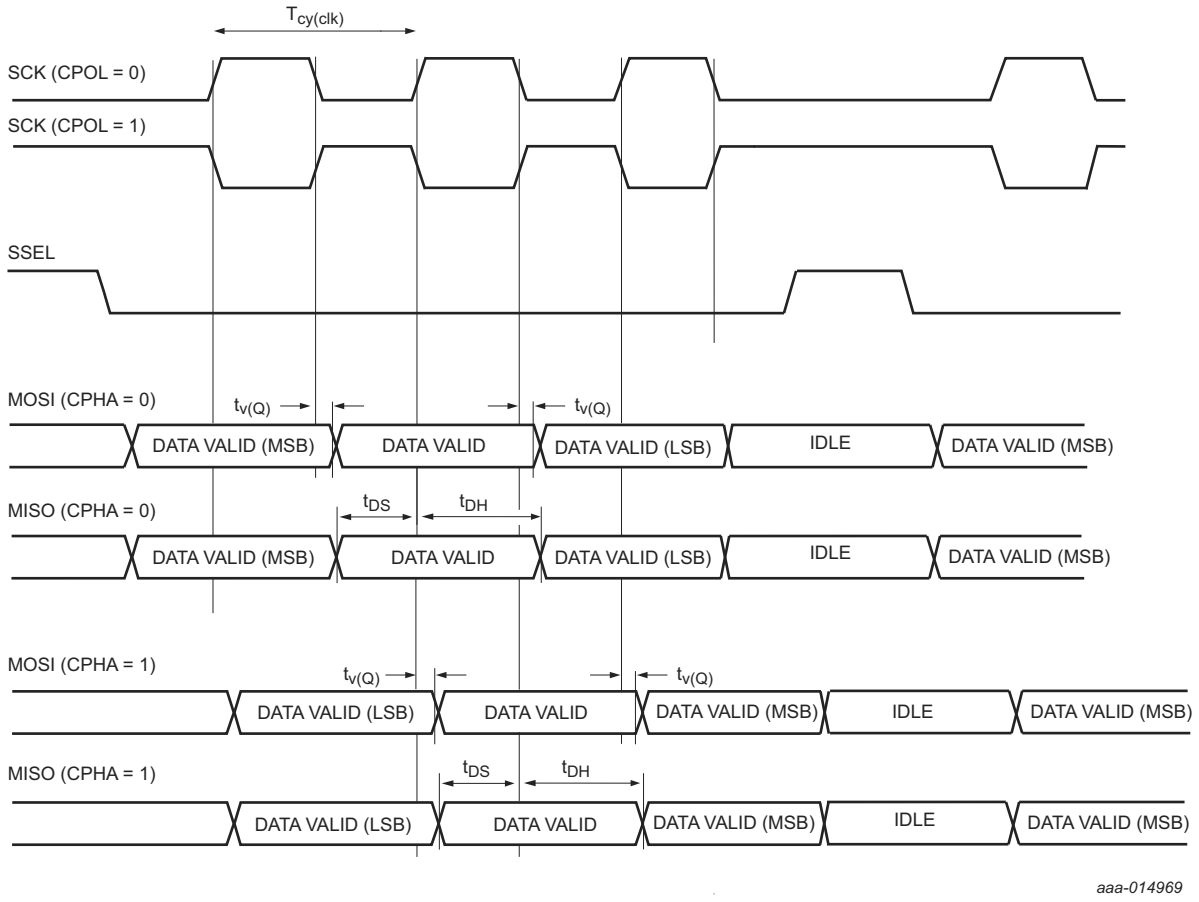
Table 15. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] See the LPC82x *user manual.*



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the LPC82x *User manual*.

Fig 35. SPI master timing

12.4.6 USART interface

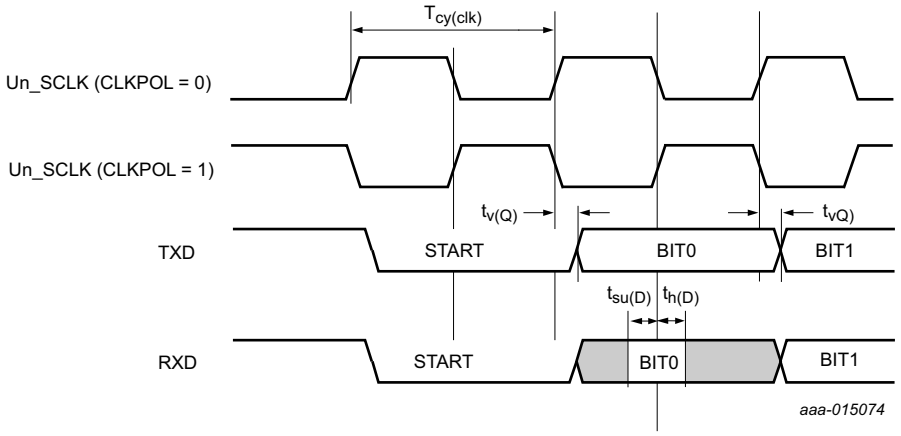
The maximum USART bit rate is 10 Mbit/s in synchronous mode master mode and 10 Mbit/s in synchronous slave mode.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 21. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V <= V_{DD} <= 3.6 V unless noted otherwise; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 30 %/70 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time	3.0 V <= V_{DD} <= 3.6 V	31	-	ns
		1.8 V <= V_{DD} < 3.0 V	37		
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		0	5	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		6	-	ns
$t_{h(D)}$	data input hold time		2	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	28	ns
		1.8 V <= V_{DD} < 3.0 V	0	37	ns



In master mode, $T_{cy(clk)}$ = U_PCLK/BRGVAL. See the LPC82x *User manual*.

Fig 37. USART timing

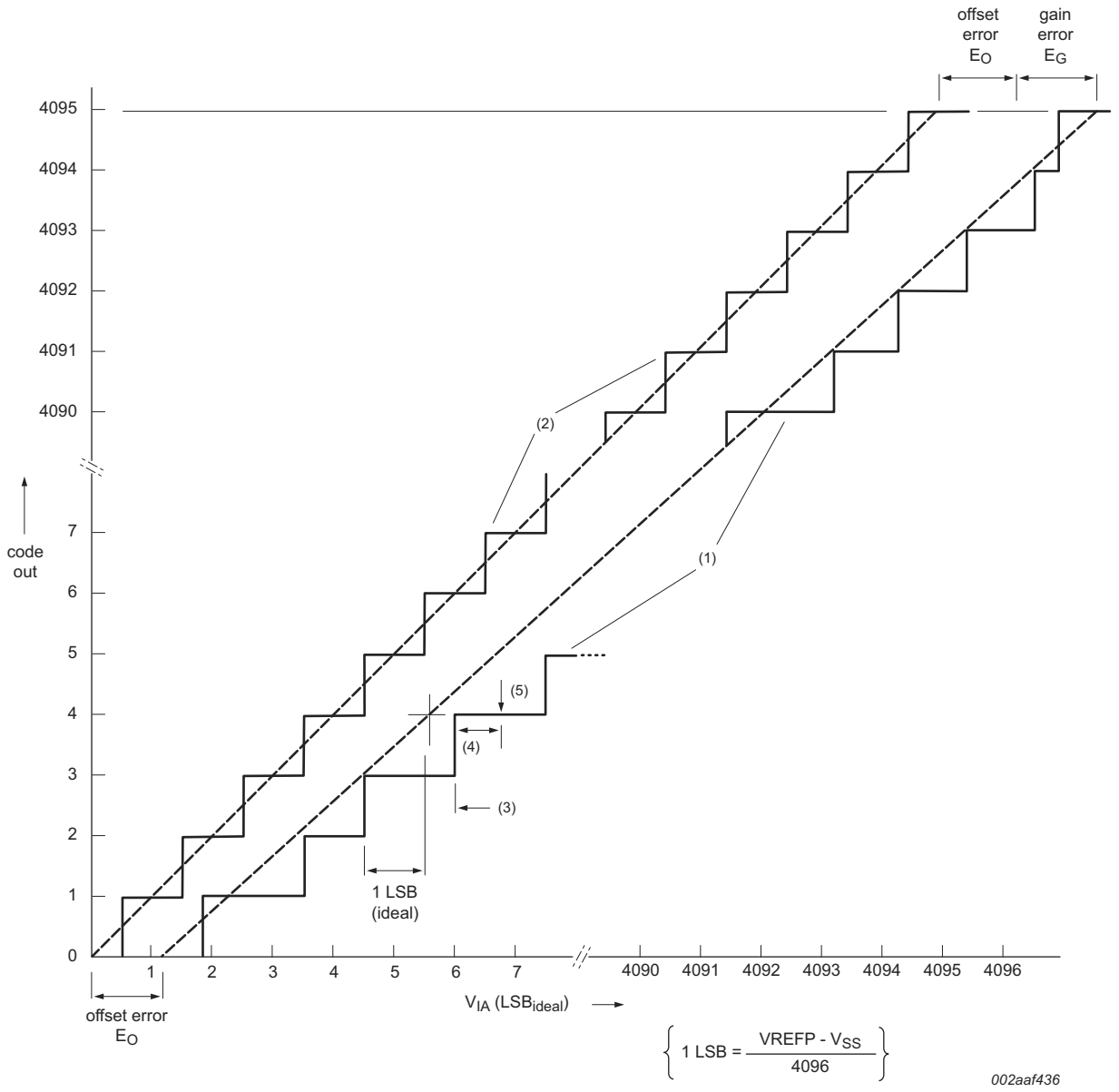
13. Characteristics of analog peripherals

13.1 BOD

Table 22. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.25	-	V
		de-assertion		-	2.40	-	V
		interrupt level 2					
		assertion		-	2.54	-	V
		de-assertion		-	2.68	-	V
		interrupt level 3					
		assertion		-	2.85	-	V
		de-assertion		-	2.95	-	V
		reset level 1					
		assertion		-	2.05	-	V
		de-assertion		-	2.20	-	V
		reset level 2					
		assertion		-	2.34	-	V
		de-assertion		-	2.49	-	V
		reset level 3					
		assertion		-	2.63	-	V
		de-assertion		-	2.78	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC82x *user manual*. Interrupt level 0 is reserved.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

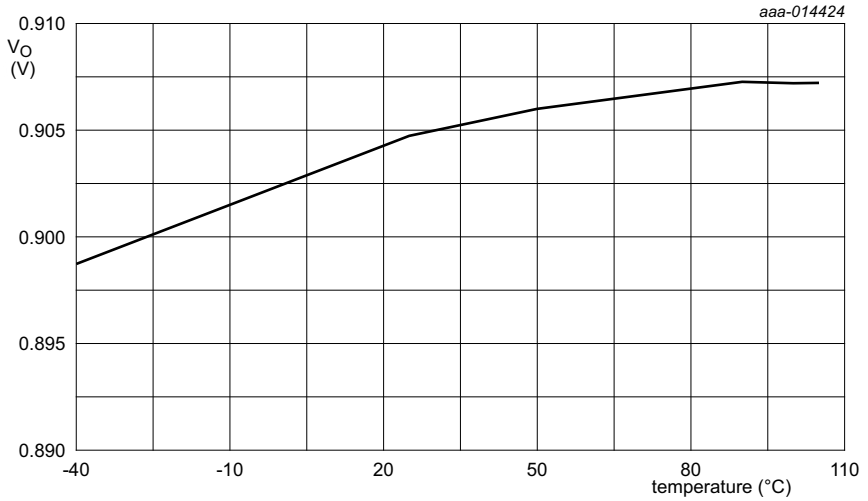
Fig 39. 12-bit ADC characteristics

13.3 Comparator and internal voltage reference

Table 24. Internal voltage reference static and dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 3.3 V; hysteresis disabled in the comparator CTRL register.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = 25 °C to 105°C		860	-	940	mV
		T_{amb} = 25 °C			904		mV



V_{DD} = 3.3 V; characterized through bench measurements on typical samples.

Fig 40. Typical internal voltage reference output voltage

Table 25. Comparator characteristics

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin PIO0_6/VDDCMP configured for function VDDCMP		1.5	-	3.6	V
I_{DD}	supply current	VP > VM; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	90	-	μA
		VM > VP; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	60	-	μA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V; V_{DD} = 2.4 V; T_{amb} = 105 °C	[2]	-	+/- 4	-	mV
		V_{IC} = 1.5 V; V_{DD} = 2.4 V; T_{amb} = 105 °C	[2]	-	+/- 2	-	mV
		V_{IC} = 2.9 V; V_{DD} = 2.4 V; T_{amb} = 105 °C	[2]	-	+/- 4	-	mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process; V_{DD} = 3.3 V; T_{amb} = 25 °C		-	13	-	μs

14. Application information

14.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended to couple the input through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

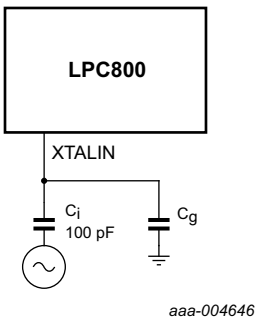
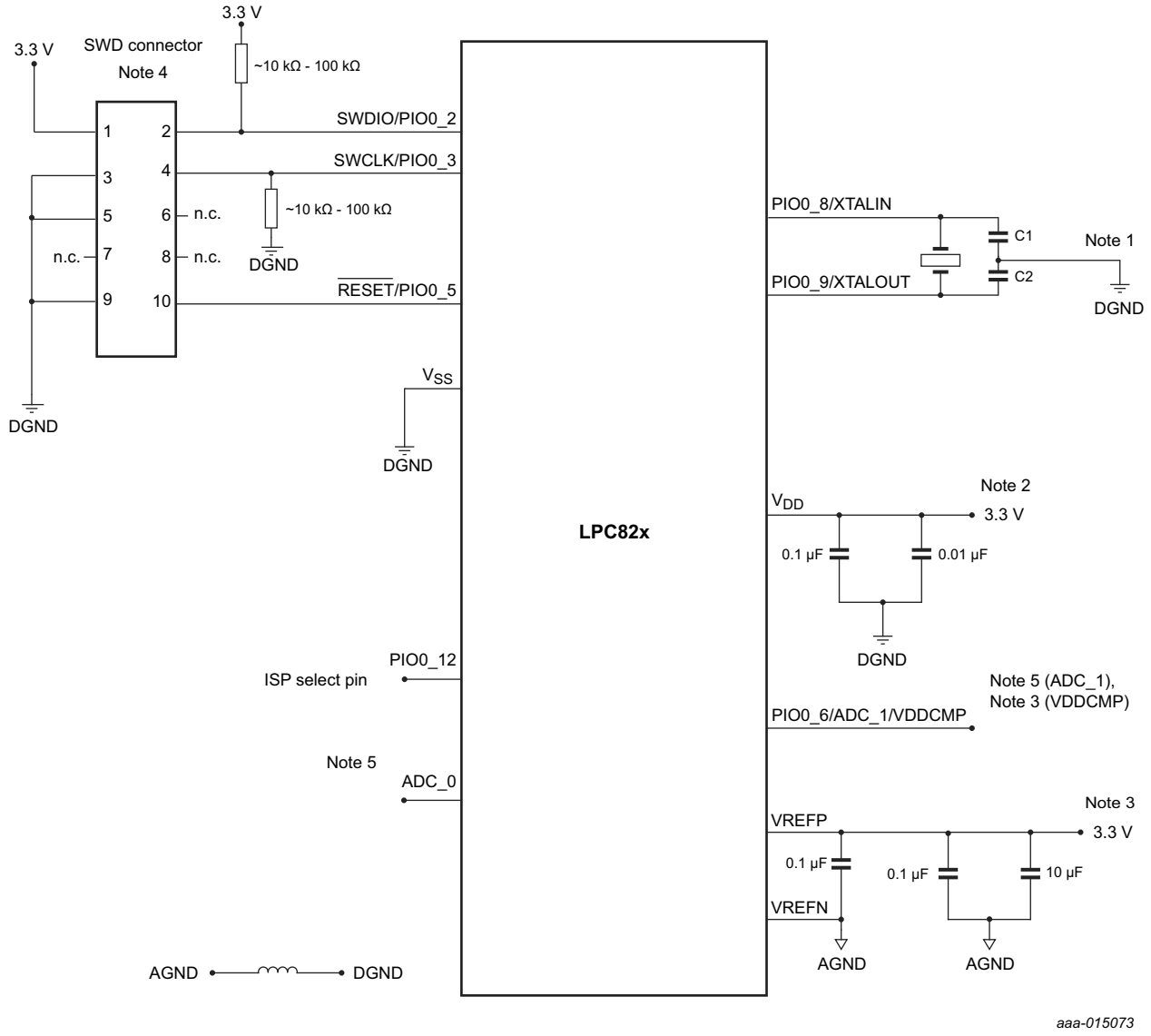


Fig 41. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled with a capacitor of 100 pF (Figure 41), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 42 and in Table 28 and Table 29. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} must be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 42 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 28).



(1) See Section 14.1 “XTAL input” for the values of C1 and C2.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DD} pins. The 10 µF bypass capacitor filters the power line. Tie VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

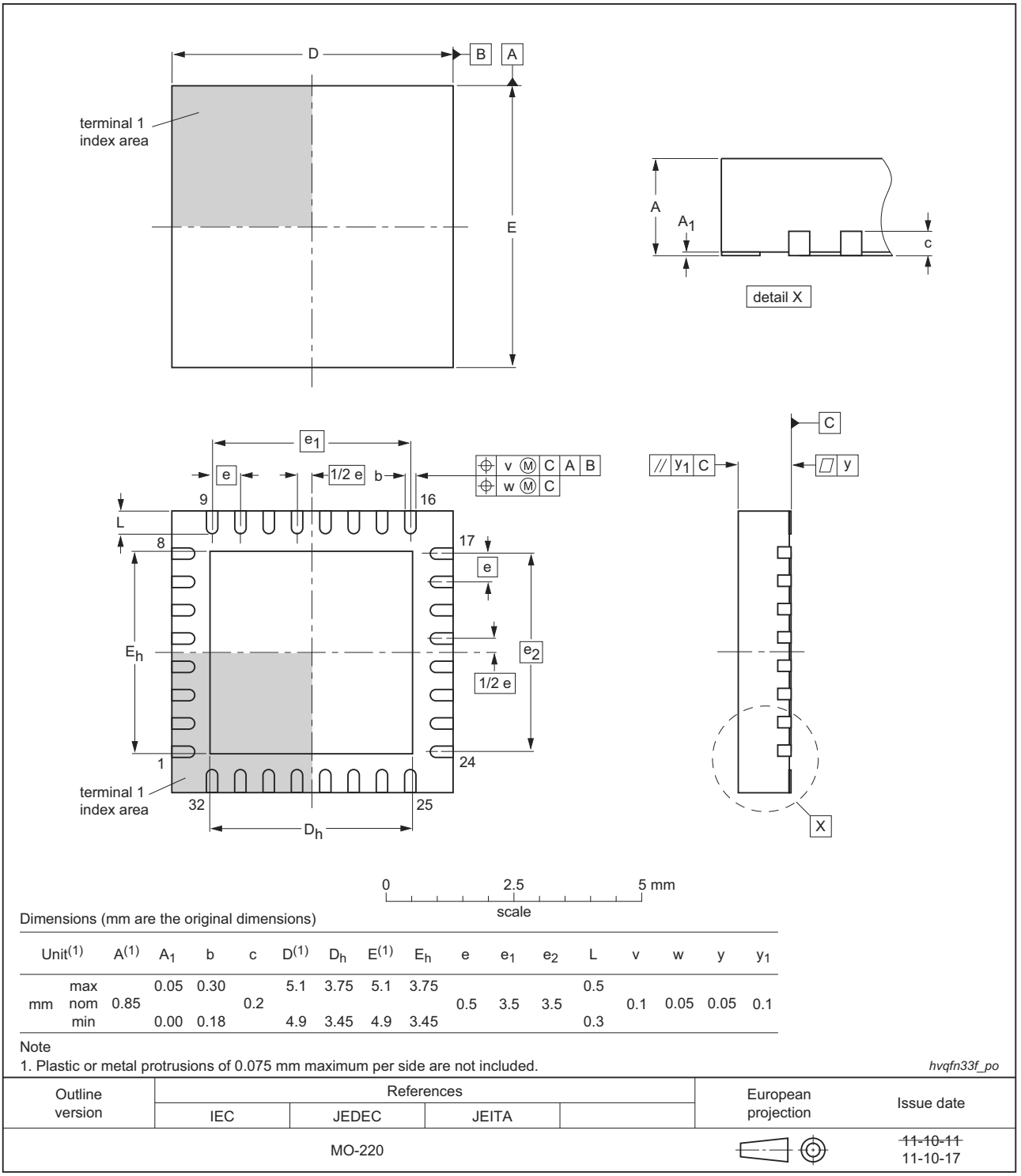
(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 4.

Fig 43. Power, clock, and debug connections

14.4 Termination of unused pins

Table 30 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max		0.05	0.30		5.1	3.75	5.1	3.75				0.5				
	nom	0.85			0.2					0.5	3.5	3.5		0.1	0.05	0.05	0.1
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 45. Package outline (HVQFN33 5x5)

17. Abbreviations

Table 32. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] LPC82x User manual UM10800: http://www.nxp.com/documents/user_manual/UM10800.pdf

[2] LPC82x Errata sheet: http://www.nxp.com/documents/errata_sheet/ES_LPC82X.pdf

[3] I2C-bus specification *UM10204*.

[4] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf