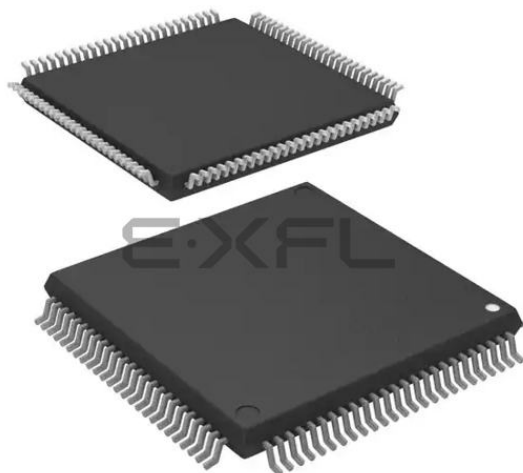




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 14x12b; D/A 1x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mfcdfp-v0

Table 1.1 Outline of Specifications (2/10)

Classification	Module/Function	Description
Operating modes		- Operating modes by the mode-setting pins at the time of release from the reset state - Single-chip mode - Boot mode (for the SCI interface) - Boot mode (for the USB interface) - User boot mode - Selection of operating mode by register setting - Single-chip mode, user boot mode - On-chip ROM disabled extended mode - On-chip ROM enabled extended mode - Endian selectable
Clock	Clock generation circuit	- Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDI-dedicated on-chip oscillator - The peripheral module clocks can be set to frequencies above that of the system clock. - Main-clock oscillation stoppage detection - Separate frequency-division and multiplication settings for the system clock (ICKL), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) - The CPU and other bus masters run in synchronization with the system clock (ICKL): Up to 240 MHz - Peripheral modules of MTU3, GPT, RSPI, SCIFA, USBA, ETHERC, EPTPC, EDMAC, and AES run in synchronization with PCLKA, which operates at up to 120 MHz. - Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz - ADCLK in the SD12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz - ADCLK in the SD12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz - Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz - Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz - Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Nine types of reset - RES# pin reset: Generated when the RES# pin is driven low. - Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises. - Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls. - Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls. - Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls. - Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. - Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. - Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. - Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or internal interrupt. - Voltage detection circuit 0 - Capable of generating an internal reset - The option-setting memory can be used to select enabling or disabling of the reset. - Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, and 2.80 V) - Voltage detection circuits 1 and 2 - Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, and 2.85 V) - Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) - Capable of generating an internal reset - Two types of timing are selectable for release from reset - An internal interrupt can be requested. - Detection of voltage rising above and falling below thresholds is selectable. - Maskable or non-maskable interrupt is selectable - Voltage detection monitoring - Event linking

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/3)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX71M	R5F571MLCDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available

1.3 Block Diagram

Figure 1.2 shows a block diagram.

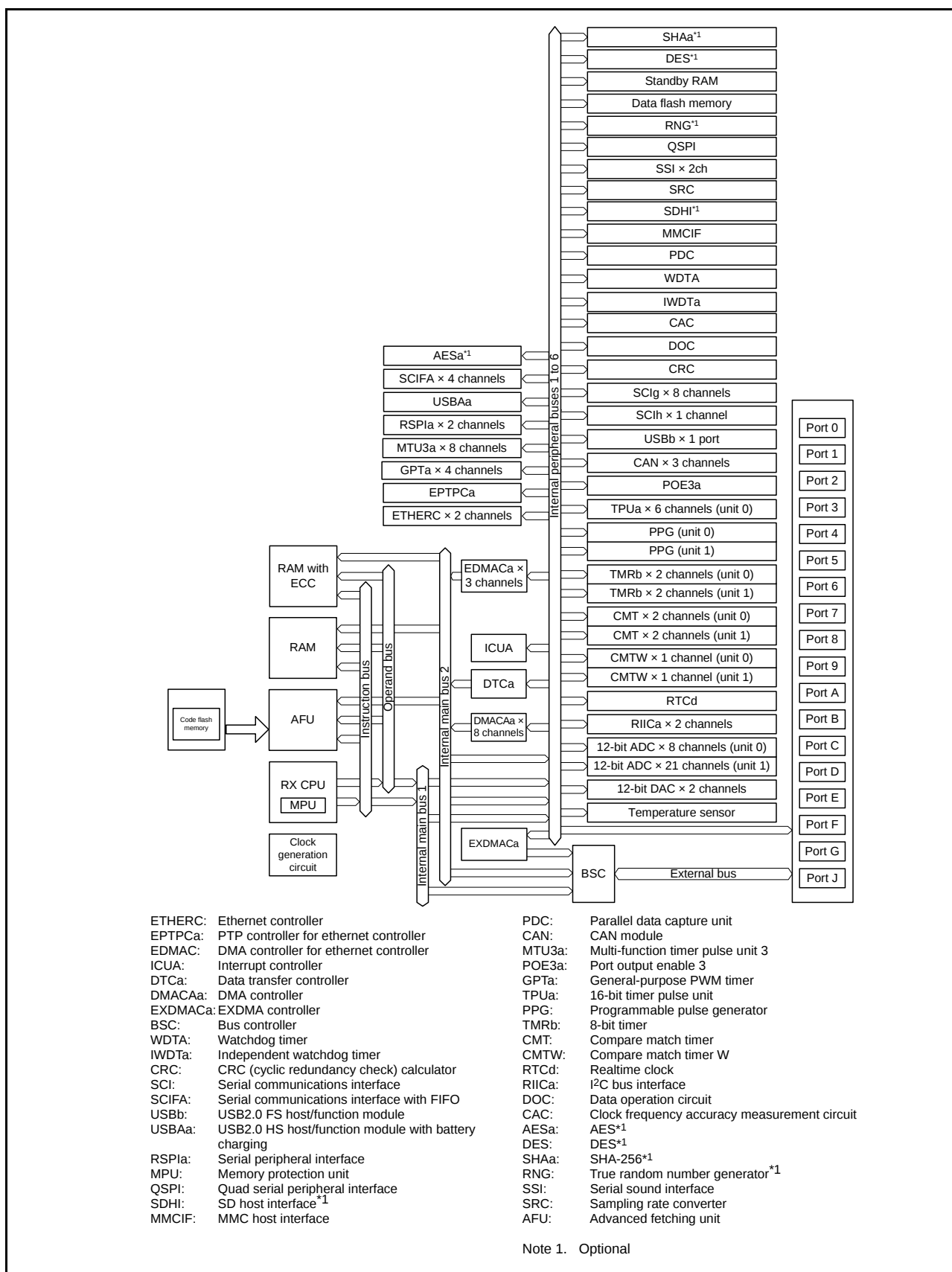


Figure 1.2 Block Diagram

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strobe signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU or GPT in the high impedance state

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
A1	AVSS0							
A2	AVCC0							
A3	VREFL0							
A4		P42					IRQ10-DS	AN002
A5		P46					IRQ14-DS	AN006
A6	VCC							
A7	VSS							
A8		P94	A20/D20		ET1_ERXD0/ RMII1_RXD0			
A9	VCC							
A10		P97	A23/D23		ET1_ERXD3			
A11		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
A12		P60	CS0#		ET1_TX_EN/ RMII1_TXD_EN			
A13		P63	CS3#/CAS#					
A14		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
A15		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXD12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
B1		P05					IRQ13	DA1
B2		P07					IRQ15	ADTRG0#
B3		P40					IRQ8-DS	AN000
B4		P41					IRQ9-DS	AN001
B5		P47					IRQ15-DS	AN007
B6		P91	A17/D17		ET1_COL/SCK7			AN115
B7		P92	A18/D18	POE4#	ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7			AN116
B8		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
B9		P96	A22/D22		ET1_ERXD2			
B10		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
B11		PG1	D25		ET1_RX_ER/ RMII1_RX_ER			
B12	VSS							
B13		P64	CS4#/WE#					
B14		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
B15		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ ET0_ERXD3	MMC_D7-B		AN101
C1	AVSS1							
C2	AVCC1							
C3	VREFH0							

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (5/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
110		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ ET0_MDIO		IRQ6-DS	
111	TRDATA3	PG7	D31		ET1_TX_ER			
112		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
113	TRDATA2	PG6	D30		ET1_ETXD3			
114		PA1	A1/DQM3	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOC0B/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
115	VCC							
116	TRCLK	PG5	D29		ET1_ETXD2			
117	VSS							
118		PA0	A0/BC0#/ DQM2	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
119	TRSYNC	PG4	D28		ET1_ETXD1/ RMII1_TXD1			
120		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
121	TRDATA1	PG3	D27		ET1_ETXD0/ RMII1_TXD0			
122		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
123	TRDATA0	PG2	D26		ET1_TX_CLK			
124		P65	CS5#/CKE					
125		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
126		PE6	D14[A14/D14]	MTIOC6C/ GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
127	VCC							
128		P70	SDCLK					
129	VSS							
130		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
131		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
132		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ ET0_ERXD3	MMC_D7-B		AN101
133		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RDX12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
134		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TDX12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
135		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
136		P64	CS4#/WE#					
137		P63	CS3#/CAS#					
138		P62	CS2#/RAS#					
139		P61	CS1#/SDCS#					
140	VSS							

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/4)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
F5		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCLO[FM+]		IRQ2	
F6		PB3	A11	MTIOC0A/MTIOC4A/ TIOC03/TCLKD/ TMO0/PO27/POE11#	SCK6/ET0_RX_ER/ RMII0_RX_ER			
F7		PB2	A10	TIOCC3/TCLKC/ PO26	CTS6#/RTS6#SS6#/ ET0_RX_CLK/ REF50CK0			
F8		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
F9		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
F10	VSS							
G1		P33	EDREQ1	MTIOC0D/TIOC0D/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0		IRQ3-DS	
G2	TMS	P31		MTIOC4D/TMCI2/ PO9/RTIC1	CTS1#/RTS1#SS1#/ SSLB0-A		IRQ1-DS	
G3	TDI	P30		MTIOC4B/TMRI3/ PO8/RTIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS	
G4	TCK	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB-A			
G5		P53	BCLK					
G6		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
G7		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
G8		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
G9		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
G10	VCC							
H1	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A			
H2		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1			ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SSCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
H4		P15		MTIOC0B/MTCLKB/ GTETR-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1		IRQ5	
H5		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
H6		P54	ALE/ EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#SS2#/ CTX1/ET0_LINKSTA			
H7	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL		IRQ14	

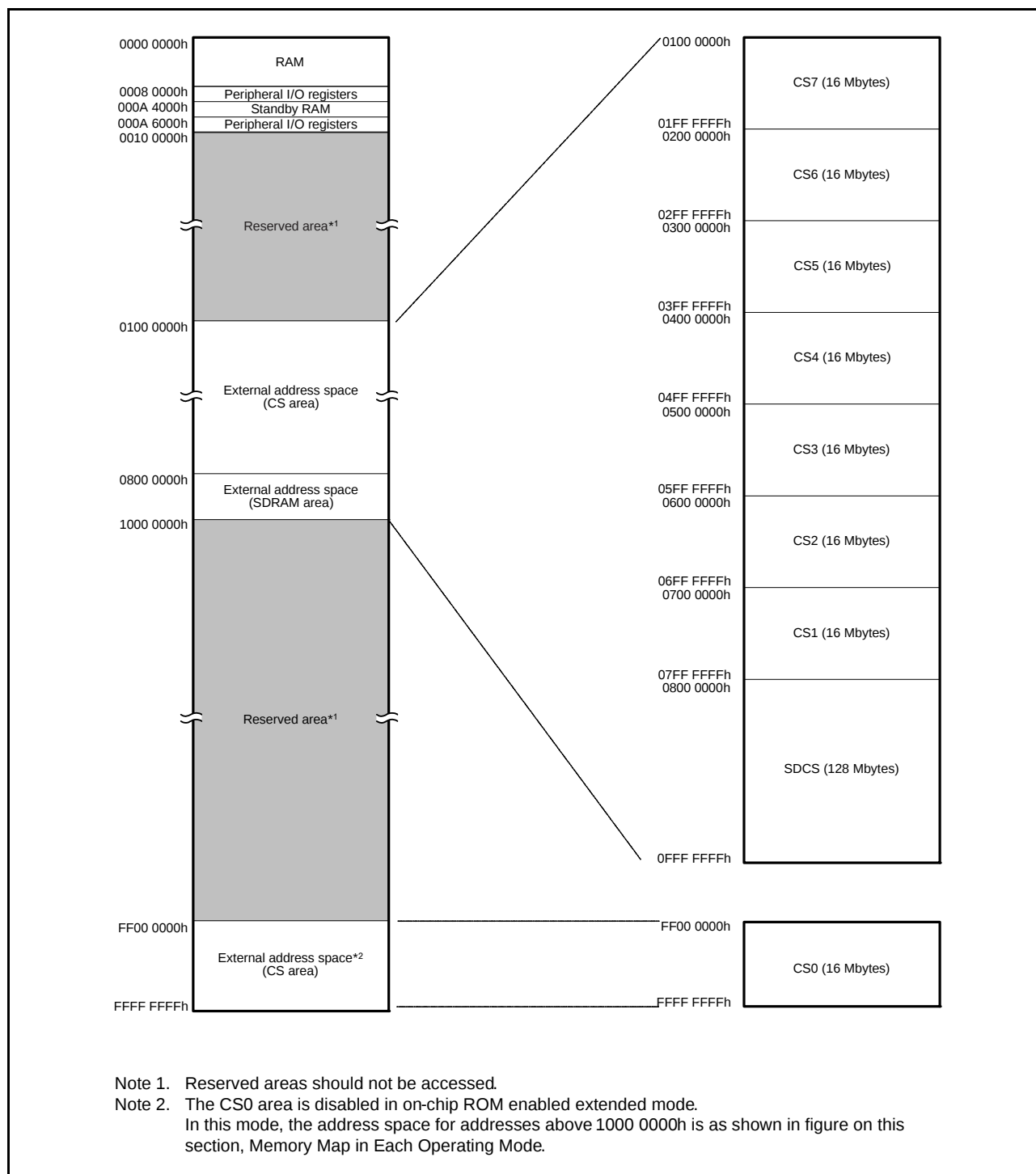
Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/4)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	
H9		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
H10		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
J1		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1			
J2		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0		IRQ9	
J3		P17		MTIOC3A/MTIOC3B/ MTIOC4B/GTIOC0B- B/TIOCB0/TCLKD/ TMO1/PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0		IRQ7	ADTRG1#
J4		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
J5	VSS_USB							
J6	VCC_USB							
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRQ-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/SSLA0- A/ET0_TX_CLK			
J9		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
J10		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
K1		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0			
K2		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK			
K3		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0		IRQ8	
K4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
K5					USB0_DM			
K6					USB0_DP			
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2			
K9		PC3	A19	MTIOC4D/GTIOC1B- D/TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
K10		PC2	A18	MTIOC4B/GTIOC2B- D/TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			

3.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7) and SDRAM area (SDCS). The CS areas are divided into up to eight areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM areas (SDCS) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

Table 4.1 List of I/O Registers (Address Order) (8 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7400h	ICU	DMAC Start Source Select Register 0	DMRSR0	8	8	2 ICLK		ICUA
0008 7404h	ICU	DMAC Start Source Select Register 1	DMRSR1	8	8	2 ICLK		ICUA
0008 7408h	ICU	DMAC Start Source Select Register 2	DMRSR2	8	8	2 ICLK		ICUA
0008 740Ch	ICU	DMAC Start Source Select Register 3	DMRSR3	8	8	2 ICLK		ICUA
0008 7410h	ICU	DMAC Start Source Select Register 4	DMRSR4	8	8	2 ICLK		ICUA
0008 7414h	ICU	DMAC Start Source Select Register 5	DMRSR5	8	8	2 ICLK		ICUA
0008 7418h	ICU	DMAC Start Source Select Register 6	DMRSR6	8	8	2 ICLK		ICUA
0008 741Ch	ICU	DMAC Start Source Select Register 7	DMRSR7	8	8	2 ICLK		ICUA
0008 7500h to 0008 750Fh	ICU	IRQ Control Registers 0 to 15	IRQCR0 to 15	8	8	2 ICLK		ICUA
0008 7520h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK		ICUA
0008 7521h	ICU	IRQ Pin Digital Filter Enable Register 1	IRQFLTE1	8	8	2 ICLK		ICUA
0008 7528h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK		ICUA
0008 752Ah	ICU	IRQ Pin Digital Filter Setting Register 1	IRQFLTC1	16	16	2 ICLK		ICUA
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK		ICUA
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK		ICUA
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK		ICUA
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK		ICUA
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK		ICUA
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK		ICUA
0008 7600h	ICU	Group BE0 Interrupt Request Register	GRPBEO	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7630h	ICU	Group BE0 Interrupt Request Register	GRPBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7634h	ICU	Group BL1 Interrupt Request Register	GRPBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7640h	ICU	Group BE0 Interrupt Request Enable Register	GENBEO	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7670h	ICU	Group BL0 Interrupt Request Enable Register	GENBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7674h	ICU	Group BL1 Interrupt Request Enable Register	GENBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7680h	ICU	Group BE0 Interrupt Clear Register	GCRBEO	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7700h	ICU	Software Configurable Interrupt B Request Register 0	PIBR0	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7701h	ICU	Software Configurable Interrupt B Request Register 1	PIBR1	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7702h	ICU	Software Configurable Interrupt B Request Register 2	PIBR2	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7703h	ICU	Software Configurable Interrupt B Request Register 3	PIBR3	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7704h	ICU	Software Configurable Interrupt B Request Register 4	PIBR4	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7705h	ICU	Software Configurable Interrupt B Request Register 5	PIBR5	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7706h	ICU	Software Configurable Interrupt B Request Register 6	PIBR6	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7707h	ICU	Software Configurable Interrupt B Request Register 7	PIBR7	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7708h	ICU	Software Configurable Interrupt B Request Register 8	PIBR8	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7709h	ICU	Software Configurable Interrupt B Request Register 9	PIBR9	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 770Ah	ICU	Software Configurable Interrupt B Request Register A	PIBRA	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7780h	ICU	Software Configurable Interrupt B Select Register 128	SLIBXR128	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7781h	ICU	Software Configurable Interrupt B Select Register 129	SLIBXR129	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7782h	ICU	Software Configurable Interrupt B Select Register 130	SLIBXR130	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (35 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C428h	RTC	RTC Control Register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ah	RTC	Frequency Register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ch	RTC	Frequency Register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C440h	RTC	Time Capture Control Register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C442h	RTC	Time Capture Control Register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C444h	RTC	Time Capture Control Register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	Second Capture Register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	BCNT0 Capture Register 0	BCNT0CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	Minute Capture Register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	BCNT1 Capture Register 0	BCNT1CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	Hour Capture Register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	BCNT2 Capture Register 0	BCNT2CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	Date Capture Register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	BCNT3 Capture Register 0	BCNT3CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ch	RTC	Month Capture Register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C462h	RTC	Second Capture Register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C462h	RTC	BCNT0 Capture Register 1	BCNT0CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C464h	RTC	Minute Capture Register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C464h	RTC	BCNT1 Capture Register 1	BCNT1CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C466h	RTC	Hour Capture Register 1	RHRCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C466h	RTC	BCNT2 Capture Register 1	BCNT2CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ah	RTC	Date Capture Register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ah	RTC	BCNT3 Capture Register 1	BCNT3CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ch	RTC	Month Capture Register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C472h	RTC	Second Capture Register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C472h	RTC	BCNT0 Capture Register 2	BCNT0CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C474h	RTC	Minute Capture Register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C474h	RTC	BCNT1 Capture Register 2	BCNT1CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C476h	RTC	Hour Capture Register 2	RHRCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C476h	RTC	BCNT2 Capture Register 2	BCNT2CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ah	RTC	Date Capture Register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ah	RTC	BCNT3 Capture Register 2	BCNT3CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ch	RTC	Month Capture Register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C4C0h	POE3	Input Level Control/Status Register 1	ICSR1	16	16	2, 3 PCLKB	2 ICLK	POE3
0008 C4C2h	POE3	Output Level Control/Status Register 1	OCSR1	16	16	2, 3 PCLKB	2 ICLK	POE3

Table 4.1 List of I/O Registers (Address Order) (41 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0080h	USB0	Pipe9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 009Ah	USB0	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 009Ch	USB0	Pipe4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 009Eh	USB0	Pipe4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00A0h	USB0	Pipe5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00A2h	USB0	Pipe5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00F0h	USB0	PHY Cross Point Adjustment Register	PHYSLEW	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb

Table 4.1 List of I/O Registers (Address Order) (63 / 67)

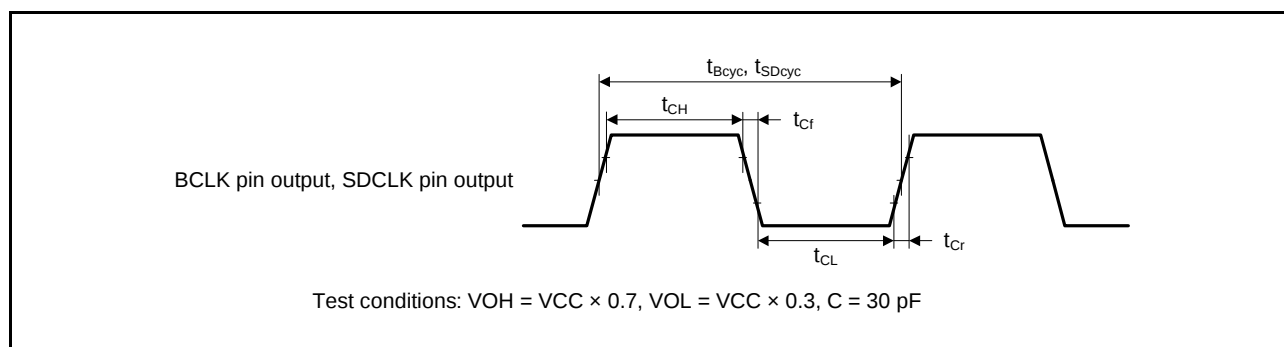
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 0456h	USBA	USB Request Value Register	USBVAL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 0458h	USBA	USB Request Index Register	USBINDX	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 045Ah	USBA	USB Request Length Register	USBLENG	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 045Ch	USBA	DCP Configuration Register	DCPCFG	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 045Eh	USBA	DCP Maximum Packet Size Register	DCPMAXP	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 0460h	USBA	DCP Control Register	DCPCTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 0464h	USBA	Pipe Window Select Register	PIPESEL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 0468h	USBA	Pipe Configuration Register	PIPECFG	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 046Ah	USBA	Pipe Buffer Register	PIPEBUF	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 046Ch	USBA	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa
000D 046Eh	USBA	Pipe Cycle Control Register	PIPEPERI	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBAa

5.3.2 Clock Timing

Table 5.11 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{CC_USBA} = AV_{CC_USBA} = 3.0$ to 3.6 V,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Packages with 177 to 144 pins	t_{Bcyc}	16.6	—	—	ns	Figure 5.3
	Packages with 100 pins or less		33.2	—	—	ns	
BCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
BCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
SDCLK pin output cycle time	Packages with 177 to 144 pins	t_{Bcyc}	16.6	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
SDCLK pin output rising time		t_{Cr}	—	—	5	ns	
SDCLK pin output falling time		t_{Cf}	—	—	5	ns	

**Figure 5.3 BCLK Pin and SDCLK Pin Output Timing**

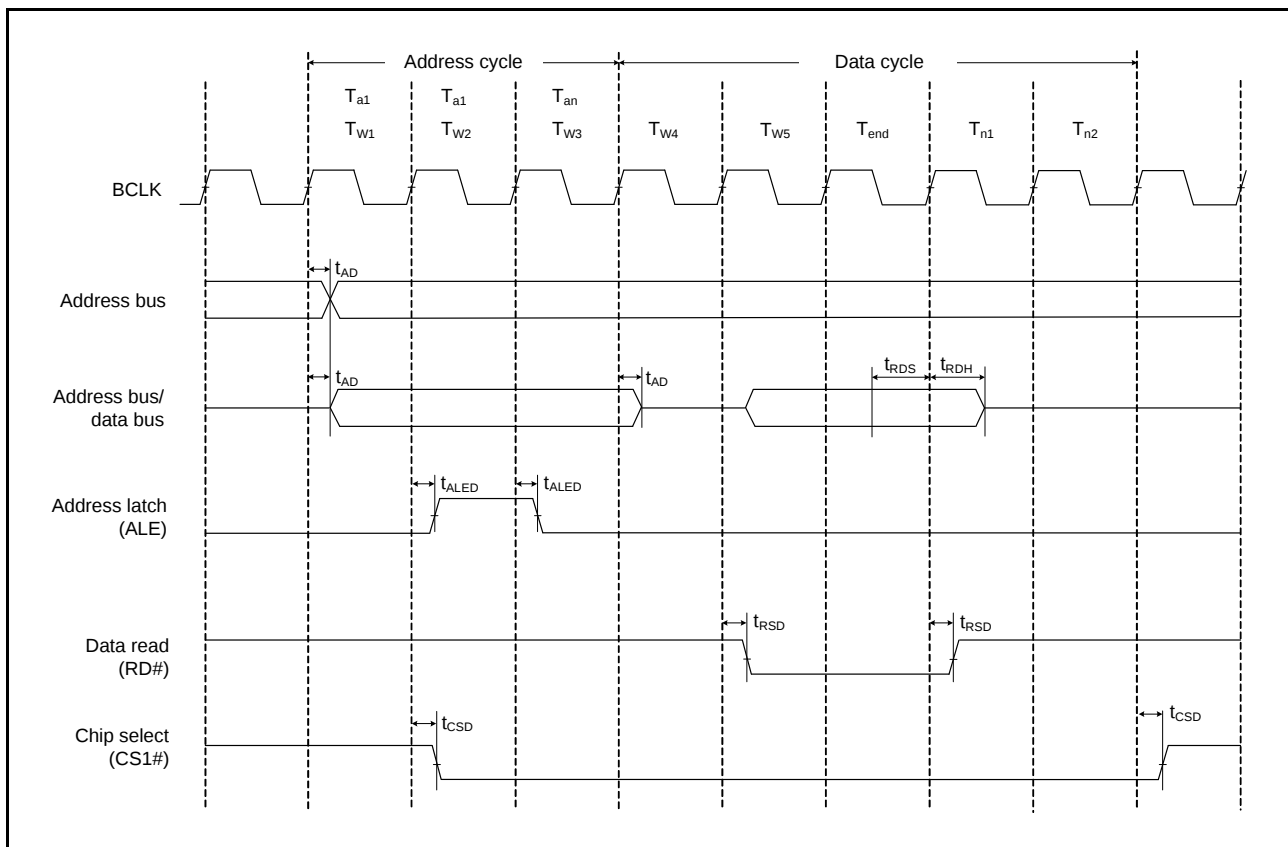


Figure 5.16 Address/Data Multiplexed Bus Read Access Timing

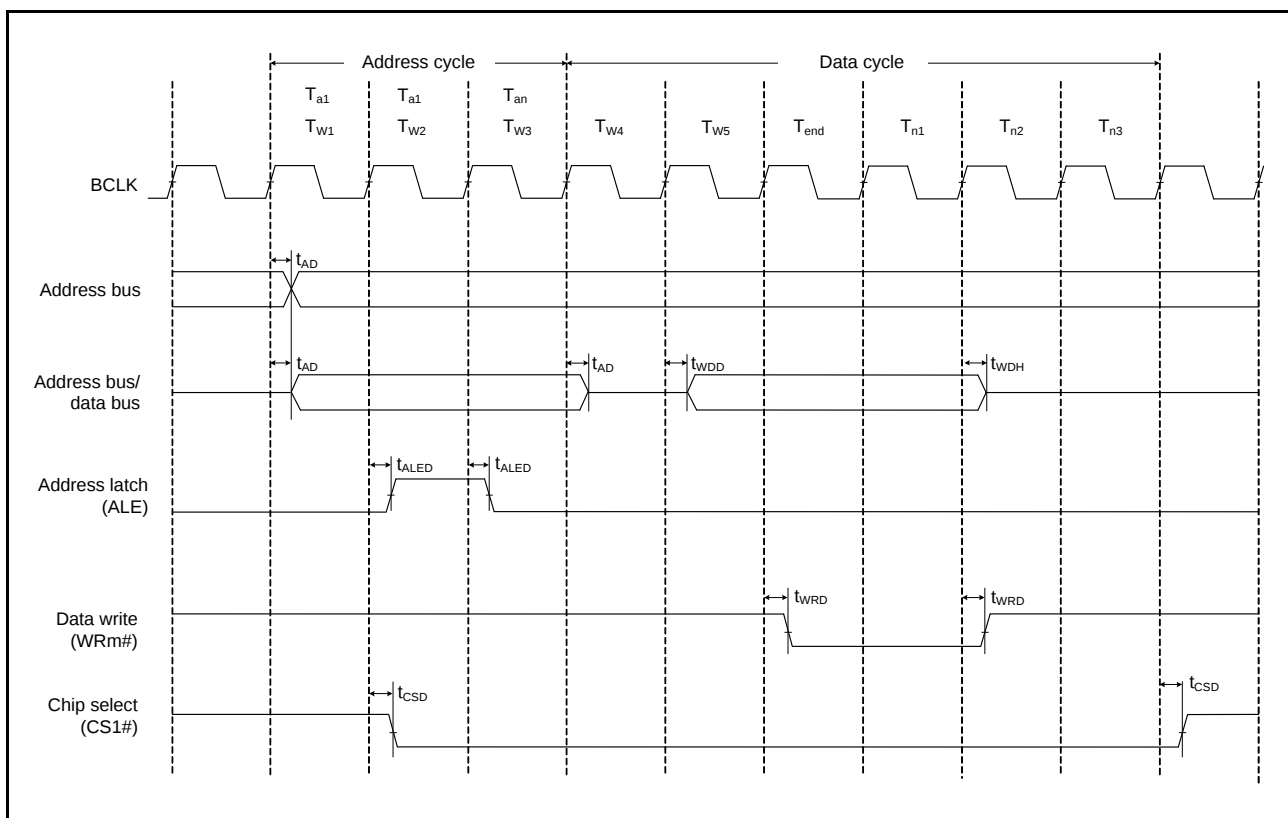


Figure 5.17 Address/Data Multiplexed Bus Write Access Timing

Table 5.34 Simple SPI Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPCyc}	4	65536	t_{PBcyc}	Figure 5.46
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPCyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPCyc}	
	SCK clock rise/fall time	t_{SPCKr} , t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 5.47 to Figure 5.52
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPCyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPCyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	−10	—	ns	
	Data rise/fall time	t_{Dr} , t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr} , t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{PACyc}	Figure 5.51, Figure 5.52
	Slave output release time	t_{REL}	—	5	t_{PACyc}	

Note 1. t_{PBcyc} : PCLKB cycle

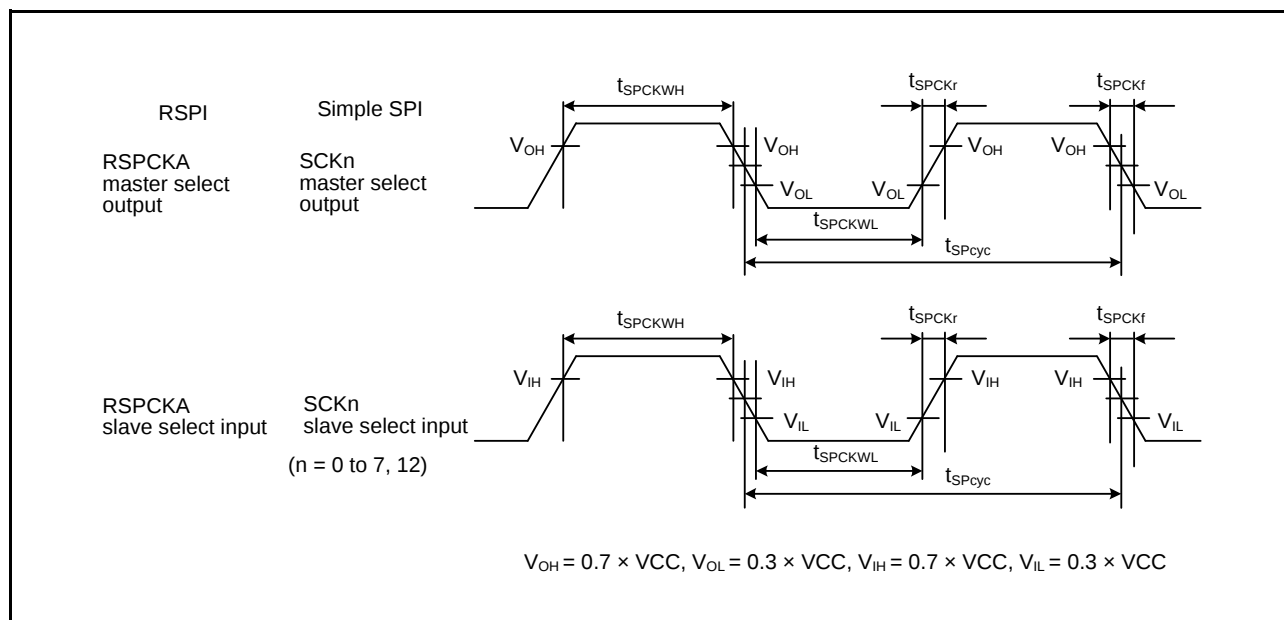
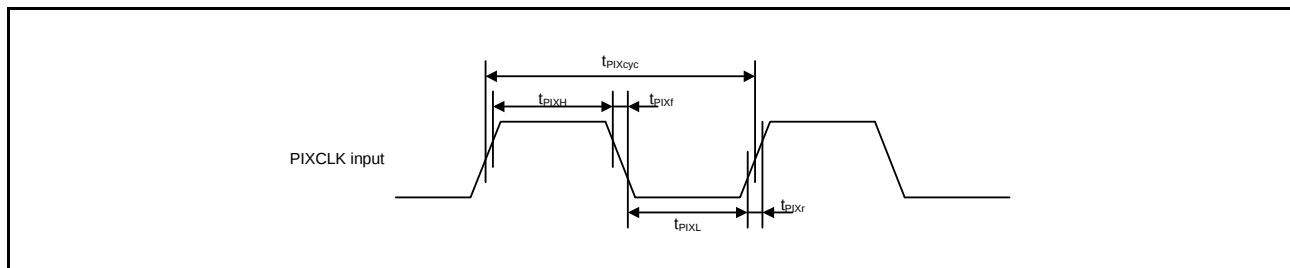
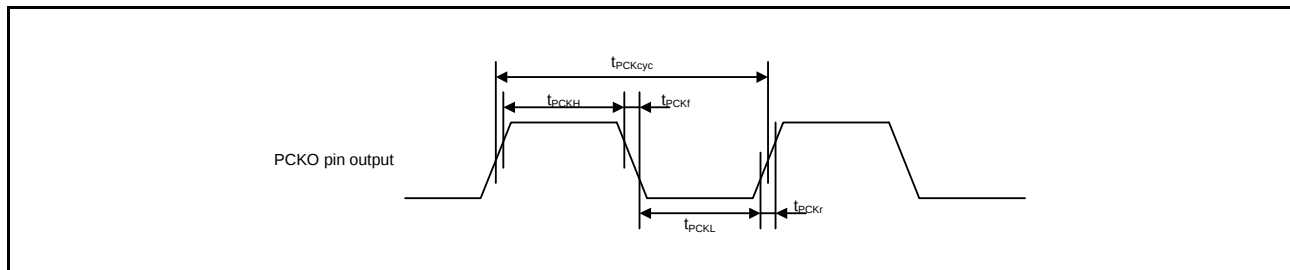
**Figure 5.46 RSPI Clock Timing and Simple SPI Clock Timing**

Table 5.41 PDC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
High-drive output is selected by the driving ability control register.

Item	Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	ns	Figure 5.72
	PIXCLK input high pulse width	t_{PIXH}	10	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	ns	
	PIXCLK rising time	t_{PIXr}	5	ns	
	PIXCLK falling time	t_{PIXf}	5	ns	
	PCKO output cycle time	t_{PCKcyc}	$2 \times t_{PBcyc}$	ns	Figure 5.73
	PCKO output high pulse width	t_{PCKH}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	ns	
	PCKO output low pulse width	t_{PCKL}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	ns	
	PCKO rising time	t_{PCKr}	5	ns	
	PCKO falling time	t_{PCKf}	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	ns	Figure 5.74
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	ns	
	PIXD input setup time	t_{PIXDS}	10	ns	
	PIXD input hold time	t_{PIXDH}	5	ns	

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.72 PDC Input Clock Timing****Figure 5.73 PDC Output Clock Timing**

5.5 A/D Conversion Characteristics

Table 5.46 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{CC_USBA} = AV_{CC_USBA} = 3.0$ to 3.6 V,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PCLKB = PCLKC = 1$ MHz to 60 MHz, $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at $PCLK = 60$ MHz) Permissible signal source impedance (max.) = 1.0 k Ω	1.06 (0.40 + 0.25) *2	—	—	μ s	- Sampling of channel-dedicated sample-and-hold circuits in 24 states - Sampling in 15 states
	Offset error	—	± 1.5	± 3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error	—	± 1.5	± 3.5	LSB	AN000 to AN002 = $V_{REFH0} - 0.25$ V
	Quantization error	—	± 0.5	—	LSB	
	Absolute accuracy	—	± 2.5	± 5.5	LSB	
	DNL differential nonlinearity error	—	± 1.0	± 2.0	LSB	
	INL integral nonlinearity error	—	± 1.5	± 3.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	20	μ s	
	Dynamic range	0.25	—	V_{REFH} 0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at $PCLK = 60$ MHz) Permissible signal source impedance (max.) = 1.0 k Ω	0.48 (0.267) *2	—	—	μ s	Sampling in 16 states
	Offset error	—	± 1.0	± 2.5	LSB	
	Full-scale error	—	± 1.0	± 2.5	LSB	
	Quantization error	—	± 0.5	—	LSB	
	Absolute accuracy	—	± 2.0	± 4.5	LSB	
	DNL differential nonlinearity error	—	± 0.5	± 1.5	LSB	
	INL integral nonlinearity error	—	± 1.0	± 2.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

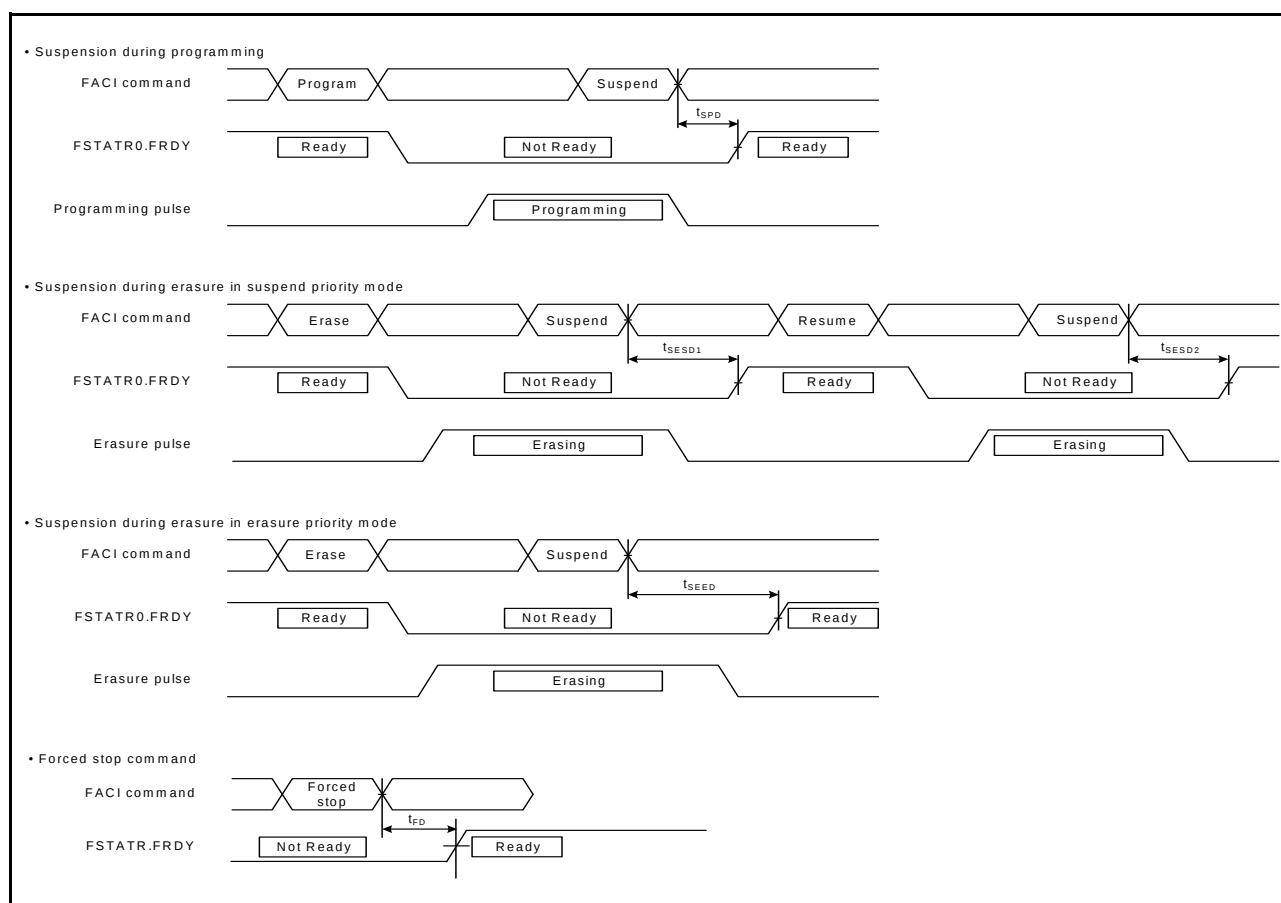


Figure 5.89 Flash Memory Programming/Erasure Suspension Timing

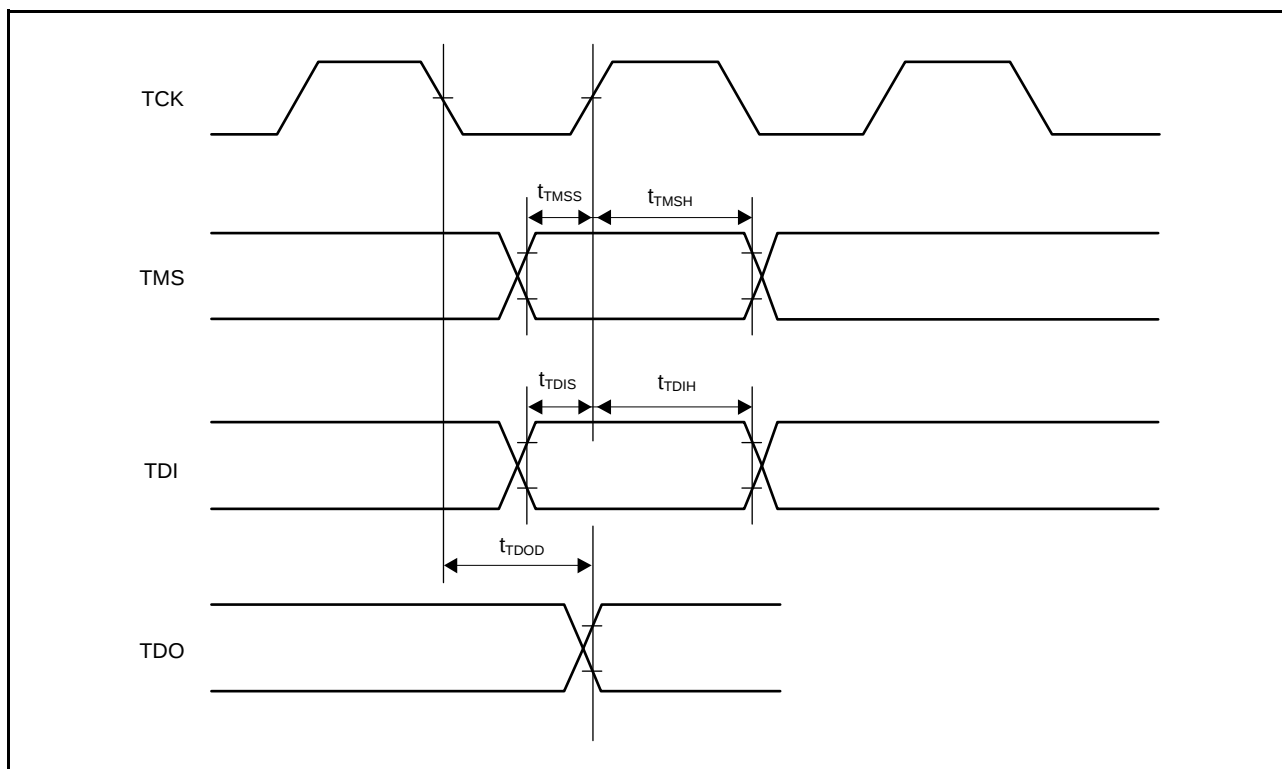


Figure 5.92 Boundary Scan Input/Output Timing