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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mfddfb-v0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.

Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package and the code flash memory capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/10)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 240 MHz 32-bit RX CPU (RXv2) - Minimum instruction execution time: One instruction per state (cycle of the system clock) - Address space: 4-Gbyte linear - Register set of the CPU - General purpose: Sixteen 32-bit registers - Control: Ten 32-bit registers - Accumulator: Two 72-bit registers - Basic instructions: 75 - Floating-point instructions: 11 - DSP instructions: 23 - Addressing modes: 11 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: $32 \times 32 \rightarrow 64$ bits - On-chip divider: $32 / 32 \rightarrow 32$ bits - Barrel shifter: 32 bits
	FPU	- Single precision (32-bit) floating point - Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	Code flash memory	- Capacity: 2 Mbytes, 2.5 Mbytes, 3 Mbytes, 4 Mbytes - No-wait access at up to 120 MHz, single wait access at frequencies above 120 MHz - No-wait access to instructions and operands when the AFU is hit in operation at 240 MHz - On-board programming: Four types - Off-board programming (parallel programmer mode) - The trusted memory (TM) function protects against the reading of programs from blocks 8 and 9.
	Data flash memory	- Capacity: 64 Kbytes - Programming/erasing: 100,000 times
	RAM	- Capacity: 512 Kbytes 0000 0000h to 0003 FFFFh (256 Kbytes): 240 MHz No-wait access 0004 0000h to 0007 FFFFh (256 Kbytes): No-wait access at up to 120 MHz, single wait access at frequencies above 120 MHz
	RAM with ECC	- Capacity: 32 Kbytes - Single wait access at up to 120 MHz, two wait accesses for reading and three wait accesses for writing at frequencies above 120 MHz - SEC-DED (single error correction/double error detection)
	Standby RAM	- Capacity: 8 Kbytes - Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access

Table 1.1 Outline of Specifications (10/10)

Classification	Module/Function	Description
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.

Note 2. Setting is only possible when the input sampling rate 44.1 kHz is selected.

Note 3. The product part number differs according to whether or not it supports encryption.

Note 4. The product part number differs according to whether or not it includes an SDHI (SD host interface).

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/8)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.22-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	XCOUT	Output	Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
	UB	Input	USB boot mode or user boot mode enable pin
	UPSEL	Input	Selects the power supply method in USB boot mode. The low level selects self-power mode and the high level selects bus power mode.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strobe signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU or GPT in the high impedance state

Table 1.4 Pin Functions (8/8)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins
	P10 to P17	I/O	8-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins (P35: input pin)
	P40 to P47	I/O	8-bit input/output pins
	P50 to P56	I/O	7-bit input/output pins (176-pin devices have only P50 to P53)
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P83, P86, P87	I/O	6-bit input/output pins
	P90 to P97	I/O	8-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF0 to PF5	I/O	6-bit input/output pins
	PG0 to PG7	I/O	8-bit input/output pins
	PJ3, PJ5	I/O	2-bit input/output pins

Note: Note the following regarding pin names. For details, see section 1.5, Pin Assignments.

- We recommend using pins that have a letter ("A", "B", etc.) to indicate group membership appended to their names as groups. For the RSPI, QSPI, SDHI, and MMC interfaces, the AC portion of the electrical characteristics is measured for each group.
- Pins that have "-DS" appended to their names can be used as triggers for release from deep software standby.
- IIC pin functions that have [FM+] appended to their names support fast-mode plus.

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCiG, SCiH, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
J14		PA7	A7	TIOCB2/PO23	MISOA-B/ ETO_WOL			
J15		PA6	A6	MTIC5V/MTCLKB/ GTETR-G-C/TIOCA2/ TMC13/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ETO_EXOUT			
K1		P33	EDREQ1	MTIOC0D/TIOC0D/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOU/RTICIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/ SSCL1			
K4	TCK	PF1			SCK1			
K12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
K13		P71	A18/CS1#		ET0_MDIO			
K14	VCC							
K15		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
L1		P31		MTIOC4D/TMC12/ PO9/RTIC1	CTS1#/RTS1#/ SS1#/ET1_MDC/ SSLB0-A		IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/ PO8/RTIC0/POE8#	RXD1/SMISO1/ SSCL1/ET1_MDIO/ MISOB-A		IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/ SSDA1			
L4		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ SSIDATA1	HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
L15		P72	A19/CS2#		ET0_MDC			
M1		P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/ET1_WOL/ RSPCKB-A			
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ ET1_EXOUT/ MOSIB-A			
M3		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
M4		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (7/7)

Pin Number								
176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
171		P41					IRQ9-DS	AN001
172	VREFL0							
173		P40					IRQ8-DS	AN000
174	VREFH0							
175	AVCC0							
176		P07					IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/4)

Pin Number				Timer	Communication	Memory Interface Camera Interface		
100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	(QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
C8		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
C9		PE5	D13[A13/ D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
C10		PE4	D12[A12/ D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
D1	XCIN							
D2	XCOUT							
D3	MD/FINED							
D4	VBATT							
D5		P45					IRQ13- DS	AN005
D6		P46					IRQ14- DS	AN006
D7		PE6	D14[A14/ D14]	TIOC6C/GTIOC3B-E/ TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
D8		PE7	D15[A15/ D15]	MTIOC6A/GTIOC3A- E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D9		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/GTIOC2A- C/TIOC0B/PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
E1	XTAL	P37						
E2	VSS							
E3	RES#							
E4	TRST#	P34		MTIOC0A/TMIC3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
E5		P41					IRQ9-DS	AN001
E6		PA2	A2	MTIOC7A/GTIOC1A- C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
E7		PA6	A6	MTIC5V/MTCLKB/ GTETR-G-C/TIOCA2/ TMIC3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
E8		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
E9		PA5	A5	MTIOC6B/TIOC0B1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
E10		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
F1	EXTAL	P36						
F2	VCC							
F3	UPSEL	P35					NMI	
F4		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOU/RTCIC2/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN		IRQ2-DS	

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (3/4)

Pin Number	Power Supply Clock System Contro	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SClg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
56		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
57		PB3	A11	MTIOC0A/MTIOC4A/ TIOC03/TCLKD/ TMO0/PO27/POE11#	SCK6/ET0_RX_ER/ RMII0_RX_ER			
58		PB2	A10	TIOCC3/TCLKC/ PO26	CTS6#/RTS6#SS6#/ ET0_RX_CLK/ REF50CK0			
59		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
60	VCC							
61		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
62	VSS							
63		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
64		PA6	A6	MTIC5V/MTCLKB/ GTETRIG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
65		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
66		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
67		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
68		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
69		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
70		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
71		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
72		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/ TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
75		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3	MMC_D7-B		AN101
76		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXD12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
77		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
78		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
79		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/ QMI-B	IRQ7	AN107

Table 4.1 List of I/O Registers (Address Order) (4 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 210Ch	DMAC4	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACa
0008 2110h	DMAC4	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACa
0008 2113h	DMAC4	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACa
0008 2114h	DMAC4	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACa
0008 211Ch	DMAC4	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACa
0008 211Dh	DMAC4	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACa
0008 211Eh	DMAC4	DMA Status Register	DMSTS	8	8	2 ICLK		DMACa
0008 211Fh	DMAC4	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACa
0008 2140h	DMAC5	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACa
0008 2144h	DMAC5	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACa
0008 2148h	DMAC5	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACa
0008 214Ch	DMAC5	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACa
0008 2150h	DMAC5	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACa
0008 2153h	DMAC5	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACa
0008 2154h	DMAC5	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACa
0008 215Ch	DMAC5	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACa
0008 215Dh	DMAC5	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACa
0008 215Eh	DMAC5	DMA Status Register	DMSTS	8	8	2 ICLK		DMACa
0008 215Fh	DMAC5	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACa
0008 2180h	DMAC6	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACa
0008 2184h	DMAC6	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACa
0008 2188h	DMAC6	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACa
0008 218Ch	DMAC6	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACa
0008 2190h	DMAC6	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACa
0008 2193h	DMAC6	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACa
0008 2194h	DMAC6	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACa
0008 219Ch	DMAC6	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACa
0008 219Dh	DMAC6	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACa
0008 219Eh	DMAC6	DMA Status Register	DMSTS	8	8	2 ICLK		DMACa
0008 219Fh	DMAC6	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACa
0008 21C0h	DMAC7	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACa
0008 21C4h	DMAC7	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACa
0008 21C8h	DMAC7	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACa
0008 21CCh	DMAC7	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACa
0008 21D0h	DMAC7	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACa
0008 21D3h	DMAC7	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACa
0008 21D4h	DMAC7	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACa
0008 21DCh	DMAC7	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACa
0008 21DDh	DMAC7	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACa
0008 21DEh	DMAC7	DMA Status Register	DMSTS	8	8	2 ICLK		DMACa
0008 21DFh	DMAC7	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACa
0008 2200h	DMAC	DMACA Module Activation Register	DMAST	8	8	2 ICLK		DMACa
0008 2204h	DMAC	DMAC74 Interrupt Status Monitor Register	DMIST	8	8	2 ICLK		DMACa
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK		DTCa
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK		DTCa
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK		DTCa
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK		DTCa
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK		DTCa
0008 2800h	EXDMA C0	EXDMA Source Address Register	EDMSAR	32	32	1, 2 BCLK		EXDMACa

Table 4.1 List of I/O Registers (Address Order) (7 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK		Buses
0008 3C00h	BSC	SDC Control Register	SDCCR	8	8	1, 2 BCLK		Buses
0008 3C01h	BSC	SDC Mode Register	SDCMOD	8	8	1, 2 BCLK		Buses
0008 3C02h	BSC	SDRAM Access Mode Register	SDAMOD	8	8	1, 2 BCLK		Buses
0008 3C10h	BSC	SDRAM Self-Refresh Control Register	SDSELF	8	8	1, 2 BCLK		Buses
0008 3C14h	BSC	SDRAM Refresh Control Register	SDRFCR	16	16	1, 2 BCLK		Buses
0008 3C16h	BSC	SDRAM Auto-Refresh Control Register	SDRFEN	8	8	1, 2 BCLK		Buses
0008 3C20h	BSC	SDRAM Initialization Sequence Control Register	SDICR	8	8	1, 2 BCLK		Buses
0008 3C24h	BSC	SDRAM Initialization Register	SDIR	16	16	1, 2 BCLK		Buses
0008 3C40h	BSC	SDRAM Address Register	SDADR	8	8	1, 2 BCLK		Buses
0008 3C44h	BSC	SDRAM Timing Register	SDTR	32	32	1, 2 BCLK		Buses
0008 3C48h	BSC	SDRAM Mode Register	SDMOD	16	16	1, 2 BCLK		Buses
0008 3C50h	BSC	SDRAM Status Register	SDSR	8	8	1, 2 BCLK		Buses
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK		MPU
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK		MPU
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK		MPU
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK		MPU
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK		MPU
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK		MPU
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK		MPU
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK		MPU
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK		MPU
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK		MPU
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK		MPU
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK		MPU
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK		MPU
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK		MPU
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK		MPU
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK		MPU
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK		MPU
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK		MPU
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK		MPU
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK		MPU
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK		MPU
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK		MPU
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK		MPU
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK		MPU
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK		MPU
0008 6610h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	32	32	1 ICLK		RAM
0008 7010h to 0008 70FFh	ICU	Interrupt Request Registers 016 to 255	IR016 to 255	8	8	2 ICLK		ICUA
0008 711Ah to 0008 71FFh	ICU	DTC Start Enable Registers 026 to 255	DTCE026 to DTCE255	8	8	2 ICLK		ICUA
0008 7202h to 0008 721Fh	ICU	Interrupt Request Enable Registers 02 to 1F	IER02 to IER1F	8	8	2 ICLK		ICUA
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8	2 ICLK		ICUA
0008 72E1h	ICU	Software Interrupt 2 Generation Register	SWINT2R	8	8	2 ICLK		ICUA
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK		ICUA
0008 7300h to 0008 73FFh	ICU	Interrupt Source Priority Registers 000 to 255	IPR000 to IPR255	8	8	2 ICLK		ICUA

Table 4.1 List of I/O Registers (Address Order) (42 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
000A 0400h	USB	Deep Standby USB Transceiver Control/Pin Monitoring Register	DPUSR0R	32	32	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*5}$	USBb
000A 0404h	USB	Deep Standby USB Suspend/Resume Interrupt Register	DPUSR1R	32	32	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*5}$	USBb
000A 0500h	PDC	PDC Control Register 0	PCCR0	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0504h	PDC	PDC Control Register 1	PCCR1	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0508h	PDC	PDC Status Register	PCSR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 050Ch	PDC	PDC Pin Monitor Register	PCMONR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0510h	PDC	PDC Receive Data Register	PCDR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0514h	PDC	Vertical Capture Register	VCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0518h	PDC	Horizontal Capture Register	HCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000C 0000h	EDMAC 0	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0008h	EDMAC 0	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0010h	EDMAC 0	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0018h	EDMAC 0	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0020h	EDMAC 0	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0028h	EDMAC 0	ETHERC/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0030h	EDMAC 0	ETHERC/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0038h	EDMAC 0	ETHERC/EDMAC Transmit/Receive Status Copy Enable Register	TRSCER	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0040h	EDMAC 0	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0048h	EDMAC 0	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0050h	EDMAC 0	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0058h	EDMAC 0	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0064h	EDMAC 0	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0068h	EDMAC 0	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 006Ch	EDMAC 0	Independent Output Signal Setting Register	IOSR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0070h	EDMAC 0	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0078h	EDMAC 0	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 007Ch	EDMAC 0	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00C8h	EDMAC 0	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00CCh	EDMAC 0	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00D4h	EDMAC 0	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00D8h	EDMAC 0	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0100h	ETHERC0	ETHERC Mode Register	ECMR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0108h	ETHERC0	Receive Frame Length Register	RFLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC

Table 4.1 List of I/O Registers (Address Order) (51 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 218Ah	GPT1	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 218Ch	GPT1	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 218Eh	GPT1	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2190h	GPT1	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2192h	GPT1	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2194h	GPT1	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2196h	GPT1	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2198h	GPT1	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 219Ah	GPT1	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 219Ch	GPT1	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 219Eh	GPT1	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21A0h	GPT1	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21A4h	GPT1	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21A8h	GPT1	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21B0h	GPT1	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2200h	GPT2	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2204h	GPT2	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2206h	GPT2	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2208h	GPT2	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 220Ch	GPT2	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 220Eh	GPT2	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2210h	GPT2	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2212h	GPT2	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2214h	GPT2	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2216h	GPT2	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2218h	GPT2	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 221Ch	GPT2	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 221Eh	GPT2	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2220h	GPT2	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2224h	GPT2	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa

Table 4.1 List of I/O Registers (Address Order) (54 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4328h	EPTPC	Timer Cycle Setting Register 2	TMCYCR2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 432Ch	EPTPC	Timer Pulse Width Setting Register 2	TMPLSR2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4330h	EPTPC	Timer Start Time Setting Register	TMSTTRU3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4334h	EPTPC	Timer Start Time Setting Register	TMSTTRL3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4338h	EPTPC	Timer Cycle Setting Register 3	TMCYCR3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 433Ch	EPTPC	Timer Pulse Width Setting Register 3	TMPLSR3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4340h	EPTPC	Timer Start Time Setting Register	TMSTTRU4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4344h	EPTPC	Timer Start Time Setting Register	TMSTTRL4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4348h	EPTPC	Timer Cycle Setting Register 4	TMCYCR4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 434Ch	EPTPC	Timer Pulse Width Setting Register 4	TMPLSR4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4350h	EPTPC	Timer Start Time Setting Register	TMSTTRU5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4354h	EPTPC	Timer Start Time Setting Register	TMSTTRL5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4358h	EPTPC	Timer Cycle Setting Register 5	TMCYCR5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 435Ch	EPTPC	Timer Pulse Width Setting Register 5	TMPLSR5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 437Ch	EPTPC	Timer Start Register	TMSTARTR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4400h	EPTPC	PRC-TC Status Register	PRSR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4404h	EPTPC	PRC-TC Status Notification Permission Register	PRIPR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4410h	EPTPC	Channel 0 Local MAC Address Register	PRMACRU0	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4414h	EPTPC	Channel 0 Local MAC Address Register	PRMACRL0	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4418h	EPTPC	Channel 1 Local MAC Address Register	PRMACRU1	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 441Ch	EPTPC	Channel 1 Local MAC Address Register	PRMACRL1	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4420h	EPTPC	Packet Transmission Control Register	TRNDISR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4430h	EPTPC	Relay Mode Register	TRNMR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4434h	EPTPC	Cut-Through Transfer Start Threshold Register	TRNCTTDR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4800h	EPTPC 0	SYNFP Status Register	YSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4804h	EPTPC 0	SYNFP Status Notification Permission Register	SYIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4810h	EPTPC 0	SYNFP MAC Address Register	SYMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4814h	EPTPC 0	SYNFP MAC Address Register	SYMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4818h	EPTPC 0	SYNFP LLC-CTL Value Register	SYLLCCTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 481Ch	EPTPC 0	SYNFP Local IP Address Register	SYIPADDRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4840h	EPTPC 0	SYNFP Specification Version Setting Register	SYSPVRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4844h	EPTPC 0	SYNFP Domain Number Setting Register	SYDOMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4850h	EPTPC 0	Announce Message Flag Field Setting Register	ANFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4854h	EPTPC 0	Sync Message Flag Field Setting Register	SYNFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4858h	EPTPC 0	Delay_Req Message Flag Field Setting Register	DYRQFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 485Ch	EPTPC 0	Delay_Resp Message Flag Field Setting Register	DYRPFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4860h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4864h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4868h	EPTPC 0	SYNFP Local Port Number Register	SYPNUMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4880h	EPTPC 0	SYNFP Register Value Load Directive Register	SYRVLDR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa

5.3 AC Characteristics

Table 5.7 Operating Frequency (High-Speed Operating Mode)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	240	MHz
	Peripheral module clock (PCLKA)			—	—	120	
	Peripheral module clock (PCLKB)			—	—	60	
	Peripheral module clock (PCLKC)			—	—	60	
	Peripheral module clock (PCLKD)			—	—	60	
	Flash-IF clock (FCLK)			—*1	—	60	
	External bus clock (BCLK)	Packages with 177 to 144 pins only		—	—	120	
		Package with 100 pins only		—	—	60	
	BCLK pin output	Packages with 177 to 144 pins only		—	—	60	
		Package with 100 pins only		—	—	30	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	60	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	60	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

Table 5.8 Operating Frequency (Low-Speed Operating Mode 1)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	1	MHz
	Peripheral module clock (PCLKA)			—	—	1	
	Peripheral module clock (PCLKB)			—	—	1	
	Peripheral module clock (PCLKC)*1			—	—	1	
	Peripheral module clock (PCLKD)*1			—	—	1	
	Flash-IF clock (FCLK)			—	—	1	
	External bus clock (BCLK)	Packages with 177 to 144 pins only		—	—	1	
		Package with 100 pins only		—	—	1	
	BCLK pin output	Packages with 177 to 144 pins only		—	—	1	
		Package with 100 pins only		—	—	1	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	1	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	1	

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

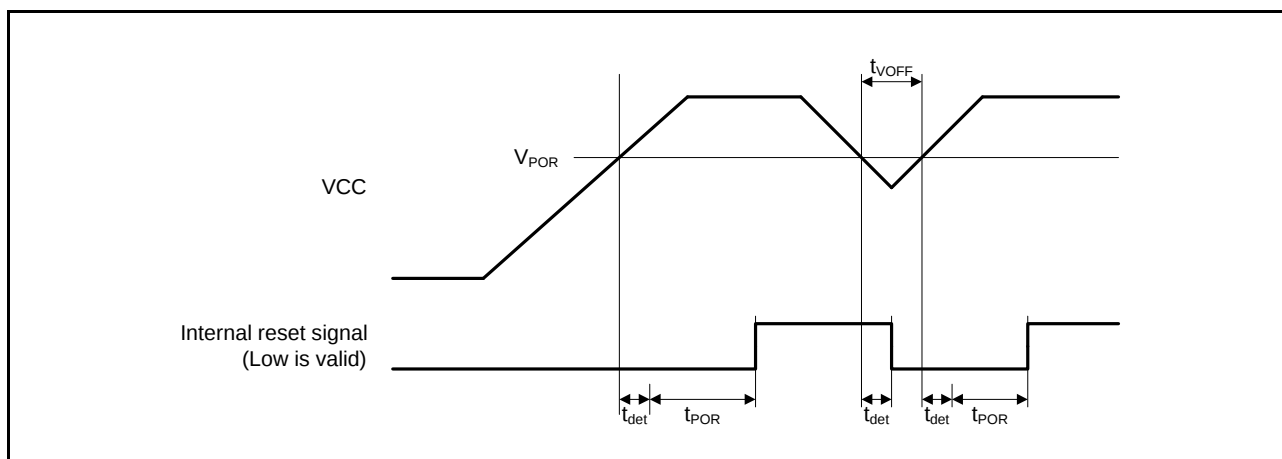


Figure 5.83 Power-on Reset Timing

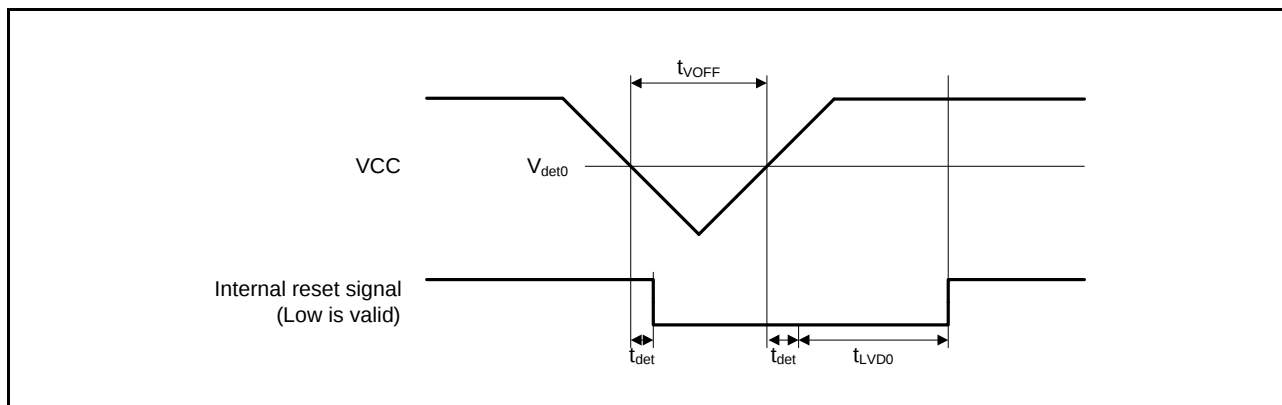


Figure 5.84 Voltage Detection Circuit Timing (V_{det0})

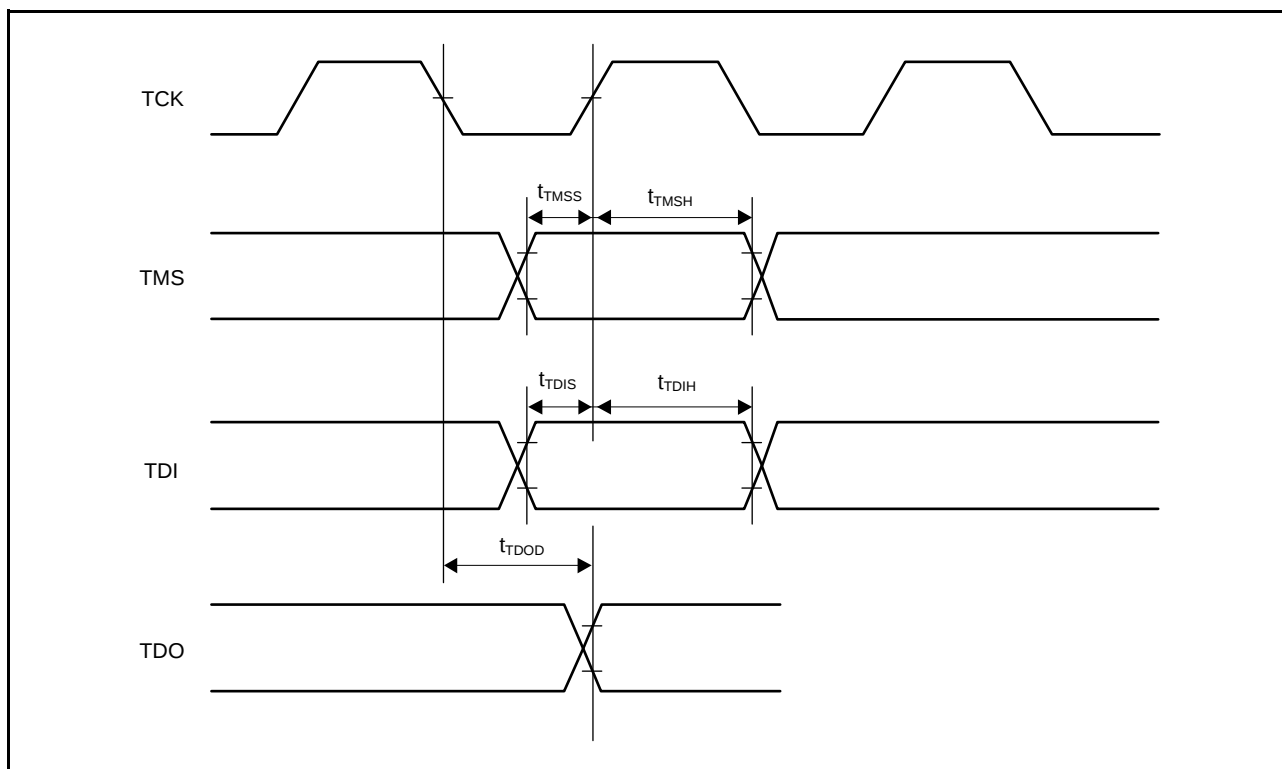


Figure 5.92 Boundary Scan Input/Output Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

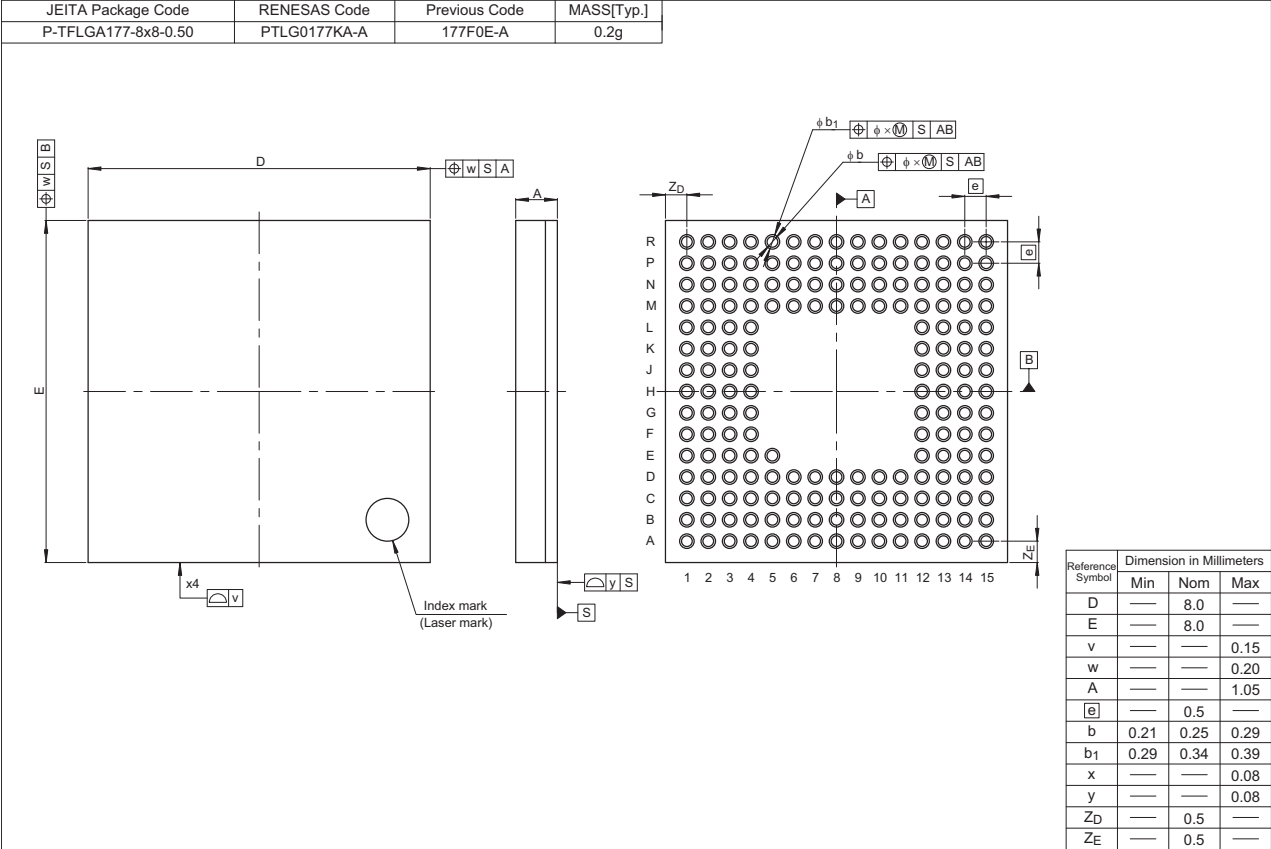


Figure A 177-Pin TFLGA (PTLG0177KA-A)

REVISION HISTORY	RX71M Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jan 15, 2015	—	First edition, issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.