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**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

**Applications of "Embedded - Microcontrollers"**

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RXv2 |
| Core Size | 32-Bit Single-Core |
| Speed | 240MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 127 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x12b, 21x12b; D/A 2x12 |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LFBGA |
| Supplier Device Package | 176-LFBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mfhdbg-20 |

## 1.4      Pin Functions

Table 1.4 lists the pin functions.

**Table 1.4          Pin Functions (1/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Digital power supply | VCC | Input | Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VCL | Input | Connect this pin to VSS via a 0.22-µF capacitor. The capacitor should be placed close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | VBATT | Input | Backup power pin |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| | SDCLK | Output | Outputs the SDRAM-dedicated clock. |
| | XCOUT | Output | Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCIN | Input | |
| Clock frequency accuracy measurement | CACREF | Input | Reference clock input pin for the clock frequency accuracy measurement circuit |
| Operating mode control | MD | Input | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation. |
| | UB | Input | USB boot mode or user boot mode enable pin |
| | UPSEL | Input | Selects the power supply method in USB boot mode. The low level selects self-power mode and the high level selects bus power mode. |
| System control | RES# | Input | Reset signal input pin. This LSI enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| | BSCANP | Input | Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low. |
| On-chip emulator | FINED | I/O | Fine interface pin |
| | TRST# | Input | On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. |
| | TRSYNC | Output | This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. |
| | TRDATA0 to TRDATA3 | Output | These pins output the trace information. |
| Address bus | A0 to A23 | Output | Output pins for the address |
| Data bus | D0 to D31 | I/O | Input and output pins for the bidirectional data bus |
| Multiplexed bus | A0/D0 to A15/D15 | I/O | Address/data multiplexed bus |

**Table 1.4        Pin Functions (2/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Bus control | RD# | Output | Strobe signal which indicates that reading from the external bus interface space is in progress |
| | WR# | Output | Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode |
| | WR0# to WR3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode |
| | BC0# to BC3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode |
| | ALE | Output | Address latch signal when address/data multiplexed bus is selected |
| | WAIT# | Input | Input pin for wait request signals in access to the external space |
| | CS0# to CS7# | Output | Select signals for CS areas |
| | CKE | Output | SDRAM clock enable signal |
| | SDCS# | Output | SDRAM chip select signal |
| | RAS# | Output | SDRAM row address strobe signal |
| | CAS# | Output | SDRAM column address strove signal |
| | WE# | Output | SDRAM write enable pin |
| | DQM0 to DQM3 | Output | SDRAM I/O data mask enable signals |
| EXDMA controller | EDREQ0, EDREQ1 | Input | External DMA transfer request pins |
| | EDACK0, EDACK1 | Output | Single address transfer acknowledge signals |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ15 | Input | Maskable interrupt request pins |
| Multi-function timer pulse unit 3 | MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins |
| | MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins |
| | MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins |
| | MTIC5U, MTIC5V MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins |
| | MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D | I/O | The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins |
| | MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D | I/O | The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins |
| | MTIOC8A, MTIOC8B MTIOC8C, MTIOC8D | I/O | The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins |
| | MTCLKA, MTCLKB MTCLKC, MTCLKD | Input | Input pins for external clock signals or for phase counting mode clock signals |
| Port output enable 3 | POE0#, POE4#, POE8#, POE10#, POE11# | Input | Input pins for request signals to place the MTU or GPT in the high impedance state |

**Table 1.5        List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (7/7)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| R8 | | P11 | | MTIC5V/TMCI3 | SCK2/ USBA_VBUS/ USBA_VBUSEN | | IRQ1 | |
| R9 | | P53*2 | BCLK | | | | | |
| R10 | VSS | | | | | | | |
| R11 | VCC | | | | | | | |
| R12 | | P80 | EDREQ0 | MTIOC3B/PO26 | SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN | MMC_D2-A/ SDHI_WP-A/ QIO2-A | | |
| R13 | | P76 | CS6# | PO22 | RXD11/ET0_RX_CLK/ REF50CK0 | MMC_CMD-A/ SDHI_CMD-A/ QSSL-A | | |
| R14 | | P74 | A20/CS4# | PO19 | CTS11#/ET0_ERXD1/ RMII0_RXD1 | | | |
| R15 | | PC1 | A17 | MTIOC3A/TCLKD/ PO18 | SCK5/SSLA2-A/ ET0_ERXD2 | | IRQ12 | |

Note 1.   The 176-pin LFBGA does not include the E5 pin.
Note 2.   The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

**Table 1.7    List of Pin and Pin Functions (145-Pin TFLGA) (1/5)**

| Pin Number<br>145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication<br>(ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface<br>(QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| A1 | AVSS0 | | | | | | | |
| A2 | | P07 | | | | | IRQ15 | ADTRG0# |
| A3 | | P40 | | | | | IRQ8-DS | AN000 |
| A4 | | P42 | | | | | IRQ10-DS | AN002 |
| A5 | | P45 | | | | | IRQ13-DS | AN005 |
| A6 | | P90 | A16 | | TXD7/SMOSI7/SSDA7 | | | AN114 |
| A7 | | P92 | A18 | POE4# | RXD7/SMISO7/SSCL7 | | | AN116 |
| A8 | | PD2 | D2[A2/D2] | MTIOC4D/ GTIOC0B-E/TIC2 | CRX0 | MMC_D2-B/ SDHI_D2-B/ QIO2-B | IRQ2 | AN110 |
| A9 | | PD6 | D6[A6/D6] | MTIC5V/MTIOC8A/ POE4# | | MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B | IRQ6 | AN106 |
| A10 | VSS | | | | | | | |
| A11 | | P62 | CS2#/RAS# | | | | | |
| A12 | | PE1 | D9[A9/D9] | MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | | ANEX1 |
| A13 | | PE3 | D11[A11/D11] | MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3 | CTS12#/RTS12#/ SS12#/ET0_ERXD3/ | MMC_D7-B | | AN101 |
| B1 | AVCC1 | | | | | | | |
| B2 | AVCC0 | | | | | | | |
| B3 | | P05 | | | | | IRQ13 | DA1 |
| B4 | VREFL0 | | | | | | | |
| B5 | | P43 | | | | | IRQ11-DS | AN003 |
| B6 | | P47 | | | | | IRQ15-DS | AN007 |
| B7 | | P91 | A17 | | SCK7 | | | AN115 |
| B8 | | PD0 | D0[A0/D0] | GTIOC1B-E/POE4# | | | IRQ0 | AN108 |
| B9 | | PD4 | D4[A4/D4] | MTIOC8B/POE11# | | MMC_CMD-B/ SDHI_CMD-B/ QSSL-B | IRQ4 | AN112 |
| B10 | VCC | | | | | | | |
| B11 | | P61 | CS1#/SDCS# | | | | | |
| B12 | | PE2 | D10[A10/D10] | MTIOC4A/ GTIOC0B-A/PO23/ TIC3 | RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B | MMC_D6-B | IRQ7-DS | AN100 |
| B13 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28 | ET0_ERXD2/SSLB0-B | | | AN102 |
| C1 | AVSS1 | | | | | | | |
| C2 | | P02 | | TMCI1 | SCK6 | | IRQ10 | AN120 |
| C3 | VREFH0 | | | | | | | |
| C4 | | P41 | | | | | IRQ9-DS | AN001 |
| C5 | | P46 | | | | | IRQ14-DS | AN006 |
| C6 | VSS | | | | | | | |
| C7 | | PD1 | D1[A1/D1] | MTIOC4B/ GTIOC1A-E/POE0# | CTX0 | | IRQ1 | AN109 |
| C8 | | PD3 | D3[A3/D3] | MTIOC8D/ GTIOC0A-E/POE8#/ TOC2 | | MMC_D3-B/ SDHI_D3-B/ QIO3-B | IRQ3 | AN111 |

**Table 1.7    List of Pin and Pin Functions (145-Pin TFLGA) (3/5)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| F13 | | PA2 | A2 | MTIOC7A/ GTIOC1A-C/PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | | |
| G1 | XTAL | P37 | | | | | | |
| G2 | RES | | | | | | | |
| G3 | MD/FINED | | | | | | | |
| G4 | BSCANP | | | | | | | |
| G10 | | PA5 | A5 | MTIOC6B/TIOCB1/ GTIOC0A-C/PO21 | RSPCKA-B/ ET0_LINKSTA | | | |
| G11 | | PA6 | A6 | MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10# | CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT | | | |
| G12 | VCC | | | | | | | |
| G13 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC | | IRQ5-DS | |
| H1 | EXTAL | P36 | | | | | | |
| H2 | VCC | | | | | | | |
| H3 | VSS | | | | | | | |
| H4 | UPSEL | P35 | | | | | NMI | |
| H10 | | P72 | A19/CS2# | | ET0_MDC | | | |
| H11 | | P71 | A18/CS1# | | ET0_MDIO | | | |
| H12 | | PB0 | A8 | MTIC5W/TIOCA3/ PO24 | RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1 | | IRQ12 | |
| H13 | | PA7 | A7 | TIOCB2/PO23 | MISOA-B/ET0_WOL | | | |
| J1 | TRST# | P34 | | MTIOC0A/TMCI3/ PO12/POE10# | SCK6/SCK0/ ET0_LINKSTA | | IRQ4 | |
| J2 | | P33 | EDREQ1 | MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11# | RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0 | PCKO | IRQ3-DS | |
| J3 | | P32 | | MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10# | TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN | VSYNC | IRQ2-DS | |
| J4 | TDI | P30 | | MTIOC4B/TMRI3/ PO8/RTCIC0/POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | IRQ0-DS | |
| J10 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11# | SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER | | | |
| J11 | | PB4 | A12 | TIOCA4/PO28 | CTS9#/ET0_TX_EN/ RMII0_TXD_EN | | | |
| J12 | | PB2 | A10 | TIOCC3/TCLKC/ PO26 | CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0 | | | |
| J13 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0 | | IRQ4-DS | |
| K1 | TCK | P27 | CS7# | MTIOC2B/TMCI3/PO7 | SCK1/RSPCKB-A | | | |
| K2 | TDO | P26 | CS6# | MTIOC2A/TMO1/PO6 | TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A | | | |
| K3 | TMS | P31 | | MTIOC4D/TMCI2/ PO9/RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0-A | | IRQ1-DS | |

**Table 1.8    List of Pin and Pin Functions (144-Pin LQFP) (5/5)**

| Pin Number 144-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 116 | VSS | | | | | | | |
| 117 | | P60 | CS0# | | | | | |
| 118 | VCC | | | | | | | |
| 119 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B | IRQ7 | AN107 |
| 120 | | PD6 | D6[A6/D6] | MTIC5V/MTIOC8A/ POE4# | | MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO-B | IRQ6 | AN106 |
| 121 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/ POE10# | | MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B | IRQ5 | AN113 |
| 122 | | PD4 | D4[A4/D4] | MTIOC8B/POE11# | | MMC_CMD-B/ SDHI_CMD-B/ QSSL-B | IRQ4 | AN112 |
| 123 | | PD3 | D3[A3/D3] | MTIOC8D/ GTIOC0A-E/POE8#/ TOC2 | | MMC_D3-B/ SDHI_D3-B/ QIO3-B | IRQ3 | AN111 |
| 124 | | PD2 | D2[A2/D2] | MTIOC4D/ GTIOC0B-E/TIC2 | CRX0 | MMC_D2-B/ SDHI_D2-B/ QIO2-B | IRQ2 | AN110 |
| 125 | | PD1 | D1[A1/D1] | MTIOC4B/ GTIOC1A-E/POE0# | CTX0 | | IRQ1 | AN109 |
| 126 | | PD0 | D0[A0/D0] | GTIOC1B-E/POE4# | | | IRQ0 | AN108 |
| 127 | | P93 | A19 | POE0# | CTS7#/RTS7#/SS7# | | | AN117 |
| 128 | | P92 | A18 | POE4# | RXD7/SMISO7/SSCL7 | | | AN116 |
| 129 | | P91 | A17 | | SCK7 | | | AN115 |
| 130 | VSS | | | | | | | |
| 131 | | P90 | A16 | | TXD7/SMOSI7/SSDA7 | | | AN114 |
| 132 | VCC | | | | | | | |
| 133 | | P47 | | | | | IRQ15-DS | AN007 |
| 134 | | P46 | | | | | IRQ14-DS | AN006 |
| 135 | | P45 | | | | | IRQ13-DS | AN005 |
| 136 | | P44 | | | | | IRQ12-DS | AN004 |
| 137 | | P43 | | | | | IRQ11-DS | AN003 |
| 138 | | P42 | | | | | IRQ10-DS | AN002 |
| 139 | | P41 | | | | | IRQ9-DS | AN001 |
| 140 | VREFL0 | | | | | | | |
| 141 | | P40 | | | | | IRQ8-DS | AN000 |
| 142 | VREFH0 | | | | | | | |
| 143 | AVCC0 | | | | | | | |
| 144 | | P07 | | | | | IRQ15 | ADTRG0# |

**Table 4.1      List of I/O Registers (Address Order) (6 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK | Number of Access Cycles ICLK < PCLK | Related Function |
|---|---|---|---|---|---|---|---|---|
| 0008 2BE8h | EXDMAC | Cluster Buffer Register 2 | CLSBR2 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BECh | EXDMAC | Cluster Buffer Register 3 | CLSBR3 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF0h | EXDMAC | Cluster Buffer Register 4 | CLSBR4 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF4h | EXDMAC | Cluster Buffer Register 5 | CLSBR5 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF8h | EXDMAC | Cluster Buffer Register 6 | CLSBR6 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BFCh | EXDMAC | Cluster Buffer Register 7 | CLSBR7 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 3002h | BSC | CS0 Mode Register | CS0MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3004h | BSC | CS0 Wait Control Register 1 | CS0WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3008h | BSC | CS0 Wait Control Register 2 | CS0WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3012h | BSC | CS1 Mode Register | CS1MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3014h | BSC | CS1 Wait Control Register 1 | CS1WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3018h | BSC | CS1 Wait Control Register 2 | CS1WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3022h | BSC | CS2 Mode Register | CS2MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3024h | BSC | CS2 Wait Control Register 1 | CS2WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3028h | BSC | CS2 Wait Control Register 2 | CS2WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3032h | BSC | CS3 Mode Register | CS3MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3034h | BSC | CS3 Wait Control Register 1 | CS3WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3038h | BSC | CS3 Wait Control Register 2 | CS3WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3042h | BSC | CS4 Mode Register | CS4MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3044h | BSC | CS4 Wait Control Register 1 | CS4WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3048h | BSC | CS4 Wait Control Register 2 | CS4WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3052h | BSC | CS5 Mode Register | CS5MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3054h | BSC | CS5 Wait Control Register 1 | CS5WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3058h | BSC | CS5 Wait Control Register 2 | CS5WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3062h | BSC | CS6 Mode Register | CS6MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3064h | BSC | CS6 Wait Control Register 1 | CS6WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3068h | BSC | CS6 Wait Control Register 2 | CS6WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3072h | BSC | CS7 Mode Register | CS7MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3074h | BSC | CS7 Wait Control Register 1 | CS7WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3078h | BSC | CS7 Wait Control Register 2 | CS7WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3802h | BSC | CS0 Control Register | CS0CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 380Ah | BSC | CS0 Recovery Cycle Register | CS0REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3812h | BSC | CS1 Control Register | CS1CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 381Ah | BSC | CS1 Recovery Cycle Register | CS1REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3822h | BSC | CS2 Control Register | CS2CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 382Ah | BSC | CS2 Recovery Cycle Register | CS2REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3832h | BSC | CS3 Control Register | CS3CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 383Ah | BSC | CS3 Recovery Cycle Register | CS3REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3842h | BSC | CS4 Control Register | CS4CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 384Ah | BSC | CS4 Recovery Cycle Register | CS4REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3852h | BSC | CS5 Control Register | CS5CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 385Ah | BSC | CS5 Recovery Cycle Register | CS5REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3862h | BSC | CS6 Control Register | CS6CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 386Ah | BSC | CS6 Recovery Cycle Register | CS6REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3872h | BSC | CS7 Control Register | CS7CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 387Ah | BSC | CS7 Recovery Cycle Register | CS7REC | 16 | 16 | 1, 2 BCLK | | Buses |

**Table 4.1      List of I/O Registers (Address Order) (20 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK $\geq$ PCLK | ICLK $<$ PCLK | |
| 0008 9E24h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 2 | SPBMUL2 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E28h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 3 | SPBMUL3 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 A000h | SCI0 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A001h | SCI0 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A002h | SCI0 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A003h | SCI0 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A004h | SCI0 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A005h | SCI0 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A006h | SCI0 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A007h | SCI0 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A008h | SCI0 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A009h | SCI0 | I2C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Ah | SCI0 | I2C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Bh | SCI0 | I2C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Ch | SCI0 | I2C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Dh | SCI0 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Eh | SCI0 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Fh | SCI0 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Eh | SCI0 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A010h | SCI0 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A011h | SCI0 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A010h | SCI0 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A012h | SCI0 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A020h | SCI1 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A021h | SCI1 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A022h | SCI1 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A023h | SCI1 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A024h | SCI1 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A025h | SCI1 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A026h | SCI1 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A027h | SCI1 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |

**Table 4.1    List of I/O Registers (Address Order) (21 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK | Number of Access Cycles ICLK < PCLK | Related Function |
|---|---|---|---|---|---|---|---|---|
| 0008 A028h | SCI1 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A029h | SCI1 | I²C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A02Ah | SCI1 | I²C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A02Bh | SCI1 | I²C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A02Ch | SCI1 | I²C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A02Dh | SCI1 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A02Eh | SCI1 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A02Fh | SCI1 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A02Eh | SCI1 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A030h | SCI1 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A031h | SCI1 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A030h | SCI1 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A032h | SCI1 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A040h | SCI2 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A041h | SCI2 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A042h | SCI2 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A043h | SCI2 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A044h | SCI2 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A045h | SCI2 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A046h | SCI2 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A047h | SCI2 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A048h | SCI2 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A049h | SCI2 | I²C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A04Ah | SCI2 | I²C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A04Bh | SCI2 | I²C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A04Ch | SCI2 | I²C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A04Dh | SCI2 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A04Eh | SCI2 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A04Fh | SCI2 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A04Eh | SCI2 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A050h | SCI2 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |

**Table 4.1    List of I/O Registers (Address Order) (29 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---------|---------------|---------------|-----------------|----------------|-------------|-------------------------|----------------|------------------|
| | | | | | | ICLK $\geq$ PCLK | ICLK $<$ PCLK | |
| 0008 C02Fh | PORTF | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C030h | PORTG | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C032h | PORTJ | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C040h | PORT0 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C041h | PORT1 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C042h | PORT2 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C043h | PORT3 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C044h | PORT4 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C045h | PORT5 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C046h | PORT6 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C047h | PORT7 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C048h | PORT8 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C049h | PORT9 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Ah | PORTA | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Bh | PORTB | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Ch | PORTC | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Dh | PORTD | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Eh | PORTE | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Fh | PORTF | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C050h | PORTG | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C052h | PORTJ | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C060h | PORT0 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C061h | PORT1 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C062h | PORT2 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C063h | PORT3 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C064h | PORT4 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C065h | PORT5 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C066h | PORT6 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C067h | PORT7 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C068h | PORT8 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C069h | PORT9 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Ah | PORTA | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Bh | PORTB | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Ch | PORTC | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Dh | PORTD | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Eh | PORTE | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Fh | PORTF | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C070h | PORTG | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C072h | PORTJ | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C080h | PORT0 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C081h | PORT0 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C082h | PORT1 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C083h | PORT1 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C084h | PORT2 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C085h | PORT2 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C086h | PORT3 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C087h | PORT3 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C088h | PORT4 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C089h | PORT4 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Ah | PORT5 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |

**Table 4.1　List of I/O Registers (Address Order) (34 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---------|---------------|---------------|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C288h | SYSTEM | Deep Standby Interrupt Flag Register 2 | DPSIFR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C289h | SYSTEM | Deep Standby Interrupt Flag Register 3 | DPSIFR3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Ah | SYSTEM | Deep Standby Interrupt Edge Register 0 | DPSIEGR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Bh | SYSTEM | Deep Standby Interrupt Edge Register 1 | DPSIEGR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Ch | SYSTEM | Deep Standby Interrupt Edge Register 2 | DPSIEGR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Dh | SYSTEM | Deep Standby Interrupt Edge Register 3 | DPSIEGR3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C290h | SYSTEM | Reset Status Register 0 | RSTSR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Resets |
| 0008 C291h | SYSTEM | Reset Status Register 1 | RSTSR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Resets |
| 0008 C293h | SYSTEM | Main Clock Oscillator Forced Oscillation Control Register | MOFCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Clock Generation Circuit |
| 0008 C294h | SYSTEM | High-Speed On-Chip Oscillator Power Supply Control Register | HOCOPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Clock Generation Circuit |
| 0008 C297h | SYSTEM | Voltage Monitoring Circuit Control Register | LVCMPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LDVA |
| 0008 C298h | SYSTEM | Voltage Detection Level Select Register | LVDLVLR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LDVA |
| 0008 C29Ah | SYSTEM | Voltage Monitoring 1 Circuit Control Register 0 | LVD1CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LDVA |
| 0008 C29Bh | SYSTEM | Voltage Monitoring 2 Circuit Control Register 0 | LVD2CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LDVA |
| 0008 C2A0h to 0008 C2BFh | SYSTEM | Deep Standby Backup Registers 0 to 31 | DPSBKR0 to 31 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C400h | RTC | 64-Hz Counter | R64CNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C402h | RTC | Second Counter | RSECCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C402h | RTC | Binary Counter 0 | BCNT0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C404h | RTC | Minute Counter | RMINCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C404h | RTC | Binary Counter 1 | BCNT1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C406h | RTC | Hour Counter | RHRCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C406h | RTC | Binary Counter 2 | BCNT2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C408h | RTC | Day-of-Week Counter | RWKCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C408h | RTC | Binary Counter 3 | BCNT3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C40Ah | RTC | Date Counter | RDAYCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C40Ch | RTC | Month Counter | RMONCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C40Eh | RTC | Year Counter | RYRCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C410h | RTC | Second Alarm Register | RSECAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C410h | RTC | Binary Counter 0 Alarm Register | BCNT0AR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C412h | RTC | Minute Alarm Register | RMINAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C412h | RTC | Binary Counter 1 Alarm Register | BCNT1AR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C414h | RTC | Hour Alarm Register | RHRAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |

**Table 4.1        List of I/O Registers (Address Order) (38 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0009 284Ah | CAN2 | Transmit FIFO Control Register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 284Bh | CAN2 | Transmit FIFO Pointer Control Register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 284Ch | CAN2 | Error Interrupt Enable Register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 284Dh | CAN2 | Error Interrupt Factor Judge Register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 284Eh | CAN2 | Receive Error Count Register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 284Fh | CAN2 | Transmit Error Count Register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2850h | CAN2 | Error Code Store Register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2851h | CAN2 | Channel Search Support Register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2852h | CAN2 | Mailbox Search Status Register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2853h | CAN2 | Mailbox Search Mode Register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2854h | CAN2 | Time Stamp Register | TSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2856h | CAN2 | Acceptance Filter Support Register | AFSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2858h | CAN2 | Test Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 4200h | CMTW0 | Timer Start Register | CMWSTR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4204h | CMTW0 | Timer Control Register | CMWCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4208h | CMTW0 | Timer I/O Control Register | CMWIOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4210h | CMTW0 | Timer Counter | CMWCNT | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4214h | CMTW0 | Compare Match Constant Register | CMWCOR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4218h | CMTW0 | Input Capture Register 0 | CMWICR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 421Ch | CMTW0 | Input Capture Register 1 | CMWICR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4220h | CMTW0 | Output Compare Register 0 | CMWOCR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4224h | CMTW0 | Output Compare Register 1 | CMWOCR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4280h | CMTW1 | Timer Start Register | CMWSTR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4284h | CMTW1 | Timer Control Register | CMWCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4288h | CMTW1 | Timer I/O Control Register | CMWIOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4290h | CMTW1 | Timer Counter | CMWCNT | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4294h | CMTW1 | Compare Match Constant Register | CMWCOR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4298h | CMTW1 | Input Capture Register 0 | CMWICR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 429Ch | CMTW1 | Input Capture Register 1 | CMWICR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 42A0h | CMTW1 | Output Compare Register 0 | CMWOCR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 42A4h | CMTW1 | Output Compare Register 1 | CMWOCR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 8000h to 0009 D6BFh | SRC | Filter Coefficient Table | SRCFCTR0 to 5551 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFF0h | SRC | Input Data Register | SRCID | 32 | 32 | 5, 6 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFF4h | SRC | Output Data Register | SRCOD | 32 | 32 | 5, 6 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFF8h | SRC | Input Data Control Register | SRCIDCTRL | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFFAh | SRC | Output Data Control Register | SRCODCTRL | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFFCh | SRC | Control Register | SRCCTRL | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFFEh | SRC | Status Register | SRCSTAT | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 000A 0000h | USB0 | System Configuration Control Register | SYSCFG | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0004h | USB0 | System Configuration Status Register 0 | SYSSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9 × (frequency ratio of ICLK/PCLKB)[5] | USBb |
| 000A 0008h | USB0 | Device State Control Register 0 | DVSTCTR0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9 × (frequency ratio of ICLK/PCLKB)[5] | USBb |
| 000A 0014h | USB0 | CFIFO Port Register | CFIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0018h | USB0 | D0FIFO Port Register | D0FIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |

**Table 4.1      List of I/O Registers (Address Order) (42 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK | Number of Access Cycles ICLK < PCLK | Related Function |
|---|---|---|---|---|---|---|---|---|
| 000A 0400h | USB | Deep Standby USB Transceiver Control/Pin Monitoring Register | DPUSR0R | 32 | 32 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0404h | USB | Deep Standby USB Suspend/Resume Interrupt Register | DPUSR1R | 32 | 32 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0500h | PDC | PDC Control Register 0 | PCCR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0504h | PDC | PDC Control Register 1 | PCCR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0508h | PDC | PDC Status Register | PCSR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 050Ch | PDC | PDC Pin Monitor Register | PCMONR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0510h | PDC | PDC Receive Data Register | PCDR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0514h | PDC | Vertical Capture Register | VCR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0518h | PDC | Horizontal Capture Register | HCR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000C 0000h | EDMAC0 | EDMAC Mode Register | EDMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0008h | EDMAC0 | EDMAC Transmit Request Register | EDTRR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0010h | EDMAC0 | EDMAC Receive Request Register | EDRRR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0018h | EDMAC0 | Transmit Descriptor List Start Address Register | TDLAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0020h | EDMAC0 | Receive Descriptor List Start Address Register | RDLAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0028h | EDMAC0 | ETHERC/EDMAC Status Register | EESR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0030h | EDMAC0 | ETHERC/EDMAC Status Interrupt Enable Register | EESIPR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0038h | EDMAC0 | ETHERC/EDMAC Transmit/Receive Status Copy Enable Register | TRSCER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0040h | EDMAC0 | Missed-Frame Counter Register | RMFCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0048h | EDMAC0 | Transmit FIFO Threshold Register | TFTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0050h | EDMAC0 | FIFO Depth Register | FDR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0058h | EDMAC0 | Receive Method Control Register | RMCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0064h | EDMAC0 | Transmit FIFO Underflow Counter | TFUCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0068h | EDMAC0 | Receive FIFO Overflow Counter | RFOCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 006Ch | EDMAC0 | Independent Output Signal Setting Register | IOSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0070h | EDMAC0 | Flow Control Start FIFO Threshold Setting Register | FCFTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0078h | EDMAC0 | Receive Data Padding Insert Register | RPADIR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 007Ch | EDMAC0 | Transmit Interrupt Setting Register | TRIMD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 00C8h | EDMAC0 | Receive Buffer Write Address Register | RBWAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 00CCh | EDMAC0 | Receive Descriptor Fetch Address Register | RDFAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 00D4h | EDMAC0 | Transmit Buffer Read Address Register | TBRAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 00D8h | EDMAC0 | Transmit Descriptor Fetch Address Register | TDFAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0100h | ETHERC0 | ETHERC Mode Register | ECMR | 32 | 32 | 13, 14 PCLKA | 2 to 7 ICLK | ETHERC |
| 000C 0108h | ETHERC0 | Receive Frame Length Register | RFLR | 32 | 32 | 13, 14 PCLKA | 2 to 7 ICLK | ETHERC |

**Table 4.1    List of I/O Registers (Address Order) (63 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK $\geq$ PCLK | ICLK $<$ PCLK | |
| 000D 0456h | USBA | USB Request Value Register | USBVAL | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 0458h | USBA | USB Request Index Register | USBINDX | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 045Ah | USBA | USB Request Length Register | USBLENG | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 045Ch | USBA | DCP Configuration Register | DCPCFG | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 045Eh | USBA | DCP Maximum Packet Size Register | DCPMAXP | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 0460h | USBA | DCP Control Register | DCPCTR | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 0464h | USBA | Pipe Window Select Register | PIPESEL | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 0468h | USBA | Pipe Configuration Register | PIPECFG | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 046Ah | USBA | Pipe Buffer Register | PIPEBUF | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 046Ch | USBA | Pipe Maximum Packet Size Register | PIPEMAXP | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |
| 000D 046Eh | USBA | Pipe Cycle Control Register | PIPEPERI | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)[*5] | USBAa |

**Table 5.14    LOCO and IWDT-Dedicated Low-Speed Clock Timing**

Conditions:   VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
          VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
          VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
          $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| LOCO clock cycle time | $t_{Lcyc}$ | 3.78 | 4.16 | 4.63 | µs | |
| LOCO clock oscillation frequency | $f_{LOCO}$ | 216 | 240 | 264 | kHz | |
| LOCO clock oscillation stabilization wait time | $t_{LOCOWT}$ | — | — | 44 | µs | Figure 5.6 |
| IWDT-dedicated low-speed clock cycle time | $t_{ILcyc}$ | 7.57 | 8.33 | 9.26 | µs | |
| IWDT-dedicated low-speed clock oscillation frequency | $f_{ILOCO}$ | 108 | 120 | 132 | kHz | |
| IWDT-dedicated low-speed clock oscillation stabilization wait time | $t_{ILOCOWT}$ | — | 142 | 190 | µs | Figure 5.7 |
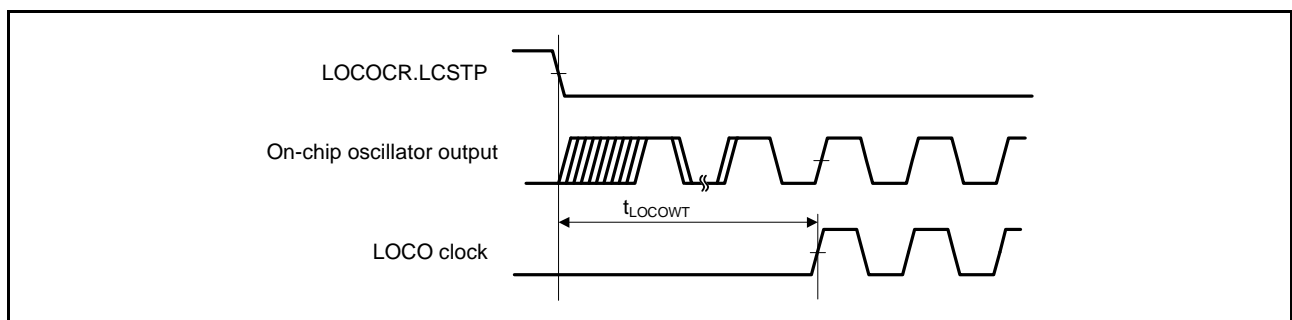


**Figure 5.6        LOCO Clock Oscillation Start Timing**
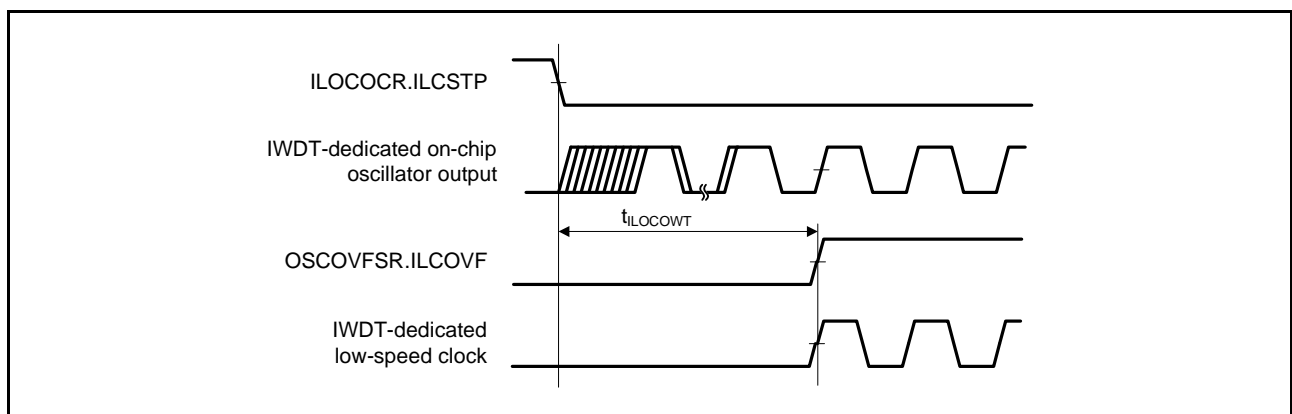


**Figure 5.7        IWDT-dedicated Low-Speed Clock Oscillation Start Timing**

### 5.3.3 Timing of Recovery from Low Power Consumption Modes

**Table 5.18 Timing of Recovery from Low Power Consumption Modes (1)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $t_{SBYOSCWT}$[2] | $t_{SBYSEQ}$[3] | | |
| Recovery time after cancellation of software standby mode[1] | Crystal resonator connected to main clock oscillator | Main clock oscillator operating | $t_{SBYMC}$ | — | — | {(MSTS[7:0] bit × 32) + 76} / 0.216 | 100 μs + 7/$f_{ICLK}$ + 2n/$f_{MAIN}$ | μs | Figure 5.12 |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPC}$ | | | {(MSTS[7:0] bit × 32) + 138} / 0.216 | 100 μs + 7/$f_{ICLK}$ + 2n/$f_{PLL}$ | | |
| | External clock input to main clock oscillator | Main clock oscillator operating | $t_{SBYEX}$ | | | 352 | 100 μs + 7/$f_{ICLK}$ + 2n/$f_{EXMAIN}$ | | |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPE}$ | | | 639 | 100 μs + 7/$f_{ICLK}$ + 2n/$f_{PLL}$ | | |
| | Sub-clock oscillator operating | | $t_{SBYSC}$ | | | {(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10/$f_{FCLK}$ | 100 μs + 4/$f_{ICLK}$ + 2n/$f_{SUB}$ | | |
| | High-speed on-chip oscillator operating | High-speed on-chip oscillator operating | $t_{SBYHO}$ | | | 454 | 100 μs + 7/$f_{ICLK}$ + 2n/$f_{HOCO}$ | | |
| | | High-speed on-chip oscillator operating and PLL circuit operating | $t_{SBYPH}$ | | | 741 | 100 μs + 7/$f_{ICLK}$ + 2n/$f_{PLL}$ | | |
| | Low-speed on-chip oscillator operating[4] | | $t_{SBYLO}$ | | | 338 | 100 μs + 7/$f_{ICLK}$ + 2n/$f_{LOCO}$ | | |

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWTO}$) and the time required for operations by the software standby release sequencer ($t_{SBYSEQ}$).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when $f_{ICLK}$:$f_{FCLK}$ = 1:1, 2:1, or 4:1.

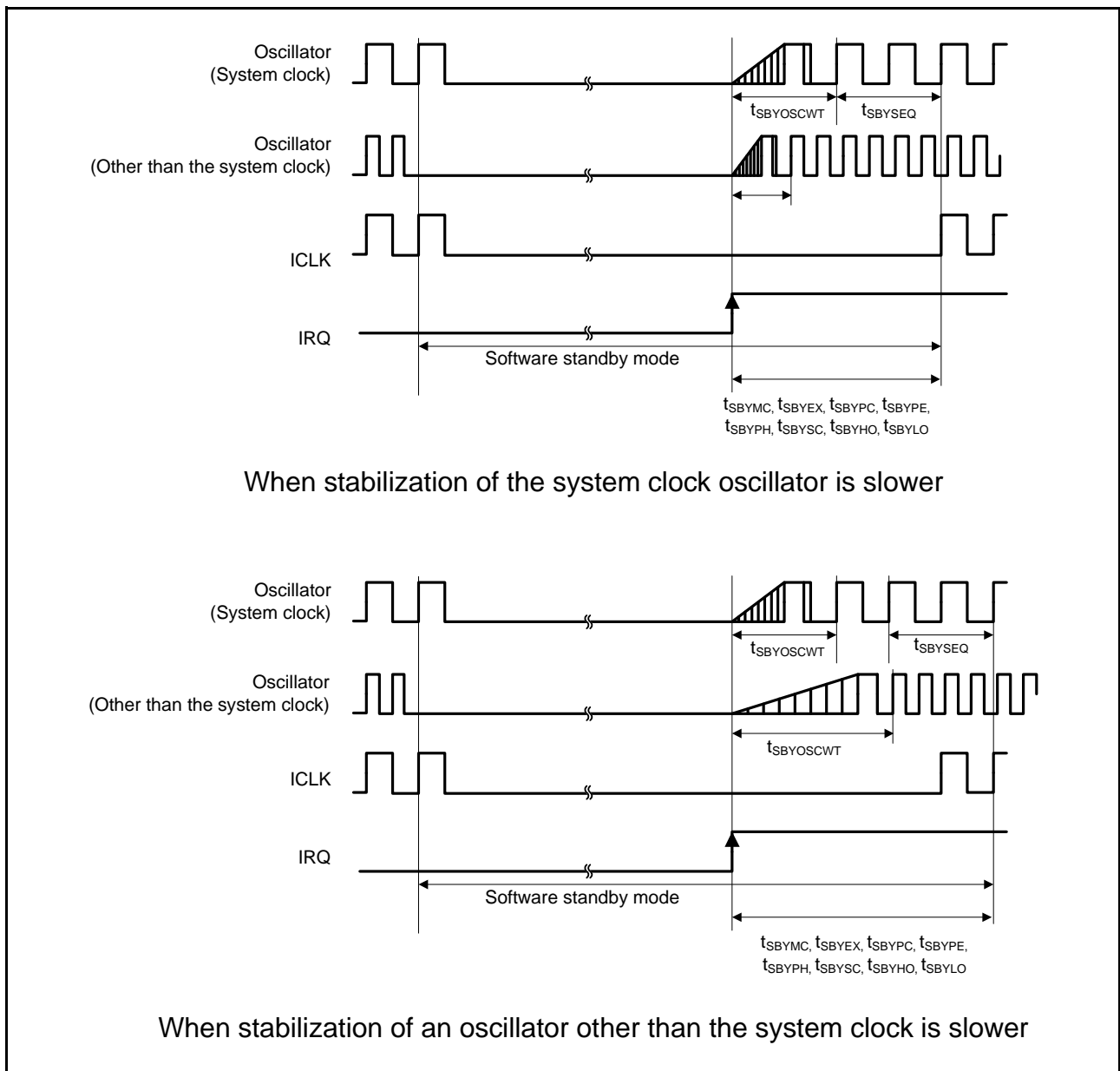When stabilization of the system clock oscillator is slower

When stabilization of an oscillator other than the system clock is slower

**Figure 5.12    Software Standby Mode Cancellation Timing**

**Table 5.32    SCI and SCIF Timing**

Conditions:  VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a$ = $T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min.[1] | Max.[1] | Unit[1] | Test Conditions |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{PBcyc}$ | Figure 5.44 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous[2] | $t_{Scyc}$ | 8 | — | $t_{PBcyc}$ | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Transmit data delay time | Clock synchronous | $t_{TXD}$ | — | 28 | ns | Figure 5.45 |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 15 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 5 | — | ns | |
| SCIF | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{PAcyc}$ | Figure 5.44 |
| | | Clock synchronous | | 12 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous[3] | $t_{Scyc}$ | 8 | — | $t_{PAcyc}$ | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Transmit data delay time | Master | $t_{TXD}$ | — | 10 | ns | Figure 5.45 |
| | | Slave | | — | $4 \times t_{PAcyc} + 20$ | | |
| | Receive data setup time | Master | $t_{RXS}$ | $3 \times t_{PAcyc} + 20$ | — | ns | |
| | | Slave | | $t_{PAcyc} + 10$ | — | | |
| | Receive data hold time | Master | $t_{RXH}$ | $-3 \times t_{PAcyc} + 5$ | — | ns | |
| | | Slave | | $2 \times t_{PAcyc} + 10$ | — | | |

Note 1.   $t_{PBcyc}$: PCLKB cycle; $t_{PAcyc}$: PCLKA cycle
Note 2.   When the SEMR.ABCS and SEMR.BGDM bits are set to 1
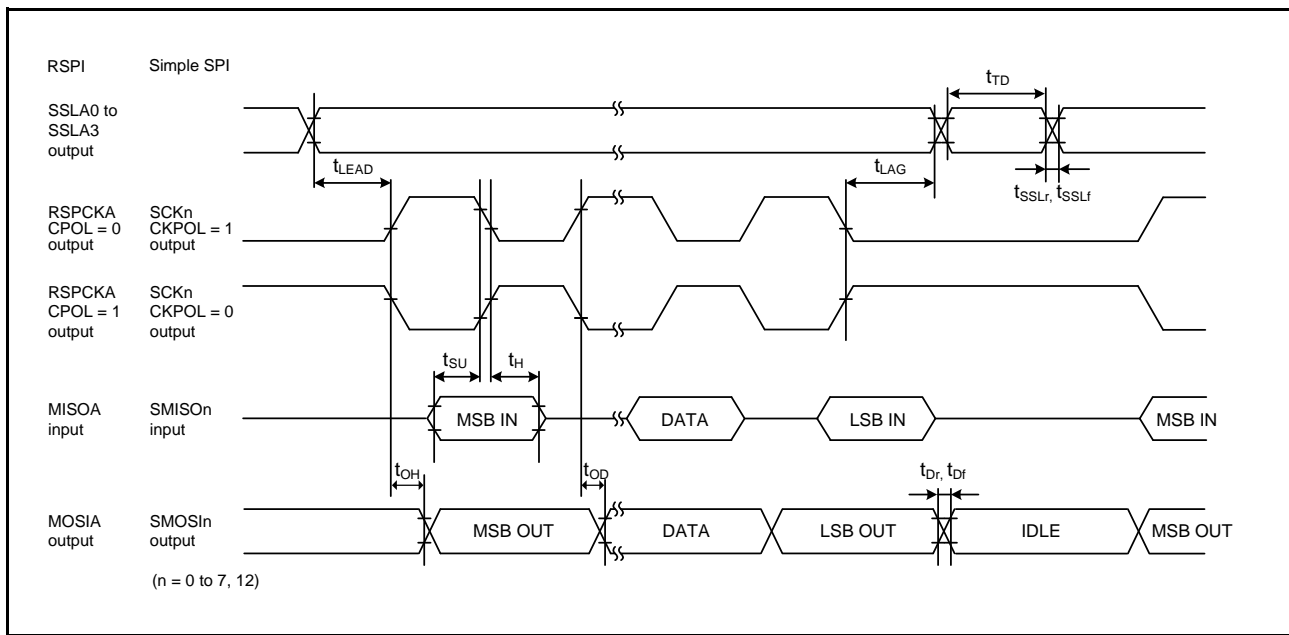Note 3.   When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1

**Figure 5.49    RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)**
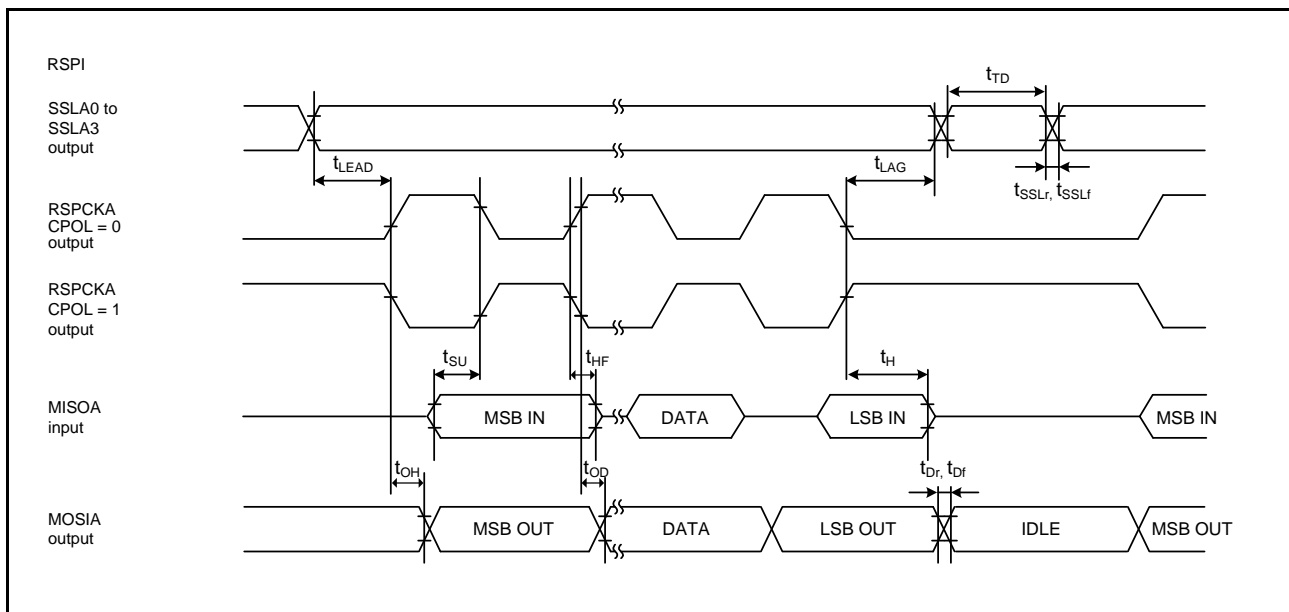


**Figure 5.50    RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)**

**Table 5.39    MMC Host Interface Timing**

Conditions:   VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
          VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
          VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
          PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a$ = $T_{opr}$
          Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
          High-drive output is selected by the driving ability control register.

| | Item | Symbol | Min.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| MMCIF | MMC_CLK clock cycle | $t_{MMCPP}$ | $2 × t_{PBcyc}$ | — | ns | Figure 5.61 |
| | MMC_CLK clock high level width | $t_{MMCWH}$ | 6.5 | — | ns | |
| | MMC_CLK clock low level width | $t_{MMCWL}$ | 6.5 | — | ns | |
| | MMC_CLK clock rising time | $t_{MMCLH}$ | — | 5 | ns | |
| | MMC_CLK clock falling time | $t_{MMCHL}$ | — | 5 | ns | |
| | MMC_CMD, MMC_D7 to MMC_D0 output data delay (data transfer mode) | $t_{MMCODLY}$ | –6.5 | 6.5 | ns | |
| | MMC_CMD, MMC_D7 to MMC_D0 input data setup | $t_{MMCISU}$ | 8 | — | ns | |
| | MMC_CMD, MMC_D7 to MMC_D0 input data hold | $t_{MMCIH}$ | 2 | — | ns | |

Note 1.   $t_{PBcyc}$: PCLKB cycle
Note 2.   We recommend using pins that have a letter ("-A", "-B", etc.) to indicate group membership appended to their names as groups.
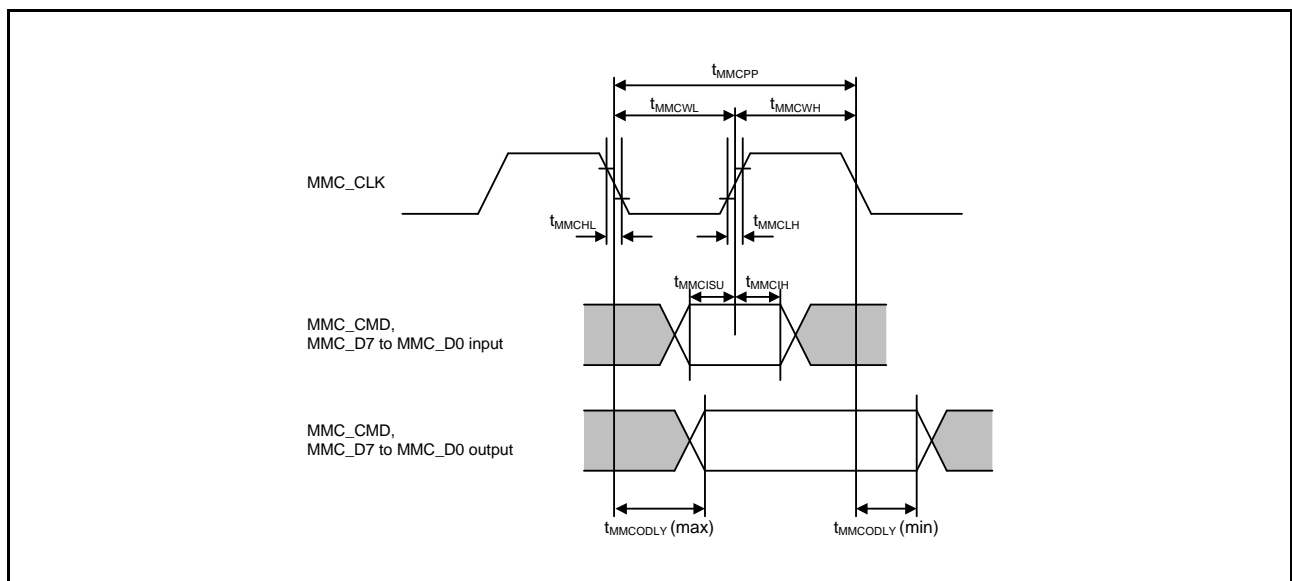          For the MMC interface, the AC portion of the electrical characteristics is measured for each group.



**Figure 5.61    MMC Interface**