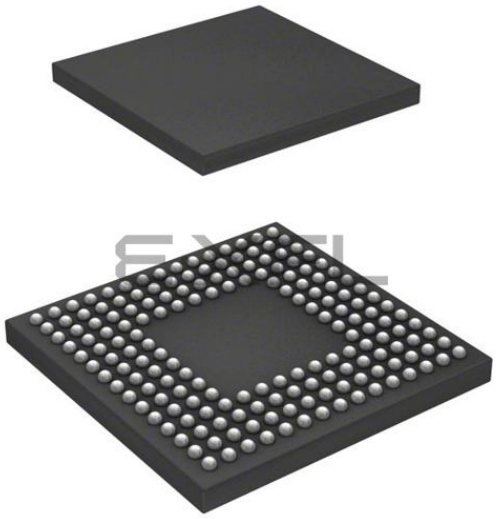

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RXv2 |
| Core Size | 32-Bit Single-Core |
| Speed | 240MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 127 |
| Program Memory Size | 2.5MB (2.5M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x12b, 21x12b; D/A 2x12 |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LFBGA |
| Supplier Device Package | 176-LFBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mgcdbg-20 |

# 1. Overview

## 1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package and the code flash memory capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

**Table 1.1 Outline of Specifications (1/10)**

| Classification | Module/Function | Description |
|---|---|---|
| CPU | CPU | • Maximum operating frequency: 240 MHz<br>• 32-bit RX CPU (RXv2)<br>• Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>• Address space: 4-Gbyte linear<br>• Register set of the CPU<br>General purpose: Sixteen 32-bit registers<br>Control: Ten 32-bit registers<br>Accumulator: Two 72-bit registers<br>• Basic instructions: 75<br>• Floating-point instructions: 11<br>• DSP instructions: 23<br>• Addressing modes: 11<br>• Data arrangement<br>Instructions: Little endian<br>Data: Selectable as little endian or big endian<br>• On-chip 32-bit multiplier: 32 × 32 → 64 bits<br>• On-chip divider: 32 / 32 → 32 bits<br>• Barrel shifter: 32 bits |
| | FPU | • Single precision (32-bit) floating point<br>• Data types and floating-point exceptions in conformance with the IEEE754 standard |
| Memory | Code flash memory | • Capacity: 2 Mbytes, 2.5 Mbytes, 3 Mbytes, 4 Mbytes<br>• No-wait access at up to 120 MHz, single wait access at frequencies above 120 MHz<br>• No-wait access to instructions and operands when the AFU is hit in operation at 240 MHz<br>• On-board programming: Four types<br>• Off-board programming (parallel programmer mode)<br>• The trusted memory (TM) function protects against the reading of programs from blocks 8 and 9. |
| | Data flash memory | • Capacity: 64 Kbytes<br>• Programming/erasing: 100,000 times |
| | RAM | • Capacity: 512 Kbytes<br>• 0000 0000h to 0003 FFFFh (256 Kbytes): 240 MHz No-wait access<br>0004 0000h to 0007 FFFFh (256 Kbytes): No-wait access at up to 120 MHz, single wait access at frequencies above 120 MHz |
| | RAM with ECC | • Capacity: 32 Kbytes<br>• Single wait access at up to 120 MHz, two wait accesses for reading and three wait accesses for writing at frequencies above 120 MHz<br>• SEC-DED (single error correction/double error detection) |
| | Standby RAM | • Capacity: 8 Kbytes<br>• Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access |

**Table 1.2 Comparison of Functions for Different Packages (2/2)**

| Functions | RX71M Group | | |
|---|---|---|---|
| **Package** | **177 Pins, 176 Pins** | **145 Pins, 144 Pins** | **100 Pins** |
| DES | Available | | |
| SHA | Available | | |
| RNG | Available | | |
| Event link controller | Available | | |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/7)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| A1 | AVSS0 | | | | | | | |
| A2 | AVCC0 | | | | | | | |
| A3 | VREFL0 | | | | | | | |
| A4 | | P42 | | | | | IRQ10-DS | AN002 |
| A5 | | P46 | | | | | IRQ14-DS | AN006 |
| A6 | VCC | | | | | | | |
| A7 | VSS | | | | | | | |
| A8 | | P94 | A20/D20 | | ET1_ERXD0/ RMII1_RXD0 | | | |
| A9 | VCC | | | | | | | |
| A10 | | P97 | A23/D23 | | ET1_ERXD3 | | | |
| A11 | | PD6 | D6[A6/D6] | MTIC5V/MTIOC8A/ POE4# | | MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B | IRQ6 | AN106 |
| A12 | | P60 | CS0# | | ET1_TX_EN/ RMII1_TXD_EN | | | |
| A13 | | P63 | CS3#/CAS# | | | | | |
| A14 | | PE1 | D9[A9/D9] | MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | | ANEX1 |
| A15 | | PE2 | D10[A10/D10] | MTIOC4A/ GTIOC0B-A/PO23/ TIC3 | RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B | MMC_D6-B | IRQ7-DS | AN100 |
| B1 | | P05 | | | | | IRQ13 | DA1 |
| B2 | | P07 | | | | | IRQ15 | ADTRG0# |
| B3 | | P40 | | | | | IRQ8-DS | AN000 |
| B4 | | P41 | | | | | IRQ9-DS | AN001 |
| B5 | | P47 | | | | | IRQ15-DS | AN007 |
| B6 | | P91 | A17/D17 | | ET1_COL/SCK7 | | | AN115 |
| B7 | | P92 | A18/D18 | POE4# | ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7 | | | AN116 |
| B8 | | PD1 | D1[A1/D1] | MTIOC4B/ GTIOC1A-E/POE0# | CTX0 | | IRQ1 | AN109 |
| B9 | | P96 | A22/D22 | | ET1_ERXD2 | | | |
| B10 | | PD4 | D4[A4/D4] | MTIOC8B/POE11# | | MMC_CMD-B/ SDHI_CMD-B/ QSSL-B | IRQ4 | AN112 |
| B11 | | PG1 | D25 | | ET1_RX_ER/ RMII1_RX_ER | | | |
| B12 | VSS | | | | | | | |
| B13 | | P64 | CS4#/WE# | | | | | |
| B14 | | PE0 | D8[A8/D8] | MTIOC3D/ GTIOC2B-A | SCK12/SSLB1-B | MMC_D4-B | | ANEX0 |
| B15 | | PE3 | D11[A11/D11] | MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3 | CTS12#/RTS12#/ SS12#/ ET0_ERXD3 | MMC_D7-B | | AN101 |
| C1 | AVSS1 | | | | | | | |
| C2 | AVCC1 | | | | | | | |
| C3 | VREFH0 | | | | | | | |

**Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (3/4)**

| Pin Number 100-Pin LQFP | Power Supply Clock System Contro | I/O Port | Bus EXDMAC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 56 | | PB4 | A12 | TIOCA4/PO28 | CTS9#/ET0_TX_EN/ RMII0_TXD_EN | | | |
| 57 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11# | SCK6/ET0_RX_ER/ RMII0_RX_ER | | | |
| 58 | | PB2 | A10 | TIOCC3/TCLKC/ PO26 | CTS6#/RTS6#SS6#/ ET0_RX_CLK/ REF50CK0 | | | |
| 59 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0 | | IRQ4-DS | |
| 60 | VCC | | | | | | | |
| 61 | | PB0 | A8 | MTIC5W/TIOCA3/ PO24 | RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1 | | IRQ12 | |
| 62 | VSS | | | | | | | |
| 63 | | PA7 | A7 | TIOCB2/PO23 | MISOA-B/ET0_WOL | | | |
| 64 | | PA6 | A6 | MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10# | CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT | | | |
| 65 | | PA5 | A5 | MTIOC6B/TIOCB1/ GTIOC0A-C/PO21 | RSPCKA-B/ ET0_LINKSTA | | | |
| 66 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC | | IRQ5-DS | |
| 67 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19 | RXD5/SMISO5/ SSCL5/ET0_MDIO | | IRQ6-DS | |
| 68 | | PA2 | A2 | MTIOC7A/ GTIOC1A-C/PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | | |
| 69 | | PA1 | A1 | MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17 | SCK5/SSLA2-B/ ET0_WOL | | IRQ11 | |
| 70 | | PA0 | A0/BC0# | MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16 | SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN | | | |
| 71 | | PE7 | D15[A15/D15] | MTIOC6A/ GTIOC3A-E/TOC1 | MISOB-B | MMC_RES#-B/ SDHI_WP-B | IRQ7 | AN105 |
| 72 | | PE6 | D14[A14/D14] | TIOC6C/GTIOC3B-E/ TIC1 | MOSIB-B | MMC_CD-B/ SDHI_CD-B | IRQ6 | AN104 |
| 73 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B/ GTIOC0A-A | ET0_RX_CLK/ REF50CK0/ RSPCKB-B | | IRQ5 | AN103 |
| 74 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28 | ET0_ERXD2/SSLB0-B | | | AN102 |
| 75 | | PE3 | D11[A11/D11] | MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3 | CTS12#/RTS12#/ SS12#/ET0_ERXD3 | MMC_D7-B | | AN101 |
| 76 | | PE2 | D10[A10/D10] | MTIOC4A/ GTIOC0B-A/PO23/ TIC3 | RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B | MMC_D6-B | IRQ7-DS | AN100 |
| 77 | | PE1 | D9[A9/D9] | MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | | ANEX1 |
| 78 | | PE0 | D8[A8/D8] | MTIOC3D/ GTIOC2B-A | SCK12/SSLB1-B | MMC_D4-B | | ANEX0 |
| 79 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | MMC_D1-B/ SDHI_D1-B/ QIO1-B/ QMI-B | IRQ7 | AN107 |

**Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (4/4)**

| Pin Number 100-Pin LQFP | Power Supply Clock System Contro | I/O Port | Bus EXDMAC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 80 | | PD6 | D6[A6/D6] | MTIC5V/MTIOC8A/ POE4# | | MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B | IRQ6 | AN106 |
| 81 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/ POE10# | | MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B | IRQ5 | AN113 |
| 82 | | PD4 | D4[A4/D4] | MTIOC8B/POE11# | | MMC_CMD-B/ SDHI_CMD-B/ QSSL-B | IRQ4 | AN112 |
| 83 | | PD3 | D3[A3/D3] | MTIOC8D/ GTIOC0A-E/POE8#/ TOC2 | | MMC_D3-B/ SDHI_D3-B/ QIO3-B | IRQ3 | AN111 |
| 84 | | PD2 | D2[A2/D2] | MTIOC4D/ GTIOC0B-E/TIC2 | CRX0 | MMC_D2-B/ SDHI_D2-B/ QIO2-B | IRQ2 | AN110 |
| 85 | | PD1 | D1[A1/D1] | MTIOC4B/ GTIOC1A-E/POE0# | CTX0 | | IRQ1 | AN109 |
| 86 | | PD0 | D0[A0/D0] | GTIOC1B-E/POE4# | | | IRQ0 | AN108 |
| 87 | | P47 | | | | | IRQ15-DS | AN007 |
| 88 | | P46 | | | | | IRQ14-DS | AN006 |
| 89 | | P45 | | | | | IRQ13-DS | AN005 |
| 90 | | P44 | | | | | IRQ12-DS | AN004 |
| 91 | | P43 | | | | | IRQ11-DS | AN003 |
| 92 | | P42 | | | | | IRQ10-DS | AN002 |
| 93 | | P41 | | | | | IRQ9-DS | AN001 |
| 94 | VREFL0 | | | | | | | |
| 95 | | P40 | | | | | IRQ8-DS | AN000 |
| 96 | VREFH0 | | | | | | | |
| 97 | AVCC0 | | | | | | | |
| 98 | | P07 | | | | | IRQ15 | ADTRG0# |
| 99 | AVSS0 | | | | | | | |
| 100 | P05 | | | | | | IRQ13 | DA1 |

**Table 4.1 List of I/O Registers (Address Order) (7 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 3880h | BSC | CS Recovery Cycle Insertion Enable Register | CSRECEN | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3C00h | BSC | SDC Control Register | SDCCR | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C01h | BSC | SDC Mode Register | SDCMOD | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C02h | BSC | SDRAM Access Mode Register | SDAMOD | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C10h | BSC | SDRAM Self-Refresh Control Register | SDSELF | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C14h | BSC | SDRAM Refresh Control Register | SDRFCR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3C16h | BSC | SDRAM Auto-Refresh Control Register | SDRFEN | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C20h | BSC | SDRAM Initialization Sequence Control Register | SDICR | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C24h | BSC | SDRAM Initialization Register | SDIR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3C40h | BSC | SDRAM Address Register | SDADR | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C44h | BSC | SDRAM Timing Register | SDTR | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3C48h | BSC | SDRAM Mode Register | SDMOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3C50h | BSC | SDRAM Status Register | SDSR | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 6400h | MPU | Region-0 Start Page Number Register | RSPAGE0 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6404h | MPU | Region-0 End Page Number Register | REPAGE0 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6408h | MPU | Region-1 Start Page Number Register | RSPAGE1 | 32 | 32 | 1 ICLK | | MPU |
| 0008 640Ch | MPU | Region-1 End Page Number Register | REPAGE1 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6410h | MPU | Region-2 Start Page Number Register | RSPAGE2 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6414h | MPU | Region-2 End Page Number Register | REPAGE2 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6418h | MPU | Region-3 Start Page Number Register | RSPAGE3 | 32 | 32 | 1 ICLK | | MPU |
| 0008 641Ch | MPU | Region-3 End Page Number Register | REPAGE3 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6420h | MPU | Region-4 Start Page Number Register | RSPAGE4 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6424h | MPU | Region-4 End Page Number Register | REPAGE4 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6428h | MPU | Region-5 Start Page Number Register | RSPAGE5 | 32 | 32 | 1 ICLK | | MPU |
| 0008 642Ch | MPU | Region-5 End Page Number Register | REPAGE5 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6430h | MPU | Region-6 Start Page Number Register | RSPAGE6 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6434h | MPU | Region-6 End Page Number Register | REPAGE6 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6438h | MPU | Region-7 Start Page Number Register | RSPAGE7 | 32 | 32 | 1 ICLK | | MPU |
| 0008 643Ch | MPU | Region-7 End Page Number Register | REPAGE7 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6500h | MPU | Memory-Protection Enable Register | MPEN | 32 | 32 | 1 ICLK | | MPU |
| 0008 6504h | MPU | Background Access Control Register | MPBAC | 32 | 32 | 1 ICLK | | MPU |
| 0008 6508h | MPU | Memory-Protection Error Status-Clearing Register | MPECLR | 32 | 32 | 1 ICLK | | MPU |
| 0008 650Ch | MPU | Memory-Protection Error Status Register | MPESTS | 32 | 32 | 1 ICLK | | MPU |
| 0008 6514h | MPU | Data Memory-Protection Error Address Register | MPDEA | 32 | 32 | 1 ICLK | | MPU |
| 0008 6520h | MPU | Region Search Address Register | MPSA | 32 | 32 | 1 ICLK | | MPU |
| 0008 6524h | MPU | Region Search Operation Register | MPOPS | 16 | 16 | 1 ICLK | | MPU |
| 0008 6526h | MPU | Region Invalidation Operation Register | MPOPI | 16 | 16 | 1 ICLK | | MPU |
| 0008 6528h | MPU | Instruction-Hit Region Register | MHITI | 32 | 32 | 1 ICLK | | MPU |
| 0008 652Ch | MPU | Data-Hit Region Register | MHITD | 32 | 32 | 1 ICLK | | MPU |
| 0008 6610h | SYSTEM | Memory Wait Cycle Setting Register | MEMWAIT | 32 | 32 | 1 ICLK | | RAM |
| 0008 7010h to 0008 70FFh | ICU | Interrupt Request Registers 016 to 255 | IR016 to 255 | 8 | 8 | 2 ICLK | | ICUA |
| 0008 711Ah to 0008 71FFh | ICU | DTC Start Enable Registers 026 to 255 | DTCER026 to DTCER255 | 8 | 8 | 2 ICLK | | ICUA |
| 0008 7202h to 0008 721Fh | ICU | Interrupt Request Enable Registers 02 to 1F | IER02 to IER1F | 8 | 8 | 2 ICLK | | ICUA |
| 0008 72E0h | ICU | Software Interrupt Generation Register | SWINTR | 8 | 8 | 2 ICLK | | ICUA |
| 0008 72E1h | ICU | Software Interrupt 2 Generation Register | SWINT2R | 8 | 8 | 2 ICLK | | ICUA |
| 0008 72F0h | ICU | Fast Interrupt Set Register | FIR | 16 | 16 | 2 ICLK | | ICUA |
| 0008 7300h to 0008 73FFh | ICU | Interrupt Source Priority Registers 000 to 255 | IPR000 to IPR255 | 8 | 8 | 2 ICLK | | ICUA |

**Table 4.1 List of I/O Registers (Address Order) (16 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 821Bh | TMR3 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 821Ch | TMR2 | Time Count Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 821Dh | TMR3 | Time Count Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8280h | CRC | CRC Control Register | CRCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CRC |
| 0008 8281h | CRC | CRC Data Input Register | CRCDIR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CRC |
| 0008 8282h | CRC | CRC Data Output Register | CRCDOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CRC |
| 0008 8300h | RIIC0 | I2C Bus Control Register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8301h | RIIC0 | I2C Bus Control Register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8302h | RIIC0 | I2C Bus Mode Register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8303h | RIIC0 | I2C Bus Mode Register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8304h | RIIC0 | I2C Bus Mode Register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8305h | RIIC0 | I2C Bus Function Enable Register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8306h | RIIC0 | I2C Bus Status Enable Register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8307h | RIIC0 | I2C Bus Interrupt Enable Register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8308h | RIIC0 | I2C Bus Status Register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8309h | RIIC0 | I2C Bus Status Register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Ah | RIIC0 | Slave Address Register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Bh | RIIC0 | Slave Address Register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Ch | RIIC0 | Slave Address Register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Dh | RIIC0 | Slave Address Register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Eh | RIIC0 | Slave Address Register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Fh | RIIC0 | Slave Address Register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8310h | RIIC0 | I2C Bus Bit Rate Low Register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8311h | RIIC0 | I2C Bus Bit Rate High Register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8312h | RIIC0 | I2C Bus Transmit Data Register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8313h | RIIC0 | I2C Bus Receive Data Register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8340h | RIIC2 | I2C Bus Control Register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8341h | RIIC2 | I2C Bus Control Register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8342h | RIIC2 | I2C Bus Mode Register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8343h | RIIC2 | I2C Bus Mode Register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8344h | RIIC2 | I2C Bus Mode Register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8345h | RIIC2 | I2C Bus Function Enable Register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8346h | RIIC2 | I2C Bus Status Enable Register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8347h | RIIC2 | I2C Bus Interrupt Enable Register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8348h | RIIC2 | I2C Bus Status Register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8349h | RIIC2 | I2C Bus Status Register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Ah | RIIC2 | Slave Address Register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Bh | RIIC2 | Slave Address Register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Ch | RIIC2 | Slave Address Register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Dh | RIIC2 | Slave Address Register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Eh | RIIC2 | Slave Address Register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Fh | RIIC2 | Slave Address Register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8350h | RIIC2 | I2C Bus Bit Rate Low Register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8351h | RIIC2 | I2C Bus Bit Rate High Register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8352h | RIIC2 | I2C Bus Transmit Data Register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8353h | RIIC2 | I2C Bus Receive Data Register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8500h | MMCIF | Command Setting Register | CECMDSET | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8508h | MMCIF | Argument Register | CEARG | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 850Ch | MMCIF | CMD12 Argument Register | CEARGCMD12 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |

**Table 4.1 List of I/O Registers (Address Order) (37 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0009 0852h | CAN0 | Mailbox Search Status Register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0853h | CAN0 | Mailbox Search Mode Register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0854h | CAN0 | Time Stamp Register | TSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0856h | CAN0 | Acceptance Filter Support Register | AFSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0858h | CAN0 | Test Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1200h to 0009 13FFh | CAN1 | Mailbox Registers 0 to 31 | MB0 to 31 | 128 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1400h to 0009 141Fh | CAN1 | Mask Registers 0 to 7 | MKR0 to 7 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1420h | CAN1 | FIFO Received ID Compare Register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1424h | CAN1 | FIFO Received ID Compare Register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1428h | CAN1 | Mask Invalid Register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 142Ch | CAN1 | Mailbox Interrupt Enable Register | MIER | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1820h to 0009 183Fh | CAN1 | Message Control Registers 0 to 31 | MCTL0 to 31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1840h | CAN1 | Control Register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1842h | CAN1 | Status Register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1844h | CAN1 | Bit Configuration Register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1848h | CAN1 | Receive FIFO Control Register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1849h | CAN1 | Receive FIFO Pointer Control Register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Ah | CAN1 | Transmit FIFO Control Register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Bh | CAN1 | Transmit FIFO Pointer Control Register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Ch | CAN1 | Error Interrupt Enable Register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Dh | CAN1 | Error Interrupt Factor Judge Register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Eh | CAN1 | Receive Error Count Register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Fh | CAN1 | Transmit Error Count Register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1850h | CAN1 | Error Code Store Register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1851h | CAN1 | Channel Search Support Register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1852h | CAN1 | Mailbox Search Status Register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1853h | CAN1 | Mailbox Search Mode Register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1854h | CAN1 | Time Stamp Register | TSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1856h | CAN1 | Acceptance Filter Support Register | AFSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1858h | CAN1 | Test Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2200h to 0009 23FFh | CAN2 | Mailbox Registers 0 to 31 | MB0 to 31 | 128 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2400h to 0009 241Fh | CAN2 | Mask Registers 0 to 7 | MKR0 to 7 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2420h | CAN2 | FIFO Received ID Compare Register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2424h | CAN2 | FIFO Received ID Compare Register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2428h | CAN2 | Mask Invalid Register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 242Ch | CAN2 | Mailbox Interrupt Enable Register | MIER | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2820h to 0009 283Fh | CAN2 | Message Control Registers 0 to 31 | MCTL0 to 31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2840h | CAN2 | Control Register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2842h | CAN2 | Status Register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2844h | CAN2 | Bit Configuration Register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2848h | CAN2 | Receive FIFO Control Register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 2849h | CAN2 | Receive FIFO Pointer Control Register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |

**Table 4.1 List of I/O Registers (Address Order) (40 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000A 0056h | USB0 | USB Request Value Register | USBVAL | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 0058h | USB0 | USB Request Index Register | USBINDX | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 005Ah | USB0 | USB Request Length Register | USBLENG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 005Ch | USB0 | DCP Configuration Register | DCPCFG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 005Eh | USB0 | DCP Maximum Packet Size Register | DCPMAXP | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 0060h | USB0 | DCP Control Register | DCPCTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 0064h | USB0 | Pipe Window Select Register | PIPESEL | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 0068h | USB0 | Pipe Configuration Register | PIPECFG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 006Ch | USB0 | Pipe Maximum Packet Size Register | PIPEMAXP | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 006Eh | USB0 | Pipe Cycle Control Register | PIPEPERI | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 0070h | USB0 | Pipe1 Control Register | PIPE1CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 0072h | USB0 | Pipe2 Control Register | PIPE2CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 0074h | USB0 | Pipe3 Control Register | PIPE3CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 0076h | USB0 | Pipe4 Control Register | PIPE4CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 0078h | USB0 | Pipe5 Control Register | PIPE5CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 007Ah | USB0 | Pipe6 Control Register | PIPE6CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 007Ch | USB0 | Pipe7 Control Register | PIPE7CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |
| 000A 007Eh | USB0 | Pipe8 Control Register | PIPE8CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB)*5 | USBb |

**Table 4.1 List of I/O Registers (Address Order) (47 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1270h | MTU | Timer Mode Register 2A | TMDR2A | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1272h | MTU3 | Timer General Register E | TGRE | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1274h | MTU4 | Timer General Register E | TGRE | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1276h | MTU4 | Timer General Register F | TGRF | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1280h | MTU | Timer Start Register A | TSTRA | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1281h | MTU | Timer Synchronous Register A | TSYRA | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1282h | MTU | Timer Counter Synchronous Start Register | TCSYSTR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1284h | MTU | Timer Read/Write Enable Register A | TRWERA | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1290h | MTU0 | Noise Filter Control Register 0 | NFCR0 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1291h | MTU1 | Noise Filter Control Register 1 | NFCR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1292h | MTU2 | Noise Filter Control Register 2 | NFCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1293h | MTU3 | Noise Filter Control Register 3 | NFCR3 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1294h | MTU4 | Noise Filter Control Register 4 | NFCR4 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1298h | MTU8 | Noise Filter Control Register 8 | NFCR8 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1299h | MTU0 | Noise Filter Control Register C | NFCRC | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1300h | MTU0 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1301h | MTU0 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1302h | MTU0 | Timer I/O Control Register H | TIORH | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1303h | MTU0 | Timer I/O Control Register L | TIORL | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1304h | MTU0 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1306h | MTU0 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1308h | MTU0 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 130Ah | MTU0 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 130Ch | MTU0 | Timer General Register C | TGRC | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 130Eh | MTU0 | Timer General Register D | TGRD | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1320h | MTU0 | Timer General Register E | TGRE | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1322h | MTU0 | Timer General Register F | TGRF | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1324h | MTU0 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1325h | MTU0 | Timer Status Register 2 | TSR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1326h | MTU0 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1328h | MTU0 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1380h | MTU1 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1381h | MTU1 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1382h | MTU1 | Timer I/O Control Register | TIOR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1384h | MTU1 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1385h | MTU1 | Timer Status Register | TSR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1386h | MTU1 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1388h | MTU1 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 138Ah | MTU1 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1390h | MTU1 | Timer Input Capture Control Register | TICCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1391h | MTU1 | Timer Mode Register 3 | TMDR3 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1394h | MTU1 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 13A0h | MTU1 | Timer Longword Counter | TCNTLW | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 13A4h | MTU1 | Timer Longword General Register | TGRALW | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 13A8h | MTU1 | Timer Longword General Register | TGRBLW | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1400h | MTU2 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1401h | MTU2 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1402h | MTU2 | Timer I/O Control Register | TIOR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1404h | MTU2 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1405h | MTU2 | Timer Status Register | TSR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (67 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000D 0564h | USBA | Deep Standby USB Suspend/Resume Interrupt Register | DPUSR1R | 32 | 32 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBAa |

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 0008 81ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 0008 81EEh and 0008 81ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 0008 81EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 0008 81EFh and 0008 81EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 0008 81FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 0008 81FEh and 0008 81FCh, respectively.

Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 0008 81FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 0008 81FFh and 0008 81FDh, respectively.

Note 5. When the register is accessed while the USB is operating, a delay may be generated in accessing.

**Table 5.3 DC Characteristics (2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output high voltage | All output pins | $V_{OH}$ | VCC – 0.5 | — | — | V | $I_{OH}$ = –1 mA |
| Output low voltage | All output pins (except for RIIC pins and ETHERC output pin) | $V_{OL}$ | — | — | 0.5 | V | $I_{OL}$ = 1.0 mA |
| | RIIC output pin | | — | — | 0.4 | | $I_{OL}$ = 3.0 mA |
| | | | — | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| | RIIC output pin (only P12 and P13 in channel 0) | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 15.0 mA (ICFER.FMPE = 1) |
| | | | — | 0.4 | — | | $I_{OL}$ = 20.0 mA (ICFER.FMPE = 1) |
| | ETHERC output pin | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.0 mA |
| Input leakage current | RES#, MD pin, EMLE*1, BSCANP*1, NMI | $\lvert I_{in} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| Three-state leakage current (off state) | Other than ports for 5 V tolerant | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| | Ports for 5 V tolerant | | — | — | 5.0 | | $V_{in}$ = 0 V<br>$V_{in}$ = 5.5 V |
| Input pull-up MOS current | Ports 0 to 2, 3, 4 to G, J3, J5 | $I_p$ | –300 | — | –10 | µA | VCC = 2.7 to 3.6 V<br>$V_{in}$ = 0 V |
| Input pull-down MOS current | EMLE, BSCANP | $I_p$ | 10 | — | 300 | µA | $V_{in}$ = VCC |
| Input capacitance | All input pins (except for ports 03, 05, 12, 13, 16, 17, EMLE, BSCANP, USB0_DP, USB0_DM, USBA_DP, and USBA_DM) | $C_{in}$ | — | — | 8 | pF | Vbias = 0 V<br>Vamp = 20 mV<br>f = 1 MHz<br>$T_a$ = 25°C |
| | Ports 03, 05, 12, 13, 16, 17, EMLE, BSCANP, USB0_DP, USB0_DM, USBA_DP, and USBA_DM | | — | — | 16 | | |

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when $V_{in}$ = 0 V.

### Table 5.6 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output low current (average value per pin) | All output pins*1 | Normal drive | $I_{OL}$ | — | — | 2.0 | mA |
| | All output pins*2 | High drive | $I_{OL}$ | — | — | 3.8 | mA |
| Permissible output low current (max. value per pin) | All output pins*1 | Normal drive | $I_{OL}$ | — | — | 4.0 | mA |
| | All output pins*2 | High drive | $I_{OL}$ | — | — | 7.6 | mA |
| Permissible output low current (total) | Total of all output pins | | $\Sigma I_{OL}$ | — | — | 80 | mA |
| Permissible output high current (average value per pin) | All output pins*1 | Normal drive | $I_{OH}$ | — | — | –2.0 | mA |
| | USB_DPUPE pin*2 | High drive | $I_{OH}$ | — | — | –3.8 | mA |
| Permissible output high current (max. value per pin) | All output pins*1 | Normal drive | $I_{OH}$ | — | — | –4.0 | mA |
| | All output pins*2 | High drive | $I_{OH}$ | — | — | –7.6 | mA |
| Permissible output high current (total) | Total of all output pins | | $\Sigma I_{OH}$ | — | — | –80 | mA |

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

## 5.3.1 Reset Timing

**Table 5.10 Reset Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RES# pulse width | Power-on | $t_{RESWP}$ | 1 | — | — | ms | Figure 5.1 |
| | Deep software standby mode | $t_{RESWD}$ | 0.6 | — | — | ms | Figure 5.2 |
| | Software standby mode, low-speed operating mode 2 | $t_{RESWS}$ | 0.3 | — | — | ms | |
| | Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory | $t_{RESWF}$ | 200 | — | — | µs | |
| | Other than above | $t_{RESW}$ | 200 | — | — | µs | |
| Waiting time after release from the RES# pin reset | | $t_{RESWT}$ | 62 | — | 63 | $t_{Lcyc}$ | Figure 5.1 |
| Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset) | | $t_{RESW2}$ | 108 | — | 116 | $t_{Lcyc}$ | |

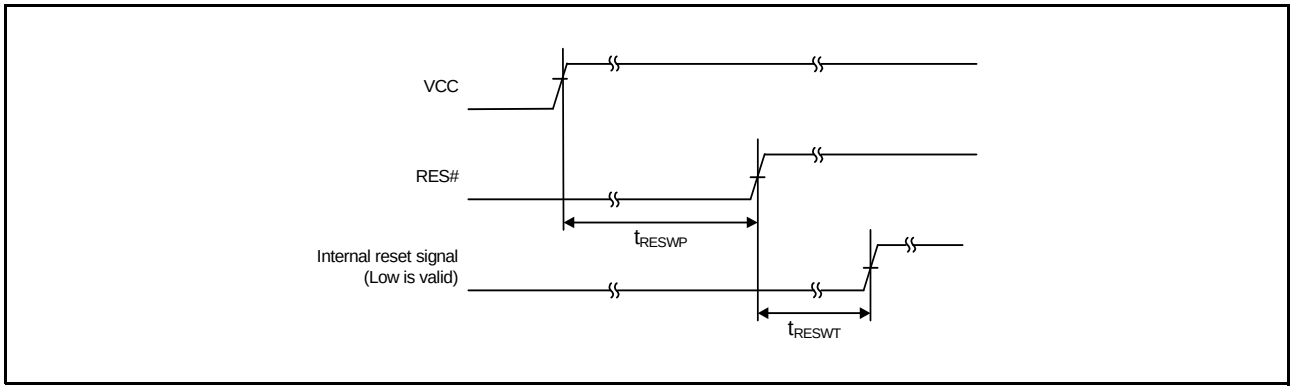


**Figure 5.1 Reset Input Timing at Power-On**

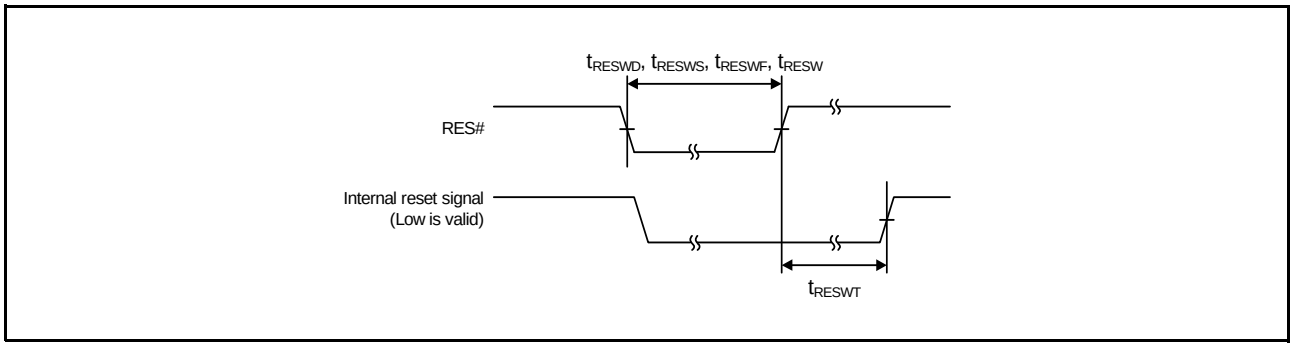


**Figure 5.2 Reset Input Timing**

## 5.3.3 Timing of Recovery from Low Power Consumption Modes

**Table 5.18 Timing of Recovery from Low Power Consumption Modes (1)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $t_{SBYOSCWT}$*2 | $t_{SBYSEQ}$*3 | | |
| Recovery time after cancellation of software standby mode*1 | Crystal resonator connected to main clock oscillator | Main clock oscillator operating | $t_{SBYMC}$ | — | — | {(MSTS[7:0] bit × 32) + 76} / 0.216 | 100 µs + 7/$f_{ICLK}$ + 2n/$f_{MAIN}$ | µs | Figure 5.12 |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPC}$ | | | {(MSTS[7:0] bit × 32) + 138} / 0.216 | 100 µs + 7/$f_{ICLK}$ + 2n/$f_{PLL}$ | | |
| | External clock input to main clock oscillator | Main clock oscillator operating | $t_{SBYEX}$ | | | 352 | 100 µs + 7/$f_{ICLK}$ + 2n/$f_{EXMAIN}$ | | |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPE}$ | | | 639 | 100 µs + 7/$f_{ICLK}$ + 2n/$f_{PLL}$ | | |
| | Sub-clock oscillator operating | | $t_{SBYSC}$ | | | {(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10/$f_{FCLK}$ | 100 µs + 4/$f_{ICLK}$ + 2n/$f_{SUB}$ | | |
| | High-speed on-chip oscillator operating | High-speed on-chip oscillator operating | $t_{SBYHO}$ | | | 454 | 100 µs + 7/$f_{ICLK}$ + 2n/$f_{HOCO}$ | | |
| | | High-speed on-chip oscillator operating and PLL circuit operating | $t_{SBYPH}$ | | | 741 | 100 µs + 7/$f_{ICLK}$ + 2n/$f_{PLL}$ | | |
| | Low-speed on-chip oscillator operating*4 | | $t_{SBYLO}$ | | | 338 | 100 µs + 7/$f_{ICLK}$ + 2n/$f_{LOCO}$ | | |

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWTO}$) and the time required for operations by the software standby release sequencer ($t_{SBYSEQ}$).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when $f_{ICLK}$:$f_{FCLK}$ = 1:1, 2:1, or 4:1.

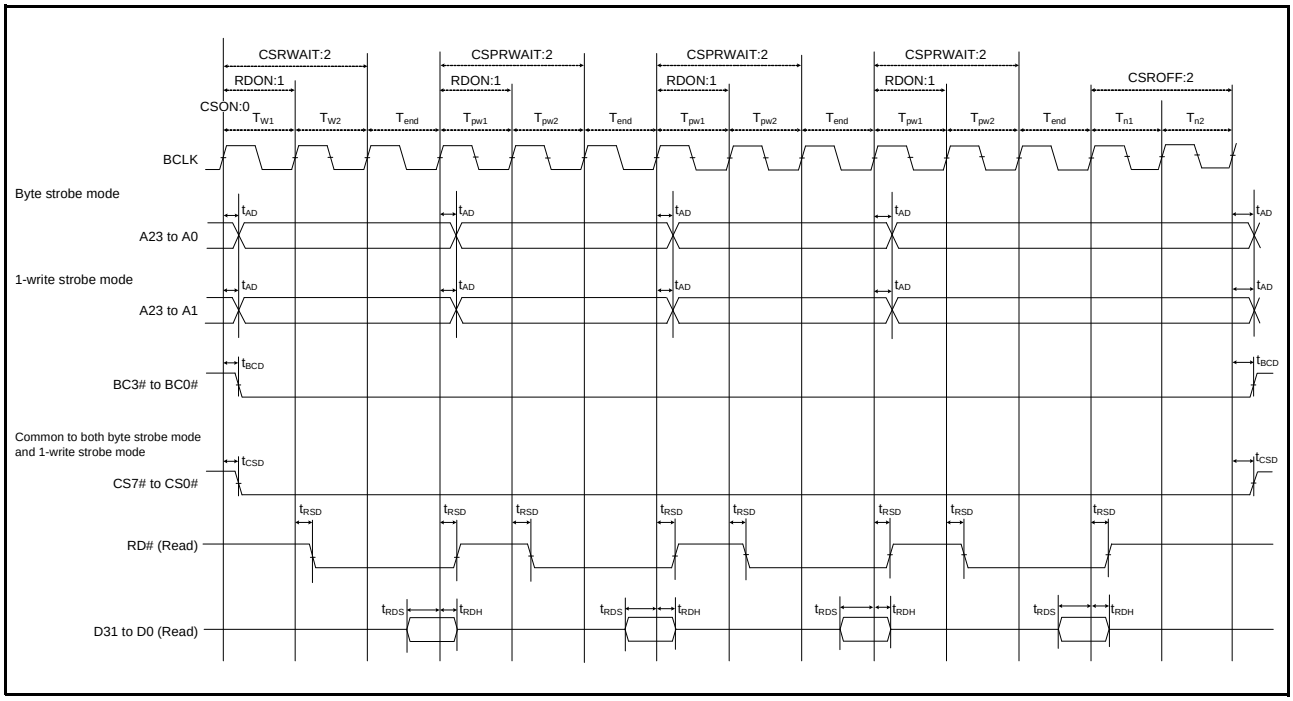


**Figure 5.20 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)**

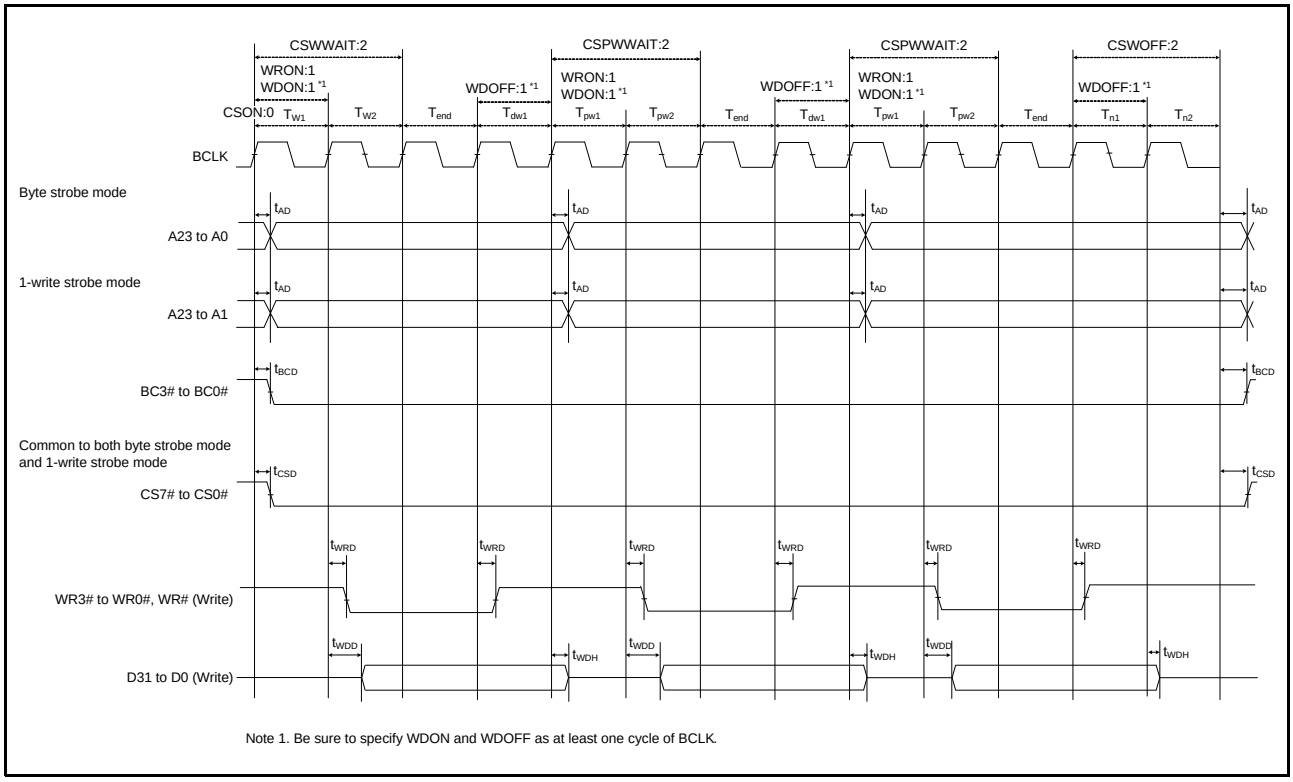


**Figure 5.21 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)**

## 5.3.7 Timing of On-Chip Peripheral Modules

**Table 5.23 I/O Port Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | $t_{PRW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.33 |

Note 1. $t_{PBcyc}$: PCLKB cycle

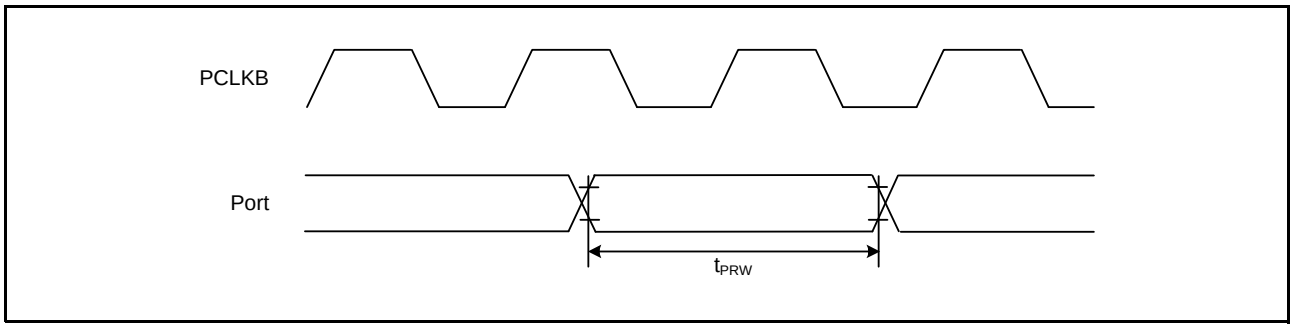


**Figure 5.33 I/O Port Input Timing**

### Table 5.29 GPT Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| GPT | Input capture input pulse width | Single-edge setting | $t_{GTICW}$ | 3 | — | $t_{PAcyc}$ | Figure 5.41 |
| | | Both-edge setting | | 5 | — | | |
| | External trigger input pulse width | Single-edge setting | $t_{OTETW}$ | 1.5 | — | $t_{PAcyc}$ | Figure 5.42 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PAcyc}$: PCLKA cycle

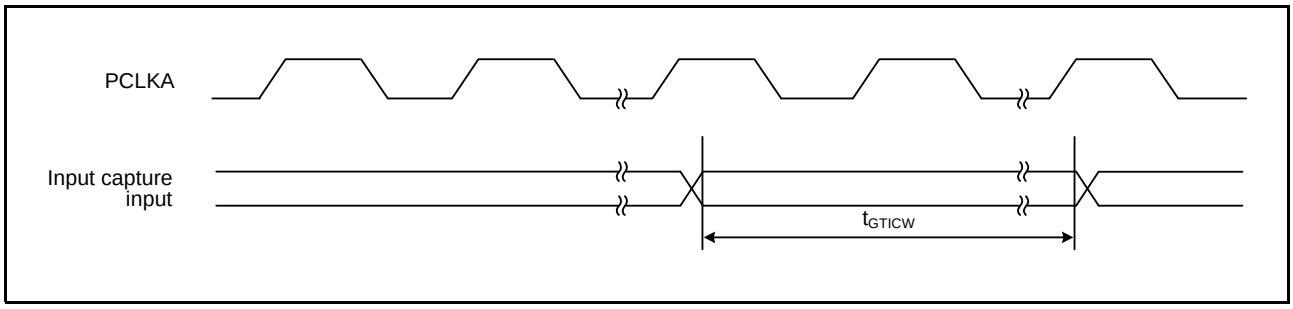


**Figure 5.41 GPT Input Capture Input Timing**

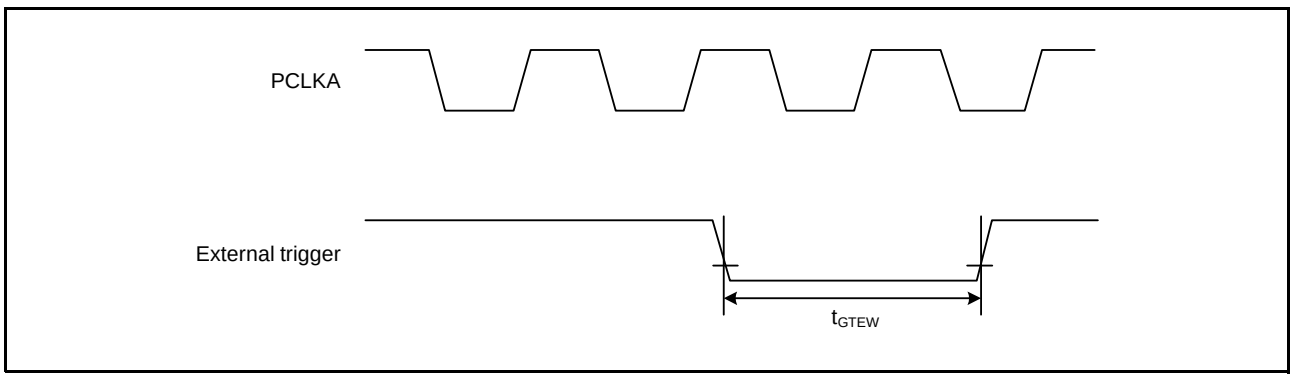


**Figure 5.42 GPT External Trigger Input Timing**

**Table 5.43 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 3.0 to 3.6 V, 3.0 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high level voltage | $V_{IH}$ | 2.0 | — | — | V | |
| | Input low level voltage | $V_{IL}$ | — | — | 0.8 | V | |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | — | — | V | \| DP – DM \| |
| | Differential common mode range | $V_{CM}$ | 0.8 | — | 2.5 | V | |
| Output characteristics | Output high level voltage | $V_{OH}$ | 2.8 | — | 3.6 | V | $I_{OH}$ = –200 µA |
| | Output low level voltage | $V_{OL}$ | 0.0 | — | 0.3 | V | $I_{OL}$ = 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | — | 2.0 | V | Figure 5.77 |
| | Rise time | $t_{FR}$ | 4 | — | 20 | ns | |
| | Fall time | $t_{FF}$ | 4 | — | 20 | ns | |
| | Rise/fall time ratio | $t_{FR}$ / $t_{FF}$ | 90 | — | 111.11 | % | $t_{FR}$/ $t_{FF}$ |
| | Output resistance | $Z_{DRV}$ | 28 | — | 44 | Ω | USBb: Rs = 27 Ω included |
| | | | 40.5 | — | 49.5 | Ω | USBA: Rs not necessary (PHYSET.REPSEL[1:0] = 01b and PHYSET.HSEB = 0) |
| Pull-up and pull-down characteristics | DP pull-up resistance (when the function controller function is selected) | $R_{pu}$ | 0.900 | — | 1.575 | kΩ | Idle state |
| | | | 1.425 | — | 3.090 | kΩ | At transmission and reception |
| | DP/DM pull-down resistance (when the host controller function is selected) | $R_{pd}$ | 14.25 | — | 24.80 | kΩ | |

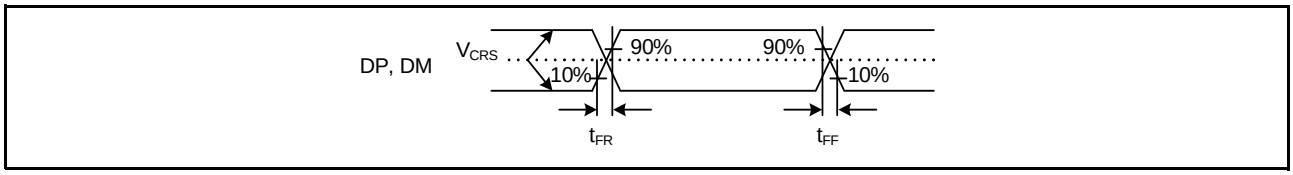


**Figure 5.77 DP and DM Output Timing (Full-Speed)**

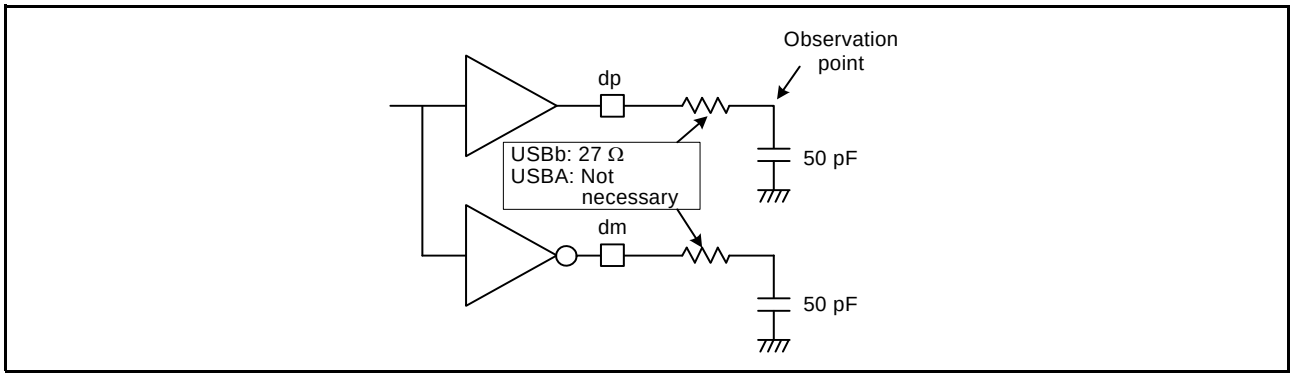


**Figure 5.78 Test Circuit (Full-Speed)**

| REVISION HISTORY | RX71M Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Jan 15, 2015 | — | First edition, issued |