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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | RXv2 |
| Core Size | 32-Bit Single-Core |
| Speed | 240MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 127 |
| Program Memory Size | 2.5MB (2.5M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x12b, 21x12b; D/A 2x12 |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-LFQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mgcdfc-v0 |

## 1.4 Pin Functions

Table 1.4 lists the pin functions.

**Table 1.4 Pin Functions (1/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Digital power supply | VCC | Input | Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VCL | Input | Connect this pin to VSS via a 0.22-μF capacitor. The capacitor should be placed close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | VBATT | Input | Backup power pin |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| | SDCLK | Output | Outputs the SDRAM-dedicated clock. |
| | XCOUT | Output | Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCIN | Input | |
| Clock frequency accuracy measurement | CACREF | Input | Reference clock input pin for the clock frequency accuracy measurement circuit |
| Operating mode control | MD | Input | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation. |
| | UB | Input | USB boot mode or user boot mode enable pin |
| | UPSEL | Input | Selects the power supply method in USB boot mode.<br>The low level selects self-power mode and the high level selects bus power mode. |
| System control | RES# | Input | Reset signal input pin. This LSI enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| | BSCANP | Input | Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low. |
| On-chip emulator | FINED | I/O | Fine interface pin |
| | TRST# | Input | On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. |
| | TRSYNC | Output | This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. |
| | TRDATA0 to TRDATA3 | Output | These pins output the trace information. |
| Address bus | A0 to A23 | Output | Output pins for the address |
| Data bus | D0 to D31 | I/O | Input and output pins for the bidirectional data bus |
| Multiplexed bus | A0/D0 to A15/D15 | I/O | Address/data multiplexed bus |

**Table 1.4 Pin Functions (6/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| USB 2.0 host/function module | VCC_USB, VCC_USBA | Input | Power supply pins |
| | VSS_USB, VSS1_USBA, VSS2_USBA | Input | Ground pins |
| | AVCC_USBA | Input | USBA analog power supply pin |
| | AVSS_USBA | Input | USBA analog ground pin. Short this pin with the PVSS_USBA pin. |
| | PVSS_USBA | Input | USBA PLL circuit ground pin. Short this pin with the AVSS_USBA pin. |
| | USBA_RREF | I/O | USBA reference current supply pin. Connect 2.2 KΩ (1%) to the AVSS_USBA pin. |
| | USB0_DP, USBA_DP | I/O | Input or output USB transceiver D+ data. |
| | USB0_DM, USBA_DM | I/O | Input or output USB transceiver D- data. |
| | USB0_EXICEN, USBA_EXICEN | Output | Connect to the OTG power IC. |
| | USB0_ID, USBA_ID | Input | Connect to the OTG power IC. |
| | USB0_VBUSEN USBA_VBUSEN | Output | USB VBUS power enable pins |
| | USB0_OVRCURA/ USB0_OVRCURB, USBA_OVRCURA/ USBA_OVRCURB | Input | USB overcurrent pins |
| | USB0_VBUS, USBA_VBUS | Input | USB cable connection/disconnection detection input pins |
| CAN module | CRX0, CRX1-DS, CRX2 | Input | Input pins |
| | CTX0 to CTX2 | Output | Output pins |
| Serial peripheral interface | RSPCKA-A/RSPCKA-B/ RSPCKB-A/RSPCKB-B | I/O | Clock input/output pin |
| | MOSIA-A/MOSIA-B/ MOSIB-A/MOSIB-B | I/O | Inputs or outputs data output from the master |
| | MISOA-A/MISOA-B/ MISOB-A/MISOB-B | I/O | Inputs or outputs data output from the slave |
| | SSLA0-A/SSLA0-B/ SSLB0-A/SSLB0-B | I/O | Input or output pin for slave selection |
| | SSLA1-A/SSLA1-B/ SSLB1-A/SSLB1-B to SSLA3-A/SSLA3-B/ SSLB3-A/SSLB3-B | Output | Output pin for slave selection |
| Quad serial peripheral interface | QSPCLK-A/-B | Output | QSPI clock output pin |
| | QSSL-A/-B | Output | QSPI slave output pin |
| | QMO-A/-B, QIO0-A/-B | I/O | Master transmit data/data 0 |
| | QMI-A/-B, QIO1-A/-B | I/O | Master input data/data 1 |
| | QIO2-A/-B, QIO3-A/-B | I/O | Data 2, data 3 |
| Serial sound interface | SSISCK0, SSISCK1 | I/O | SSI serial bit clock pins |
| | SSIWS0, SSIWS1 | I/O | Word select pins |
| | SSITXD0, SSITXD1 | Output | Serial data output pins |
| | SSIRXD0, SSIRXD1 | Input | Serial data input pins |
| | SSIDATA0, SSIDATA1 | I/O | Serial data input/output pins |
| | AUDIO_MCLK | Input | Master clock pin for audio |

**Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (3/7)**

| Pin Number 176-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 56 | | | | | USB0_DP | | | |
| 57 | VSS_USB | | | | | | | |
| 58 | AVCC_ USBA | | | | | | | |
| 59 | USBA_ RREF | | | | | | | |
| 60 | AVSS_ USBA | | | | | | | |
| 61 | PVSS_ USBA | | | | | | | |
| 62 | VSS2_ USBA | | | | | | | |
| 63 | | | | | USBA_DM | | | |
| 64 | | | | | USBA_DP | | | |
| 65 | VSS1_ USBA | | | | | | | |
| 66 | VCC_ USBA | | | | | | | |
| 67 | | P11 | | MTIC5V/TMCI3 | SCK2/USBA_VBUS/ USBA_VBUSEN | | IRQ1 | |
| 68 | | P10 | ALE | MTIC5W/TMRI3 | USBA_OVRCURA | | IRQ0 | |
| 69 | | P53*1 | BCLK | | | | | |
| 70 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | |
| 71 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2-A | | | |
| 72 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | |
| 73 | VSS | | | | | | | |
| 74 | | P83 | EDACK1 | MTIOC4C/ GTIOC0A-D | CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10 | | | |
| 75 | VCC | | | | | | | |
| 76 | UB | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF | TXD8/MISOA-A/ ET0_COL | MMC_D7-A | IRQ14 | |
| 77 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30 | RXD8/MOSIA-A/ ET0_ETXD3 | MMC_D6-A | IRQ13 | |
| 78 | | PC5 | A21/CS2#/ WAIT# | MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29 | SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2 | MMC_D5-A | | |
| 79 | | P82 | EDREQ1 | MTIOC4A/ GTIOC2A-D/PO28 | TXD10/ET0_ETXD1/ RMII0_TXD1 | MMC_D4-A | | |
| 80 | | P81 | EDACK0 | MTIOC3D/ GTIOC0B-D/PO27 | RXD10/ET0_ETXD0/ RMII0_TXD0 | MMC_D3-A/ SDHI_CD-A/ QIO3-A | | |
| 81 | | P80 | EDREQ0 | MTIOC3B/PO26 | SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN | MMC_D2-A/ SDHI_WP-A/ QIO2-A | | |
| 82 | | PC4 | A20/CS3# | MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0# | SCK5/CTS8#/SSLA0- A/ET0_TX_CLK | MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A | | |
| 83 | | PC3 | A19 | MTIOC4D/ GTIOC1B-D/TCLKB/ PO24 | TXD5/SMOSI5/ SSDA5/ ET0_TX_ER | MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A | | |

**Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (2/5)**

| Pin Number 144-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 36 | | P21 | | MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0 | PIXD5 | IRQ9 | |
| 37 | | P20 | | MTIOC1A/TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0 | PIXD4 | IRQ8 | |
| 38 | | P17 | | MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8# | SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0 | PIXD3 | IRQ7 | ADTRG1# |
| 39 | | P87 | | MTIOC4C/ GTIOC1B-B/TIOCA2 | TXD10 | PIXD2 | | |
| 40 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT | TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | | IRQ6 | ADTRG0# |
| 41 | | P86 | | MTIOC4D/ GTIOC2B-B/TIOCA0 | RXD10 | PIXD1 | | |
| 42 | | P15 | | MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13 | RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1 | PIXD0 | IRQ5 | |
| 43 | | P14 | | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15 | CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA | | IRQ4 | |
| 44 | | P13 | | MTIOC0B/TIOCA5/ TMO3/PO13 | TXD2/SMOSI2/ SSDA2/SDA0[FM+] | | IRQ3 | ADTRG1# |
| 45 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/SCL0[FM+] | | IRQ2 | |
| 46 | VCC_USB | | | | | | | |
| 47 | | | | | USB0_DM | | | |
| 48 | | | | | USB0_DP | | | |
| 49 | VSS_USB | | | | | | | |
| 50 | | P56 | EDACK1 | MTIOC3C/TIOCA1 | | | | |
| 51 | TRDATA3 | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | CRX1/ET0_EXOUT | | IRQ10 | |
| 52 | TRDATA2 | P54 | ALE/EDACK0 | MTIOC4B/TMCI1 | CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA | | | |
| 53 | | P53 | BCLK | | | | | |
| 54 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | |
| 55 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2-A | | | |
| 56 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | |
| 57 | VSS | | | | | | | |
| 58 | TRCLK | P83 | EDACK1 | MTIOC4C/ GTIOC0A-D | CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10 | | | |
| 59 | VCC | | | | | | | |
| 60 | UB | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF | TXD8/MISOA-A/ ET0_COL | MMC_D7-A | IRQ14 | |
| 61 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30 | RXD8/MOSIA-A/ ET0_ETXD3 | MMC_D6-A | IRQ13 | |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/4)**

| Pin Number 100-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| F5 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/SCL0[FM+] | | IRQ2 | |
| F6 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11# | SCK6/ET0_RX_ER/ RMII0_RX_ER | | | |
| F7 | | PB2 | A10 | TIOCC3/TCLKC/ PO26 | CTS6#/RTS6#SS6#/ ET0_RX_CLK/ REF50CK0 | | | |
| F8 | | PB0 | A8 | MTIC5W/TIOCA3/ PO24 | RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1 | | IRQ12 | |
| F9 | | PA7 | A7 | TIOCB2/PO23 | MISOA-B/ET0_WOL | | | |
| F10 | VSS | | | | | | | |
| G1 | | P33 | EDREQ1 | MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11# | RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0 | | IRQ3-DS | |
| G2 | TMS | P31 | | MTIOC4D/TMCI2/ PO9/RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0-A | | IRQ1-DS | |
| G3 | TDI | P30 | | MTIOC4B/TMRI3/ PO8/RTCIC0/POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | IRQ0-DS | |
| G4 | TCK | P27 | CS7# | MTIOC2B/TMCI3/PO7 | SCK1/RSPCKB-A | | | |
| G5 | | P53 | BCLK | | | | | |
| G6 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | |
| G7 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4# | SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0 | | | |
| G8 | | PB4 | A12 | TIOCA4/PO28 | CTS9#/ET0_TX_EN/ RMII0_TXD_EN | | | |
| G9 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0 | | IRQ4-DS | |
| G10 | VCC | | | | | | | |
| H1 | TDO | P26 | CS6# | MTIOC2A/TMO1/PO6 | TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A | | | |
| H2 | | P25 | CS5#/ EDACK1 | MTIOC4C/MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3/SSIDATA1 | | | ADTRG0# |
| H3 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT | TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | | IRQ6 | ADTRG0# |
| H4 | | P15 | | MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13 | RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1 | | IRQ5 | |
| H5 | | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | CRX1/ET0_EXOUT | | IRQ10 | |
| H6 | | P54 | ALE/ EDACK0 | MTIOC4B/TMCI1 | CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA | | | |
| H7 | UB | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF | TXD8/MISOA-A/ ET0_COL | | IRQ14 | |

**Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (1/4)**

| Pin Number 100-Pin LQFP | Power Supply Clock System Contro | I/O Port | Bus EXDMAC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 1 | AVCC1 | | | | | | | |
| 2 | EMLE | | | | | | | |
| 3 | AVSS1 | | | | | | | |
| 4 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0# | | | |
| 5 | VCL | | | | | | | |
| 6 | VBATT | | | | | | | |
| 7 | MD/FINED | | | | | | | |
| 8 | XCIN | | | | | | | |
| 9 | XCOUT | | | | | | | |
| 10 | RES# | | | | | | | |
| 11 | XTAL | P37 | | | | | | |
| 12 | VSS | | | | | | | |
| 13 | EXTAL | P36 | | | | | | |
| 14 | VCC | | | | | | | |
| 15 | UPSEL | P35 | | | | | NMI | |
| 16 | TRST# | P34 | | MTIOC0A/TMCI3/ PO12/POE10# | SCK6/SCK0/ ET0_LINKSTA | | IRQ4 | |
| 17 | | P33 | EDREQ1 | MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11# | RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0 | | IRQ3-DS | |
| 18 | | P32 | | MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10# | TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN | | IRQ2-DS | |
| 19 | TMS | P31 | | MTIOC4D/TMCI2/ PO9/RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0-A | | IRQ1-DS | |
| 20 | TDI | P30 | | MTIOC4B/TMRI3/ PO8/RTCIC0/POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | IRQ0-DS | |
| 21 | TCK | P27 | CS7# | MTIOC2B/TMCI3/PO7 | SCK1/RSPCKB-A | | | |
| 22 | TDO | P26 | CS6# | MTIOC2A/TMO1/PO6 | TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A | | | |
| 23 | | P25 | CS5#/ EDACK1 | MTIOC4C/MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3/SSIDATA1 | | | ADTRG0# |
| 24 | | P24 | CS4#/ EDREQ1 | MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4 | SCK3/ USB0_VBUSEN/ SSISCK1 | | | |
| 25 | | P23 | EDACK0 | MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3 | TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0 | | | |
| 26 | | P22 | EDREQ0 | MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2 | SCK0/ USB0_OVRCURB/ AUDIO_MCLK | | | |
| 27 | | P21 | | MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0 | | IRQ9 | |
| 28 | | P20 | | MTIOC1A/TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0 | | IRQ8 | |
| 29 | | P17 | | MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8# | SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0 | | IRQ7 | ADTRG1# |

**Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (3/4)**

| Pin Number 100-Pin LQFP | Power Supply Clock System Contro | I/O Port | Bus EXDMAC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 56 | | PB4 | A12 | TIOCA4/PO28 | CTS9#/ET0_TX_EN/ RMII0_TXD_EN | | | |
| 57 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11# | SCK6/ET0_RX_ER/ RMII0_RX_ER | | | |
| 58 | | PB2 | A10 | TIOCC3/TCLKC/ PO26 | CTS6#/RTS6#SS6#/ ET0_RX_CLK/ REF50CK0 | | | |
| 59 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0 | | IRQ4-DS | |
| 60 | VCC | | | | | | | |
| 61 | | PB0 | A8 | MTIC5W/TIOCA3/ PO24 | RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1 | | IRQ12 | |
| 62 | VSS | | | | | | | |
| 63 | | PA7 | A7 | TIOCB2/PO23 | MISOA-B/ET0_WOL | | | |
| 64 | | PA6 | A6 | MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10# | CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT | | | |
| 65 | | PA5 | A5 | MTIOC6B/TIOCB1/ GTIOC0A-C/PO21 | RSPCKA-B/ ET0_LINKSTA | | | |
| 66 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC | | IRQ5-DS | |
| 67 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19 | RXD5/SMISO5/ SSCL5/ET0_MDIO | | IRQ6-DS | |
| 68 | | PA2 | A2 | MTIOC7A/ GTIOC1A-C/PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | | |
| 69 | | PA1 | A1 | MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17 | SCK5/SSLA2-B/ ET0_WOL | | IRQ11 | |
| 70 | | PA0 | A0/BC0# | MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16 | SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN | | | |
| 71 | | PE7 | D15[A15/D15] | MTIOC6A/ GTIOC3A-E/TOC1 | MISOB-B | MMC_RES#-B/ SDHI_WP-B | IRQ7 | AN105 |
| 72 | | PE6 | D14[A14/D14] | TIOC6C/GTIOC3B-E/ TIC1 | MOSIB-B | MMC_CD-B/ SDHI_CD-B | IRQ6 | AN104 |
| 73 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B/ GTIOC0A-A | ET0_RX_CLK/ REF50CK0/ RSPCKB-B | | IRQ5 | AN103 |
| 74 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28 | ET0_ERXD2/SSLB0-B | | | AN102 |
| 75 | | PE3 | D11[A11/D11] | MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3 | CTS12#/RTS12#/ SS12#/ET0_ERXD3 | MMC_D7-B | | AN101 |
| 76 | | PE2 | D10[A10/D10] | MTIOC4A/ GTIOC0B-A/PO23/ TIC3 | RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B | MMC_D6-B | IRQ7-DS | AN100 |
| 77 | | PE1 | D9[A9/D9] | MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | | ANEX1 |
| 78 | | PE0 | D8[A8/D8] | MTIOC3D/ GTIOC2B-A | SCK12/SSLB1-B | MMC_D4-B | | ANEX0 |
| 79 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | MMC_D1-B/ SDHI_D1-B/ QIO1-B/ QMI-B | IRQ7 | AN107 |

## 2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.

Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

### (3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to section Table 4.1, List of I/O Registers (Address Order). The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown inTable 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown inTable 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

### (4) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

### (5) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

**Table 4.1 List of I/O Registers (Address Order) (12 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 79DCh | ICU | Software Configurable Interrupt A Select Register 220 | SLIAR220 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79DDh | ICU | Software Configurable Interrupt A Select Register 221 | SLIAR221 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79DEh | ICU | Software Configurable Interrupt A Select Register 222 | SLIAR222 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79DFh | ICU | Software Configurable Interrupt A Select Register 223 | SLIAR223 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E0h | ICU | Software Configurable Interrupt A Select Register 224 | SLIAR224 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E1h | ICU | Software Configurable Interrupt A Select Register 225 | SLIAR225 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E2h | ICU | Software Configurable Interrupt A Select Register 226 | SLIAR226 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E3h | ICU | Software Configurable Interrupt A Select Register 227 | SLIAR227 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E4h | ICU | Software Configurable Interrupt A Select Register 228 | SLIAR228 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E5h | ICU | Software Configurable Interrupt A Select Register 229 | SLIAR229 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E6h | ICU | Software Configurable Interrupt A Select Register 230 | SLIAR230 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E7h | ICU | Software Configurable Interrupt A Select Register 231 | SLIAR231 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E8h | ICU | Software Configurable Interrupt A Select Register 232 | SLIAR232 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79E9h | ICU | Software Configurable Interrupt A Select Register 233 | SLIAR233 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79EAh | ICU | Software Configurable Interrupt A Select Register 234 | SLIAR234 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79EBh | ICU | Software Configurable Interrupt A Select Register 235 | SLIAR235 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79ECh | ICU | Software Configurable Interrupt A Select Register 236 | SLIAR236 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79EDh | ICU | Software Configurable Interrupt A Select Register 237 | SLIAR237 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79EEh | ICU | Software Configurable Interrupt A Select Register 238 | SLIAR238 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79EFh | ICU | Software Configurable Interrupt A Select Register 239 | SLIAR239 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F0h | ICU | Software Configurable Interrupt A Select Register 240 | SLIAR240 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F1h | ICU | Software Configurable Interrupt A Select Register 241 | SLIAR241 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F2h | ICU | Software Configurable Interrupt A Select Register 242 | SLIAR242 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F3h | ICU | Software Configurable Interrupt A Select Register 243 | SLIAR243 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F4h | ICU | Software Configurable Interrupt A Select Register 244 | SLIAR244 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F5h | ICU | Software Configurable Interrupt A Select Register 245 | SLIAR245 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F6h | ICU | Software Configurable Interrupt A Select Register 246 | SLIAR246 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F7h | ICU | Software Configurable Interrupt A Select Register 247 | SLIAR247 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F8h | ICU | Software Configurable Interrupt A Select Register 248 | SLIAR248 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79F9h | ICU | Software Configurable Interrupt A Select Register 249 | SLIAR249 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79FAh | ICU | Software Configurable Interrupt A Select Register 250 | SLIAR250 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79FBh | ICU | Software Configurable Interrupt A Select Register 251 | SLIAR251 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79FCh | ICU | Software Configurable Interrupt A Select Register 252 | SLIAR252 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79FDh | ICU | Software Configurable Interrupt A Select Register 253 | SLIAR253 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |
| 0008 79FEh | ICU | Software Configurable Interrupt A Select Register 254 | SLIAR254 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUA |

**Table 5.9 Operating Frequency (Low-Speed Operating Mode 2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | | f | 32 | — | 264 | kHz |
| | Peripheral module clock (PCLKA) | | | — | — | 264 | |
| | Peripheral module clock (PCLKB) | | | — | — | 264 | |
| | Peripheral module clock (PCLKC)*1 | | | — | — | 264 | |
| | Peripheral module clock (PCLKD)*1 | | | — | — | 264 | |
| | Flash-IF clock (FCLK) | | | 32 | — | 264 | |
| | External bus clock (BCLK) | Packages with 177 to 144 pins only | | — | — | 264 | |
| | | Package with 100 pins only | | — | — | 264 | |
| | BCLK pin output | Packages with 177 to 144 pins only | | — | — | 264 | |
| | | Package with 100 pins only | | — | — | 264 | |
| | SDRAM clock (SDCLK) | Packages with 177 to 144 pins only | | — | — | 264 | |
| | SDCLK pin output | Packages with 177 to 144 pins only | | — | — | 264 | |

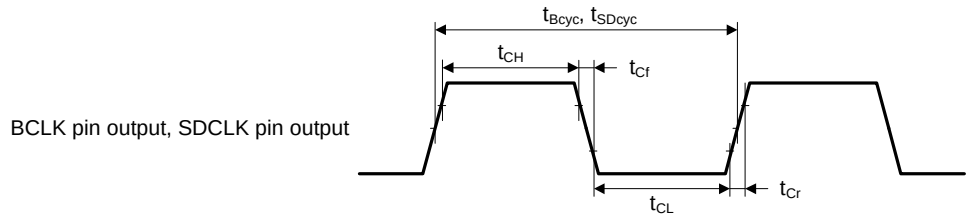
Note 1. The 12-bit A/D converter cannot be used.

## 5.3.2 Clock Timing

**Table 5.11 BCLK Pin Output, SDCLK Pin Output Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| BCLK pin output cycle time | Packages with 177 to 144 pins | $t_{Bcyc}$ | 16.6 | — | — | ns | Figure 5.3 |
| | Packages with 100 pins or less | | 33.2 | — | — | ns | |
| BCLK pin output high pulse width | | $t_{CH}$ | 3.3 | — | — | ns | |
| BCLK pin output low pulse width | | $t_{CL}$ | 3.3 | — | — | ns | |
| BCLK pin output rising time | | $t_{Cr}$ | — | — | 5 | ns | |
| BCLK pin output falling time | | $t_{Cf}$ | — | — | 5 | ns | |
| SDCLK pin output cycle time | Packages with 177 to 144 pins | $t_{Bcyc}$ | 16.6 | — | — | ns | |
| SDCLK pin output high pulse width | | $t_{CH}$ | 3.3 | — | — | ns | |
| SDCLK pin output low pulse width | | $t_{CL}$ | 3.3 | — | — | ns | |
| SDCLK pin output rising time | | $t_{Cr}$ | — | — | 5 | ns | |
| SDCLK pin output falling time | | $t_{Cf}$ | — | — | 5 | ns | |




Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, C = 30 pF

**Figure 5.3 BCLK Pin and SDCLK Pin Output Timing**

## 5.3.4 Control Signal Timing

**Table 5.20 Control Signal Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PLCKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | Symbol | Min.*1 | Typ. | Max. | Unit | Test Conditions*1 |
|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | $t_{PBcyc}$ × 2 ≤ 200 ns, Figure 5.14 |
| | | $t_{PBcyc}$ × 2 | — | — | ns | $t_{PBcyc}$ × 2 > 200 ns, Figure 5.14 |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | $t_{PBcyc}$ × 2 ≤ 200 ns, Figure 5.15 |
| | | $t_{PBcyc}$ × 2 | — | — | ns | $t_{PBcyc}$ × 2 > 200 ns, Figure 5.15 |

Note 1. $t_{PBcyc}$: PCLKB cycle

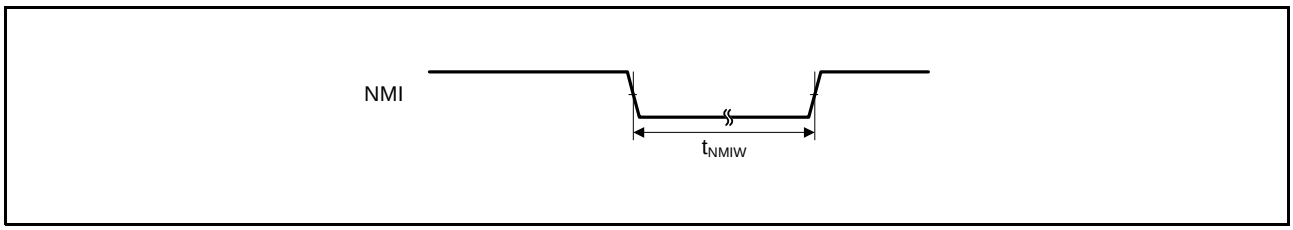



**Figure 5.14 NMI Interrupt Input Timing**

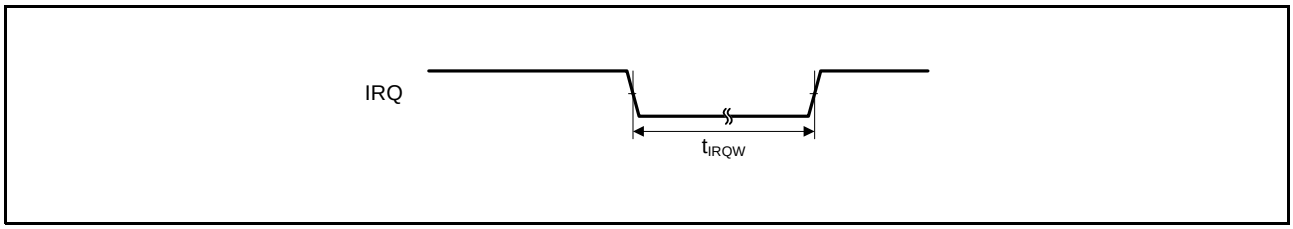



**Figure 5.15 IRQ Interrupt Input Timing**

### Table 5.27 MTU3 Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| MTU3 | Input capture input pulse width | Single-edge setting | $t_{MTICW}$ | 1.5 | — | $t_{PAcyc}$ | Figure 5.38 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{MTCKWH}$, $t_{MTCKWL}$ | 1.5 | — | $t_{PAcyc}$ | Figure 5.39 |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |

Note 1. $t_{PAcyc}$: PCLKA cycle

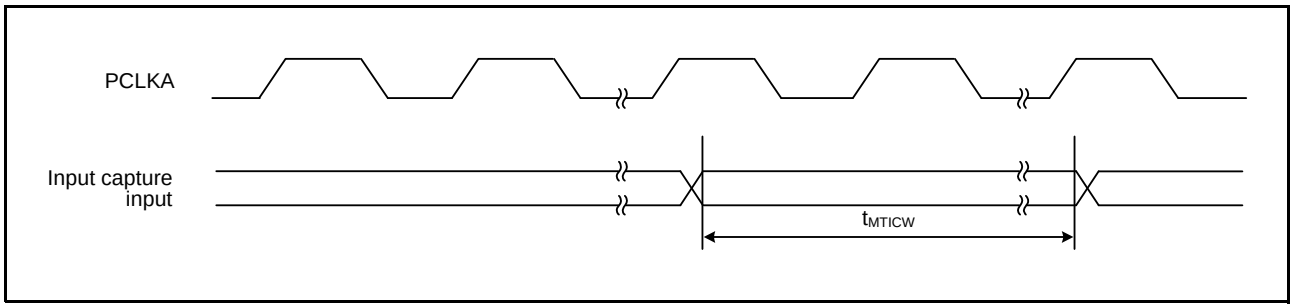



**Figure 5.38 MTU3 Input Capture Input Timing**

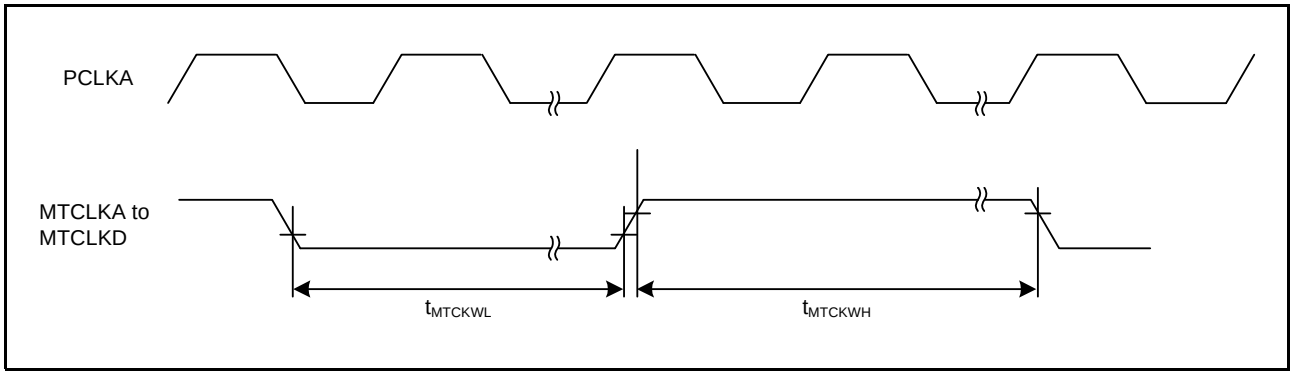



**Figure 5.39 MTU3 Clock Input Timing**

### Table 5.30 A/D Converter Trigger Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| A/D converter | A/D converter trigger input pulse width | $t_{TRGW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.43 |

Note 1. $t_{PBcyc}$: PCLKB cycle

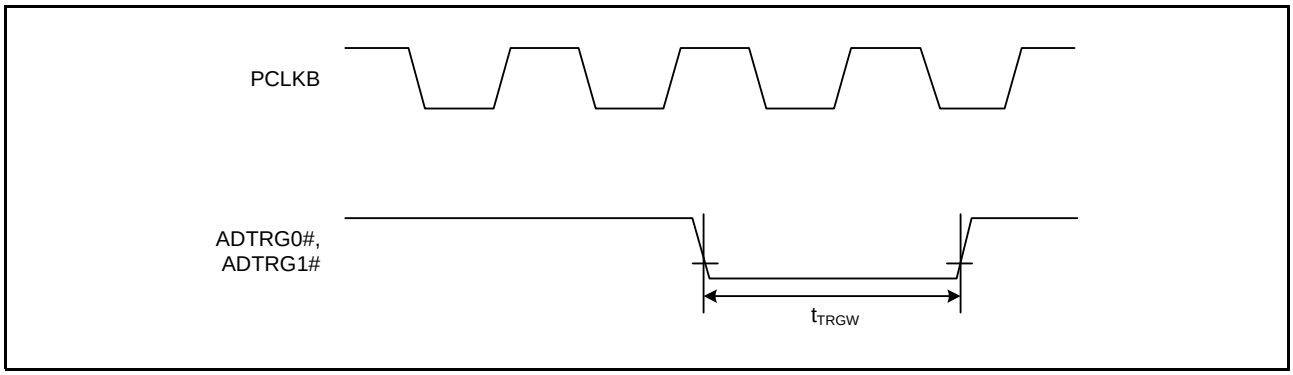



**Figure 5.43 A/D Converter Trigger Input Timing**

### Table 5.31 CAC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item*1, *2 | | | Symbol | Min.*1 | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| CAC | CACREF input pulse width | $t_{PBcyc} \le t_{cac}$ | $t_{CACREF}$ | $4.5t_{cac}$ + $3t_{PBcyc}$ | — | ns | |
| | | $t_{PBcyc} > t_{cac}$ | | $5t_{cac}$ + $6.5t_{PBcyc}$ | — | | |

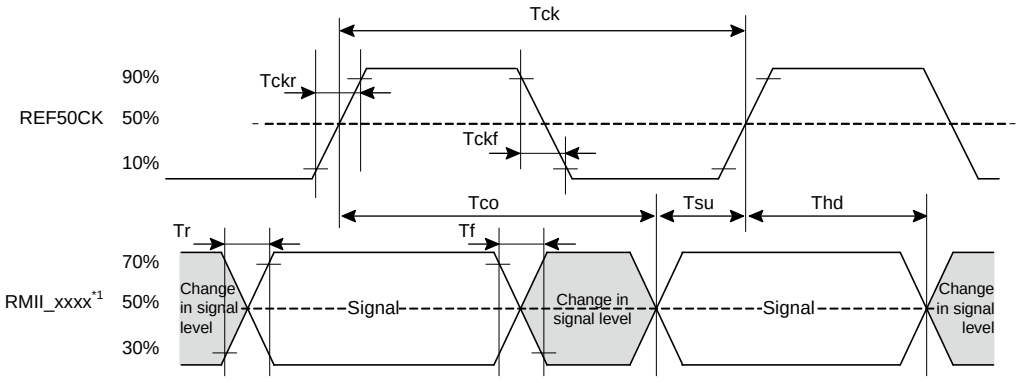
Note 1. $t_{PBcyc}$: PCLKB cycle
Note 2. $t_{CAC}$: CAC count clock source cycle

### Table 5.40 ETHERC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| ETHERC (RMII) | REF50CK cycle time | $T_{ck}$ | 20 | — | ns | Figure 5.62 to Figure 5.64 |
| | REF50CK frequency Typ. 50 MHz | — | — | 50 + 100ppm | MHz | |
| | REF50CK duty | — | 35 | 65 | % | |
| | REF50CK rise/fall time | $T_{ckr/ckf}$ | 0.5 | 3.5 | ns | |
| | RMII_xxxx*1 output delay time | $T_{co}$ | 2.5 | 15.0 | ns | |
| | RMII_xxxx*2 setup time | $T_{su}$ | 3 | — | ns | |
| | RMII_xxxx*2 hold time | $T_{hd}$ | 1 | — | ns | |
| | RMII_xxxx*1, *2 rise/fall time | $T_r/T_f$ | 0.5 | 5 | ns | |
| | ET_WOL output delay time | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 5.66 |
| ETHERC (MII) | ET_TX_CLK cycle time | $t_{Tcyc}$ | 40 | — | ns | — |
| | ET_TX_EN output delay time | $t_{TENd}$ | 1 | 20 | ns | Figure 5.67 |
| | ET_ETXD0 to ET_ETXD3 output delay time | $t_{MTDd}$ | 1 | 20 | ns | |
| | ET_CRS setup time | $t_{CRSs}$ | 10 | — | ns | |
| | ET_CRS hold time | $t_{CRSh}$ | 10 | — | ns | |
| | ET_COL setup time | $t_{COLs}$ | 10 | — | ns | Figure 5.68 |
| | ET_COL hold time | $t_{COLh}$ | 10 | — | ns | |
| | ET_RX_CLK cycle time | $t_{TRcyc}$ | 40 | — | ns | — |
| | ET_RX_DV setup time | $t_{RDVs}$ | 10 | — | ns | Figure 5.69 |
| | ET_RX_DV hold time | $t_{RDVh}$ | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 setup time | $t_{MRDs}$ | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 hold time | $t_{MRDh}$ | 10 | — | ns | |
| | ET_RX_ER setup time | $t_{RERs}$ | 10 | — | ns | Figure 5.70 |
| | ET_RX_ER hold time | $t_{RESh}$ | 10 | — | ns | |
| | ET_WOL output delay time | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 5.71 |

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER




Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0, RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

**Figure 5.62 Timing with the REF50CK and RMII Signals**

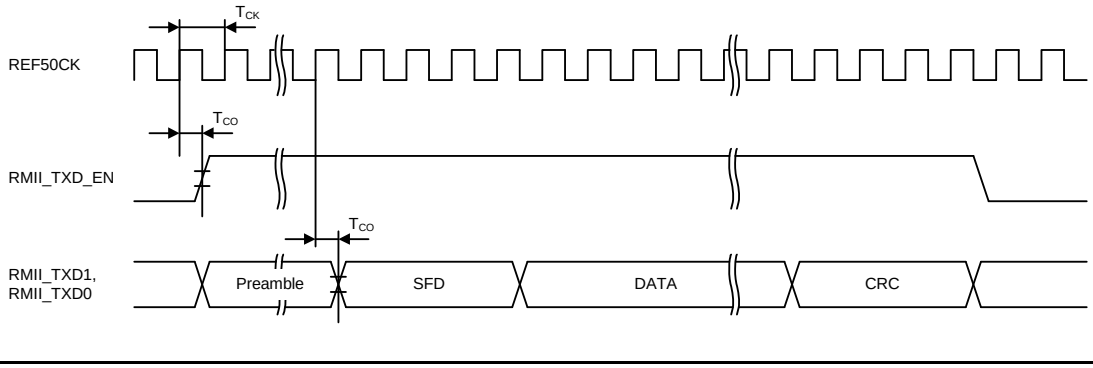



**Figure 5.63 RMII Transmission Timing**

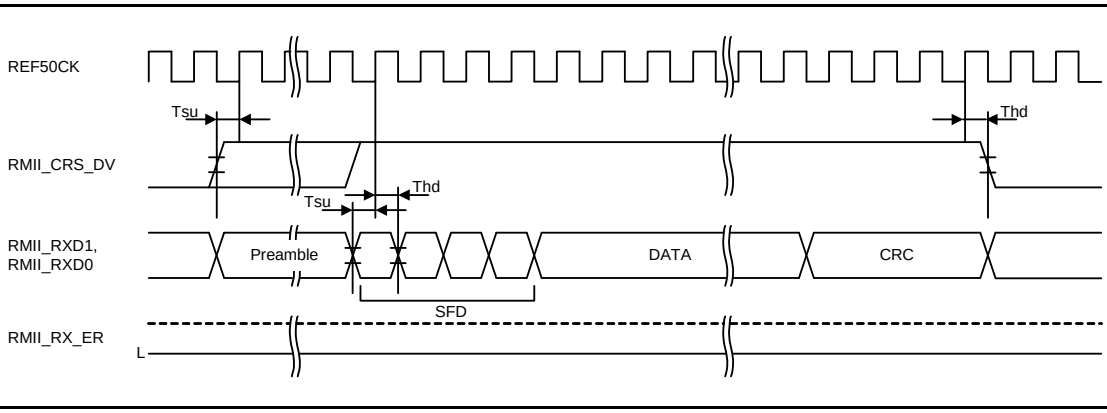



**Figure 5.64 RMII Reception Timing (Normal Operation)**

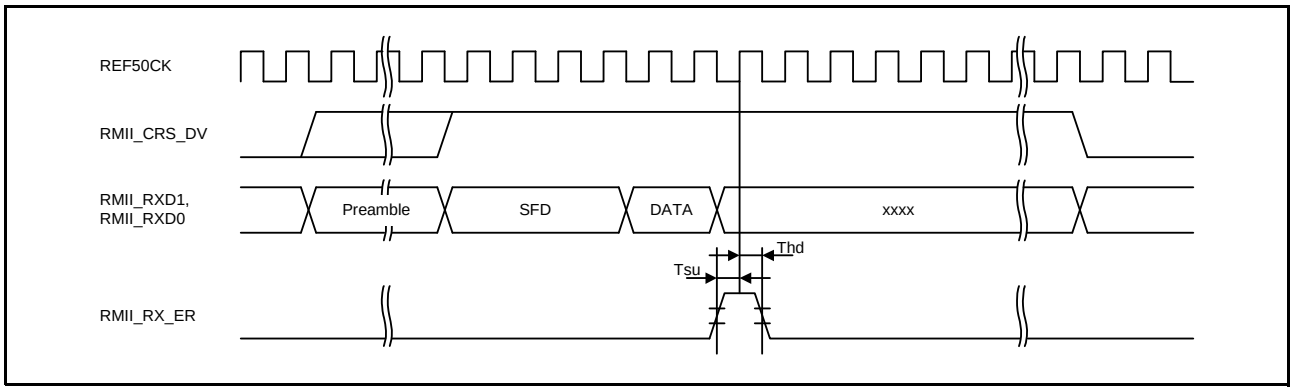



**Figure 5.65 RMII Reception Timing (Error Occurrence)**

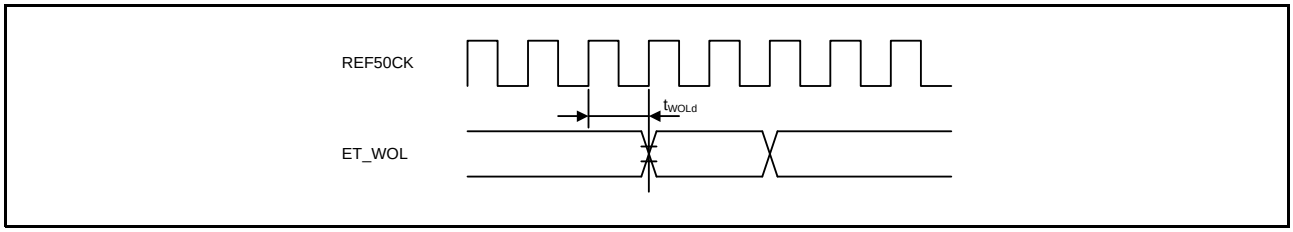



**Figure 5.66 WOL Output Timing (RMII)**

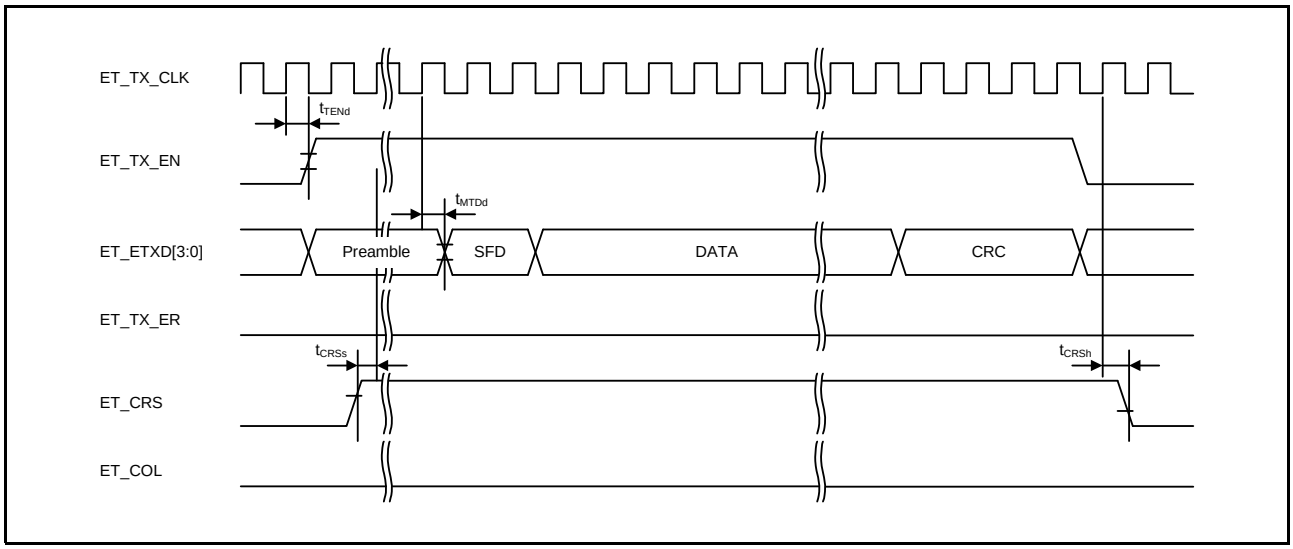



**Figure 5.67 MII Transmission Timing (Normal Operation)**

## 5.6 D/A Conversion Characteristics

**Table 5.49 D/A Conversion Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V,
2.7 ≤ VREFH0 ≤ AVCC0, VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resolution | | 12 | 12 | 12 | Bit | |
| Without AMP output | Absolute accuracy | — | — | ±6.0 | LSB | 2-MΩ resistive load<br>10-bit conversion |
| | DNL differential nonlinearity error | — | ±1.0 | ±2.0 | LSB | 2-MΩ resistive load |
| | RO output resistance | — | 7.5 | — | kΩ | |
| | Conversion time | — | — | 3.0 | µs | 20-pF capacitive load |
| With AMP output | Resistive load | 5 | — | — | kΩ | |
| | Capacitive load | — | | 50 | pF | |
| | Output voltage range | 0.2 | — | AVCC1 – 0.2 | V | |
| | DNL differential nonlinearity error | — | ±1.0 | ±2.0 | LSB | |
| | INL integral nonlinearity error | — | ±2.0 | ±4.0 | LSB | |
| | Conversion time | — | — | 4.0 | µs | |

## 5.7 Temperature Sensor Characteristics

**Table 5.50 Temperature Sensor Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Relative accuracy | — | ±1 | — | °C | |
| Temperature slope | — | 4.1 | — | mV/°C | |
| Output voltage (at 25°C) | — | 1.24 | — | V | |
| Temperature sensor start time | — | — | 30 | µs | |
| Sampling time | 4.15 | — | — | µs | ADSSTRT.SST[7:0] = 250 states |

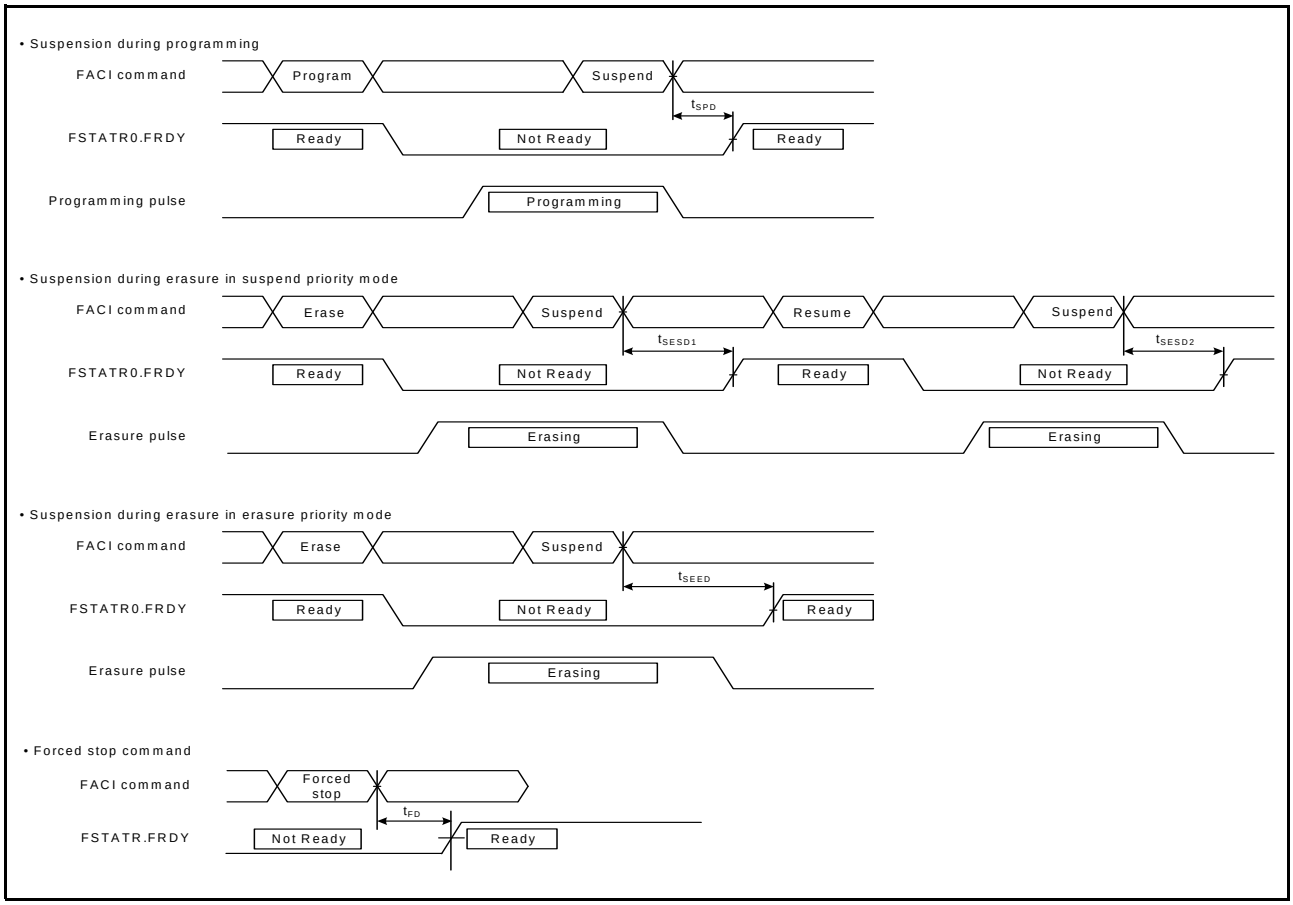



**Figure 5.89 Flash Memory Programming/Erasure Suspension Timing**