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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mgddfb-v0

Table 1.4 Pin Functions (3/8)

Classifications	Pin Name	I/O	Description
General-purpose PWM timer	GTIOC0A-A/GTIOC0A-B/ GTIOC0A-C/GTIOC0A-D/ GTIOC0A-E, GTIOC0B-A/GTIOC0B-B/ GTIOC0B-C/GTIOC0B-D/ GTIOC0B-E	I/O	GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins
	GTIOC1A-A/GTIOC1A-B/ GTIOC1A-C/GTIOC1A-D/ GTIOC1A-E, GTIOC1B-A/GTIOC1B-B/ GTIOC1B-C/GTIOC1B-D/ GTIOC1B-E	I/O	GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins
	GTIOC2A-A/GTIOC2A-B/ GTIOC2A-C/GTIOC2A-D/ GTIOC2A-E, GTIOC2B-A/GTIOC2B-B/ GTIOC2B-C/GTIOC2B-D/ GTIOC2B-E	I/O	GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins
	GTIOC3A-D/GTIOC3A-E, GTIOC3B-D/GTIOC3B-E	I/O	GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins
	GTETRGR-B/GTETRGR-C/ GTETRGR-D	Input	External trigger input pin for GPT0 to GPT3
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter
	TMRI0 to TMRI3	Input	Input pins for the counter reset
Compare match timer W	TIC0 to TIC3	Input	Input pins for CMTW
	TOC0 to TOC3	Output	Output pins for CMTW

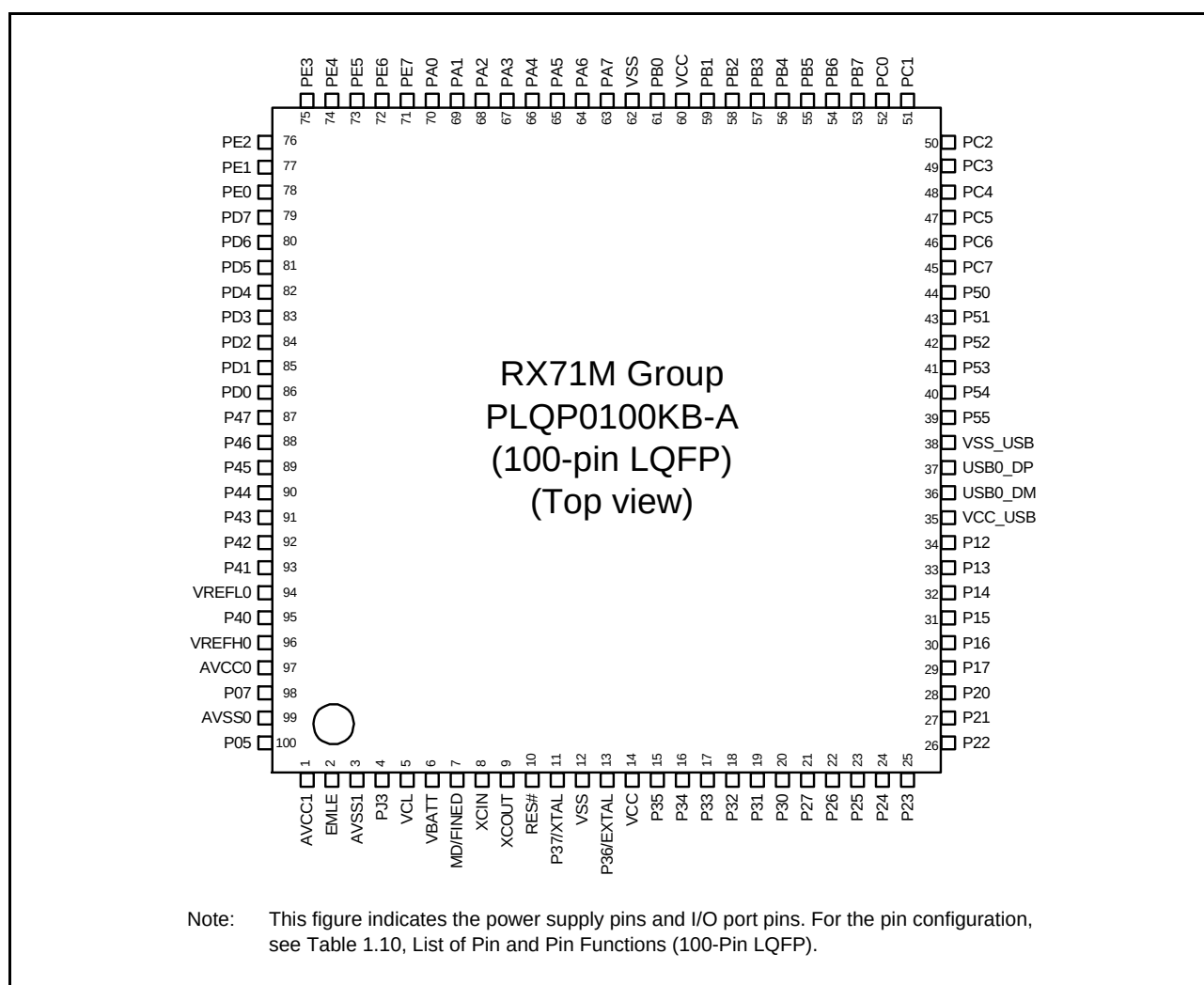
**Figure 1.9 Pin Assignment (100-Pin LQFP)**

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer	Communication	Memory Interface Camera Interface	Interrupt	S12ADC, R12DA
J14		PA7	A7	TIOCB2/PO23	MISOA-B/ ET0_WOL			
J15		PA6	A6	MTIC5V/MTCLKB/ GTETR-G-C/TIOCA2/ TMC13/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
K1		P33	EDREQ1	MTIOC0D/TIOC0D/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOU/RTICIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/ SSCL1			
K4	TCK	PF1			SCK1			
K12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
K13		P71	A18/CS1#		ET0_MDIO			
K14	VCC							
K15		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
L1		P31		MTIOC4D/TMC12/ PO9/RTIC1	CTS1#/RTS1#/ SS1#/ET1_MDC/ SSLB0-A		IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/ PO8/RTIC0/POE8#	RXD1/SMISO1/ SSCL1/ET1_MDIO/ MISOB-A		IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/ SSDA1			
L4		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ SSIDATA1	HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOC03/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
L15		P72	A19/CS2#		ET0_MDC			
M1		P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/ET1_WOL/ RSPCKB-A			
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ ET1_EXOUT/ MOSIB-A			
M3		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
M4		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
F13		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
G1	XTAL	P37						
G2	RES							
G3	MD/FINED							
G4	BSCANP							
G10		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
G11		PA6	A6	MTIC5V/MTCLKB/ GTETR-G-C/TIOCA2/ TMC13/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
G12	VCC							
G13		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
H1	EXTAL	P36						
H2	VCC							
H3	VSS							
H4	UPSEL	P35					NMI	
H10		P72	A19/CS2#		ET0_MDC			
H11		P71	A18/CS1#		ET0_MDIO			
H12		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
H13		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
J1	TRST#	P34		MTIOC0A/TMC13/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
J2		P33	EDREQ1	MTIOC0D/TIOC0D/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
J3		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
J4	TDI	P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS	
J10		PB3	A11	MTIOC0A/MTIOC4A/ TIOC03/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
J11		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
J12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
J13		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
K1	TCK	P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/RSPCKB-A			
K2	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A			
K3	TMS	P31		MTIOC4D/TMC12/ PO9/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0-A		IRQ1-DS	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
M2		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOC0B0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
M3		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
M4		P12		TMC11	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
M5	VCC_USB							
M6	VSS_USB							
M7		P50	WR0#/NR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
M8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMC12/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
M10		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		
M11		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
M12		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
M13	VCC							
N1		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0	PIXD5	IRQ9	
N2		P20		MTIOC1A/TIOC3B/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0	PIXD4	IRQ8	
N3		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
N4		P14		MTIOC3A/MTCLKA/ TIOC3B5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
N5					USB0_DM			
N6					USB0_DP			
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
N8	VSS							
N9	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
N11		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
N12		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
N13		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/4)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMC12/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	
H9		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
H10		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
J1		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1			
J2		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0		IRQ9	
J3		P17		MTIOC3A/MTIOC3B/ MTIOC4B/GTIOC0B- B/TIOCB0/TCLKD/ TMO1/PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0		IRQ7	ADTRG1#
J4		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
J5	VSS_USB							
J6	VCC_USB							
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRQ-D/TMC11/ PO25/POE0#	SCK5/CTS8#/SSLA0- A/ET0_TX_CLK			
J9		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
J10		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
K1		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0			
K2		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK			
K3		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0		IRQ8	
K4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
K5					USB0_DM			
K6					USB0_DP			
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2			
K9		PC3	A19	MTIOC4D/GTIOC1B- D/TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
K10		PC2	A18	MTIOC4B/GTIOC2B- D/TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			

Table 4.1 List of I/O Registers (Address Order) (40 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0070h	USB0	Pipe1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0072h	USB0	Pipe2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0074h	USB0	Pipe3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0076h	USB0	Pipe4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0078h	USB0	Pipe5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 007Ah	USB0	Pipe6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 007Ch	USB0	Pipe7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 007Eh	USB0	Pipe8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb

Table 4.1 List of I/O Registers (Address Order) (42 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
000A 0400h	USB	Deep Standby USB Transceiver Control/Pin Monitoring Register	DPUSR0R	32	32	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*5}$	USBb
000A 0404h	USB	Deep Standby USB Suspend/Resume Interrupt Register	DPUSR1R	32	32	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*5}$	USBb
000A 0500h	PDC	PDC Control Register 0	PCCR0	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0504h	PDC	PDC Control Register 1	PCCR1	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0508h	PDC	PDC Status Register	PCSR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 050Ch	PDC	PDC Pin Monitor Register	PCMONR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0510h	PDC	PDC Receive Data Register	PCDR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0514h	PDC	Vertical Capture Register	VCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0518h	PDC	Horizontal Capture Register	HCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000C 0000h	EDMAC 0	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0008h	EDMAC 0	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0010h	EDMAC 0	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0018h	EDMAC 0	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0020h	EDMAC 0	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0028h	EDMAC 0	ETHERC/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0030h	EDMAC 0	ETHERC/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0038h	EDMAC 0	ETHERC/EDMAC Transmit/Receive Status Copy Enable Register	TRSCER	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0040h	EDMAC 0	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0048h	EDMAC 0	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0050h	EDMAC 0	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0058h	EDMAC 0	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0064h	EDMAC 0	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0068h	EDMAC 0	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 006Ch	EDMAC 0	Independent Output Signal Setting Register	IOSR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0070h	EDMAC 0	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0078h	EDMAC 0	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 007Ch	EDMAC 0	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00C8h	EDMAC 0	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00CCh	EDMAC 0	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00D4h	EDMAC 0	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00D8h	EDMAC 0	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0100h	ETHERC0	ETHERC Mode Register	ECMR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0108h	ETHERC0	Receive Frame Length Register	RFLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC

Table 4.1 List of I/O Registers (Address Order) (48 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1406h	MTU2	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1408h	MTU2	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 140Ch	MTU2	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1600h	MTU8	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1601h	MTU8	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1602h	MTU8	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1603h	MTU8	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1604h	MTU8	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1606h	MTU8	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1608h	MTU8	Timer Counter	TCNT	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 160Ch	MTU8	Timer General Register A	TGRA	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1610h	MTU8	Timer General Register B	TGRB	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1614h	MTU8	Timer General Register C	TGRC	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1618h	MTU8	Timer General Register D	TGRD	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A00h	MTU6	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A10h	MTU6	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRb	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A31h	MTU	Timer Interrupt Skipping Counter 1B	TITCNT1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (52 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 2228h	GPT2	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2230h	GPT2	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 4000h	EPTPC	MINT Interrupt Source Status Register	MIESR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPCa

Table 4.1 List of I/O Registers (Address Order) (54 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4328h	EPTPC	Timer Cycle Setting Register 2	TMCYCR2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 432Ch	EPTPC	Timer Pulse Width Setting Register 2	TMPLSR2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4330h	EPTPC	Timer Start Time Setting Register	TMSTTRU3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4334h	EPTPC	Timer Start Time Setting Register	TMSTTRL3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4338h	EPTPC	Timer Cycle Setting Register 3	TMCYCR3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 433Ch	EPTPC	Timer Pulse Width Setting Register 3	TMPLSR3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4340h	EPTPC	Timer Start Time Setting Register	TMSTTRU4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4344h	EPTPC	Timer Start Time Setting Register	TMSTTRL4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4348h	EPTPC	Timer Cycle Setting Register 4	TMCYCR4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 434Ch	EPTPC	Timer Pulse Width Setting Register 4	TMPLSR4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4350h	EPTPC	Timer Start Time Setting Register	TMSTTRU5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4354h	EPTPC	Timer Start Time Setting Register	TMSTTRL5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4358h	EPTPC	Timer Cycle Setting Register 5	TMCYCR5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 435Ch	EPTPC	Timer Pulse Width Setting Register 5	TMPLSR5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 437Ch	EPTPC	Timer Start Register	TMSTARTR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4400h	EPTPC	PRC-TC Status Register	PRSR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4404h	EPTPC	PRC-TC Status Notification Permission Register	PRIPR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4410h	EPTPC	Channel 0 Local MAC Address Register	PRMACRU0	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4414h	EPTPC	Channel 0 Local MAC Address Register	PRMACRL0	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4418h	EPTPC	Channel 1 Local MAC Address Register	PRMACRU1	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 441Ch	EPTPC	Channel 1 Local MAC Address Register	PRMACRL1	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4420h	EPTPC	Packet Transmission Control Register	TRNDISR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4430h	EPTPC	Relay Mode Register	TRNMR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4434h	EPTPC	Cut-Through Transfer Start Threshold Register	TRNCTTDR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4800h	EPTPC 0	SYNFP Status Register	YSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4804h	EPTPC 0	SYNFP Status Notification Permission Register	SYIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4810h	EPTPC 0	SYNFP MAC Address Register	SYMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4814h	EPTPC 0	SYNFP MAC Address Register	SYMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4818h	EPTPC 0	SYNFP LLC-CTL Value Register	SYLLCCTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 481Ch	EPTPC 0	SYNFP Local IP Address Register	SYIPADDRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4840h	EPTPC 0	SYNFP Specification Version Setting Register	SYSPVRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4844h	EPTPC 0	SYNFP Domain Number Setting Register	SYDOMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4850h	EPTPC 0	Announce Message Flag Field Setting Register	ANFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4854h	EPTPC 0	Sync Message Flag Field Setting Register	SYNFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4858h	EPTPC 0	Delay_Req Message Flag Field Setting Register	DYRQFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 485Ch	EPTPC 0	Delay_Resp Message Flag Field Setting Register	DYRPFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4860h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4864h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4868h	EPTPC 0	SYNFP Local Port Number Register	SYPNUMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4880h	EPTPC 0	SYNFP Register Value Load Directive Register	SYRVLDR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa

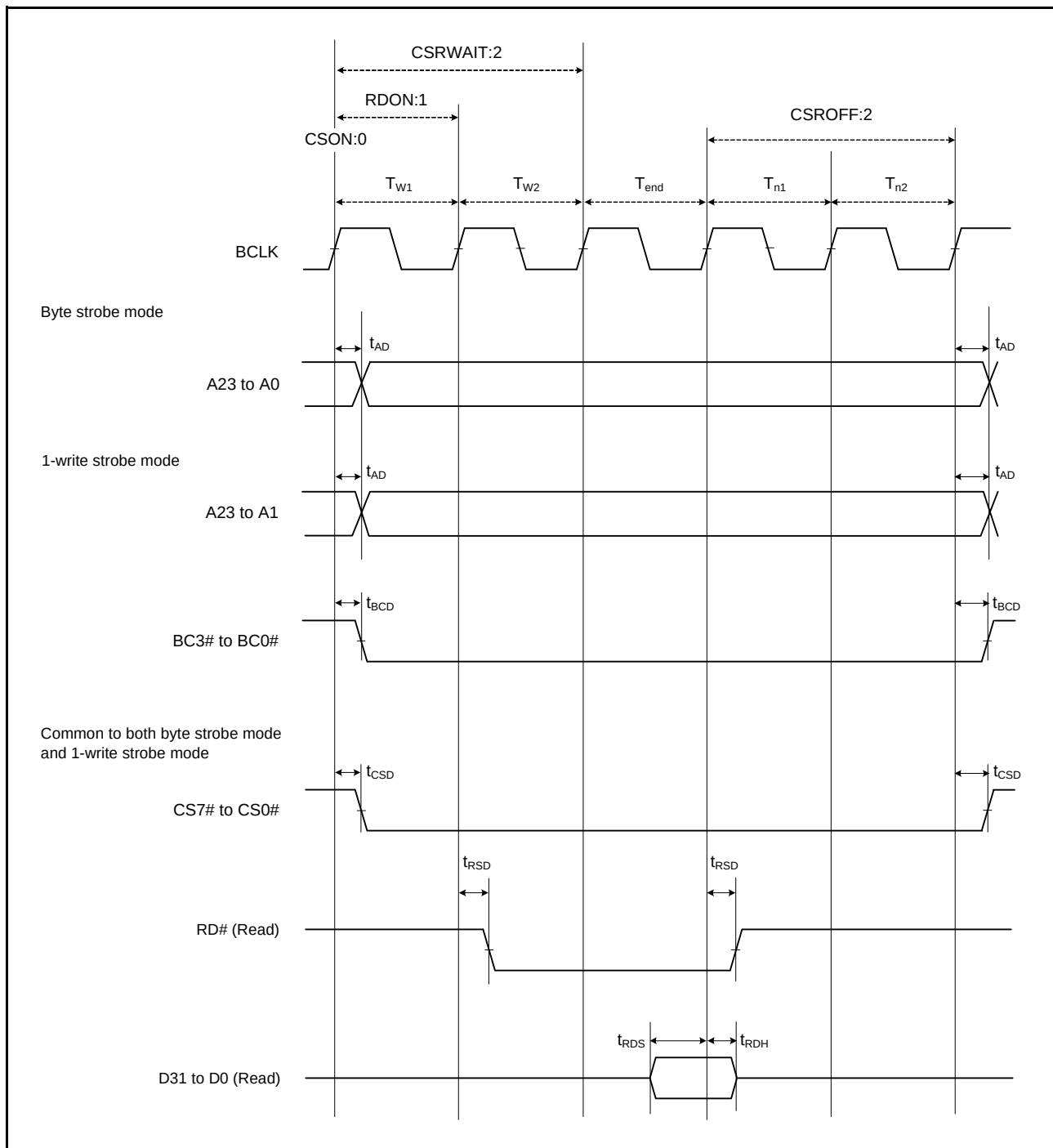
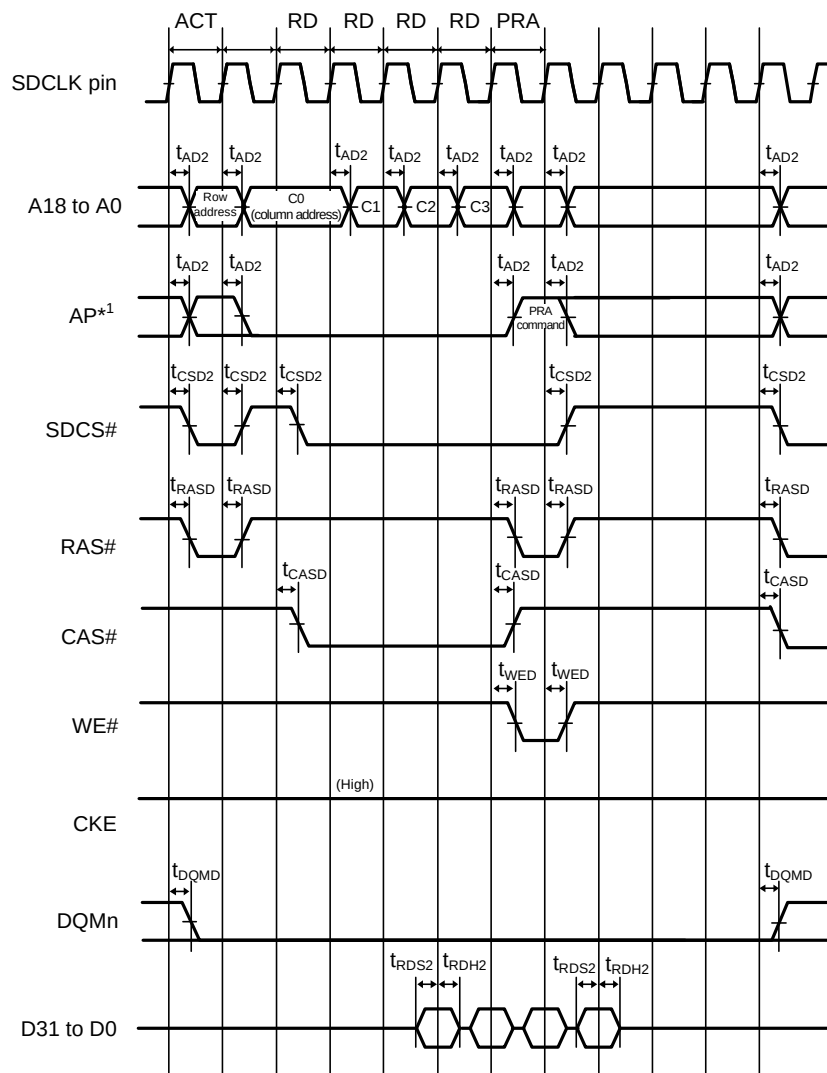


Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.25 SDRAM Space Multiple Read Bus Timing

Table 5.24 TPU Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{PBcyc}	Figure 5.34
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH} , t_{TCKWL}	1.5	—	t_{PBcyc}	Figure 5.35
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PBcyc} : PCLKB cycle

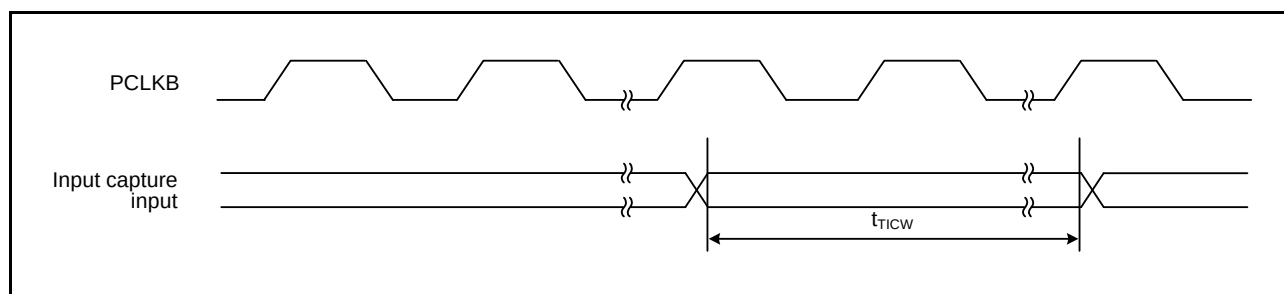
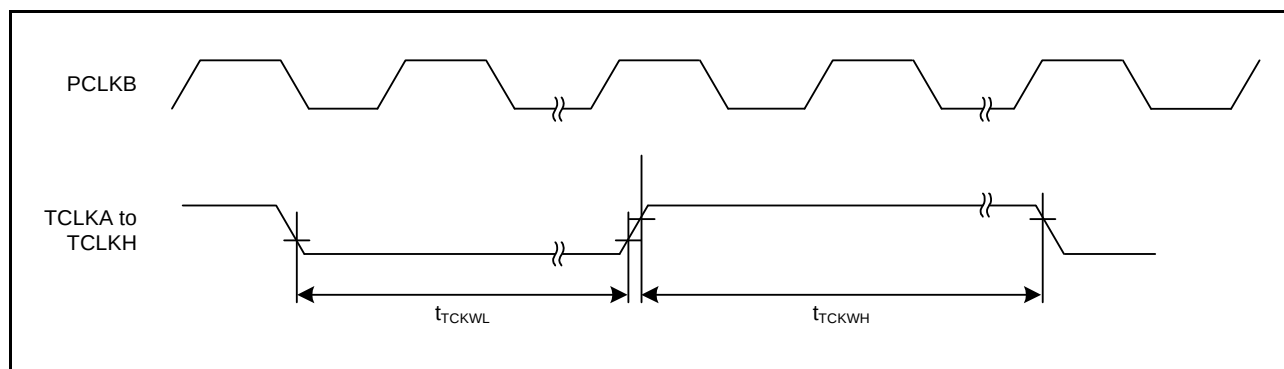
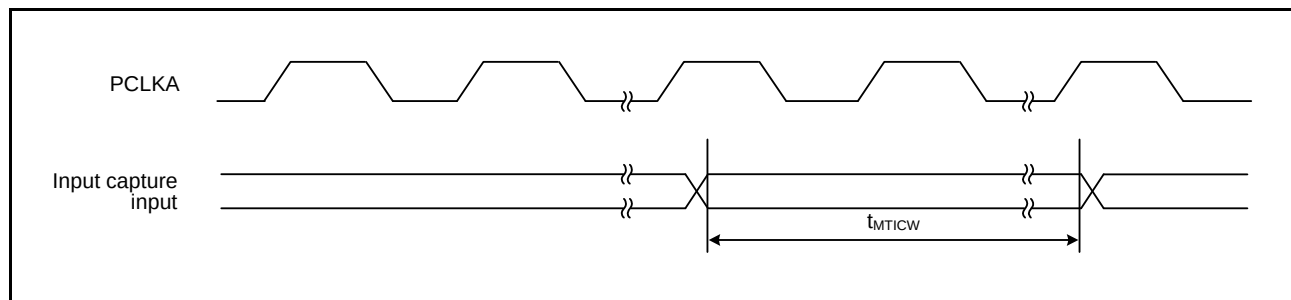
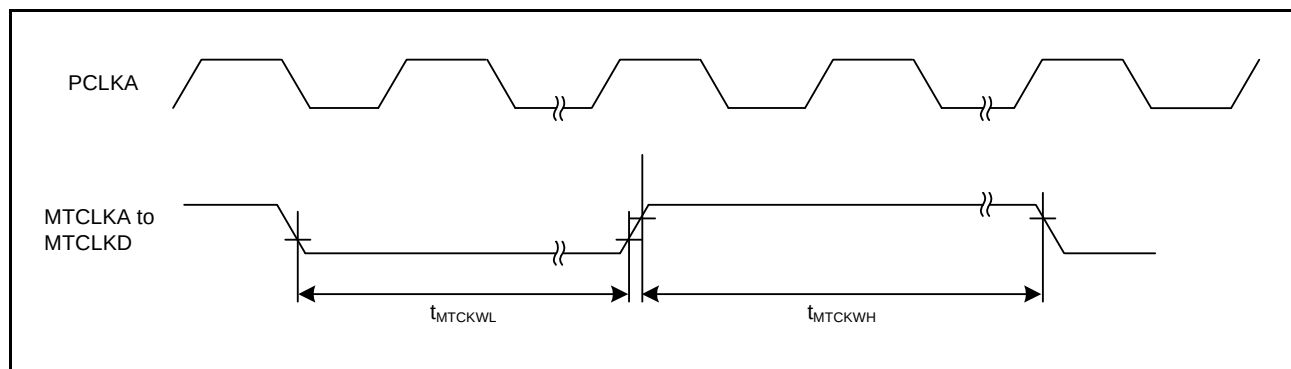
**Figure 5.34 TPU Input Capture Input Timing****Figure 5.35 TPU Clock Input Timing**

Table 5.27 MTU3 Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU3	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PAcyc}	Figure 5.38
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH} , t_{MTCKWL}	1.5	—	t_{PAcyc}	Figure 5.39
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PAcyc} : PCLKA cycle

**Figure 5.38 MTU3 Input Capture Input Timing****Figure 5.39 MTU3 Clock Input Timing**

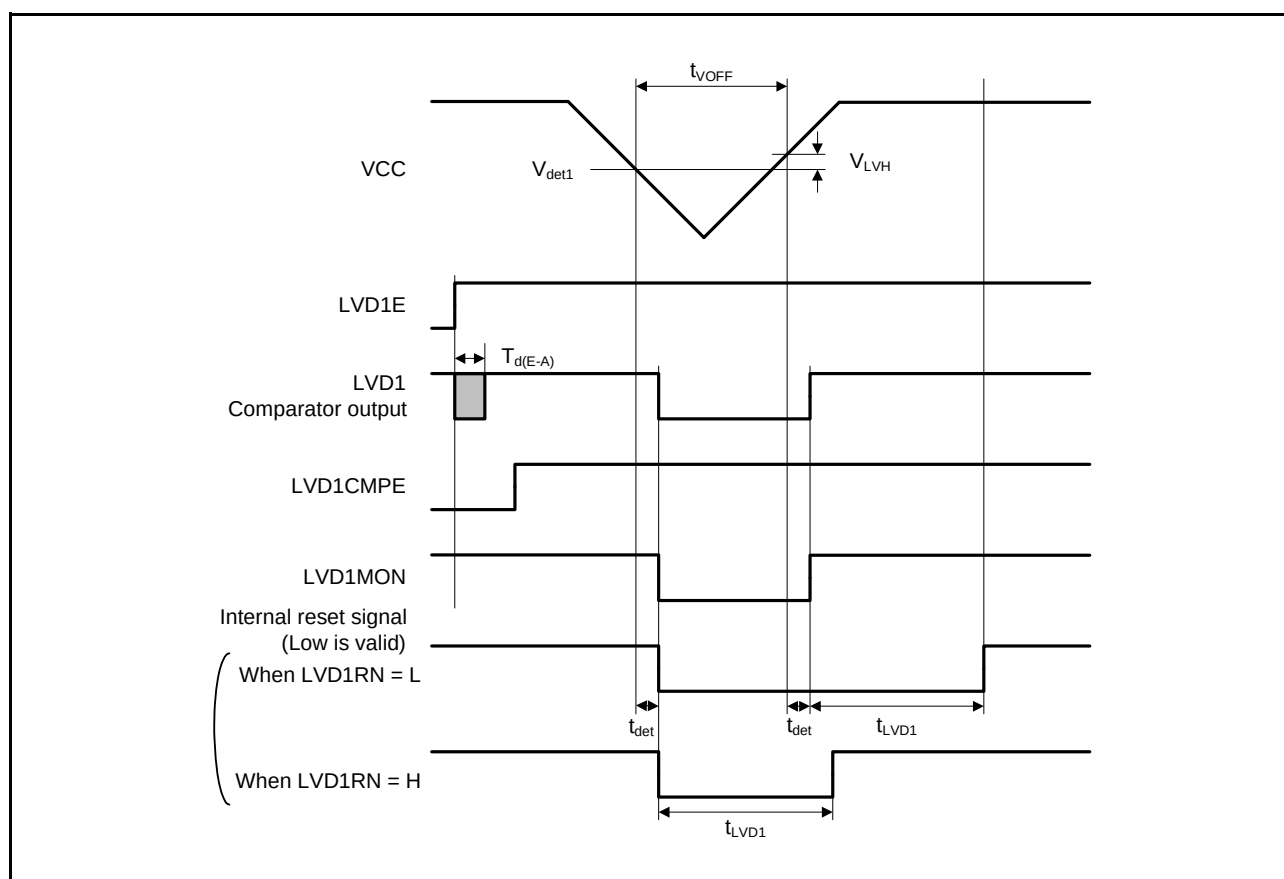


Figure 5.85 Voltage Detection Circuit Timing (V_{det1})

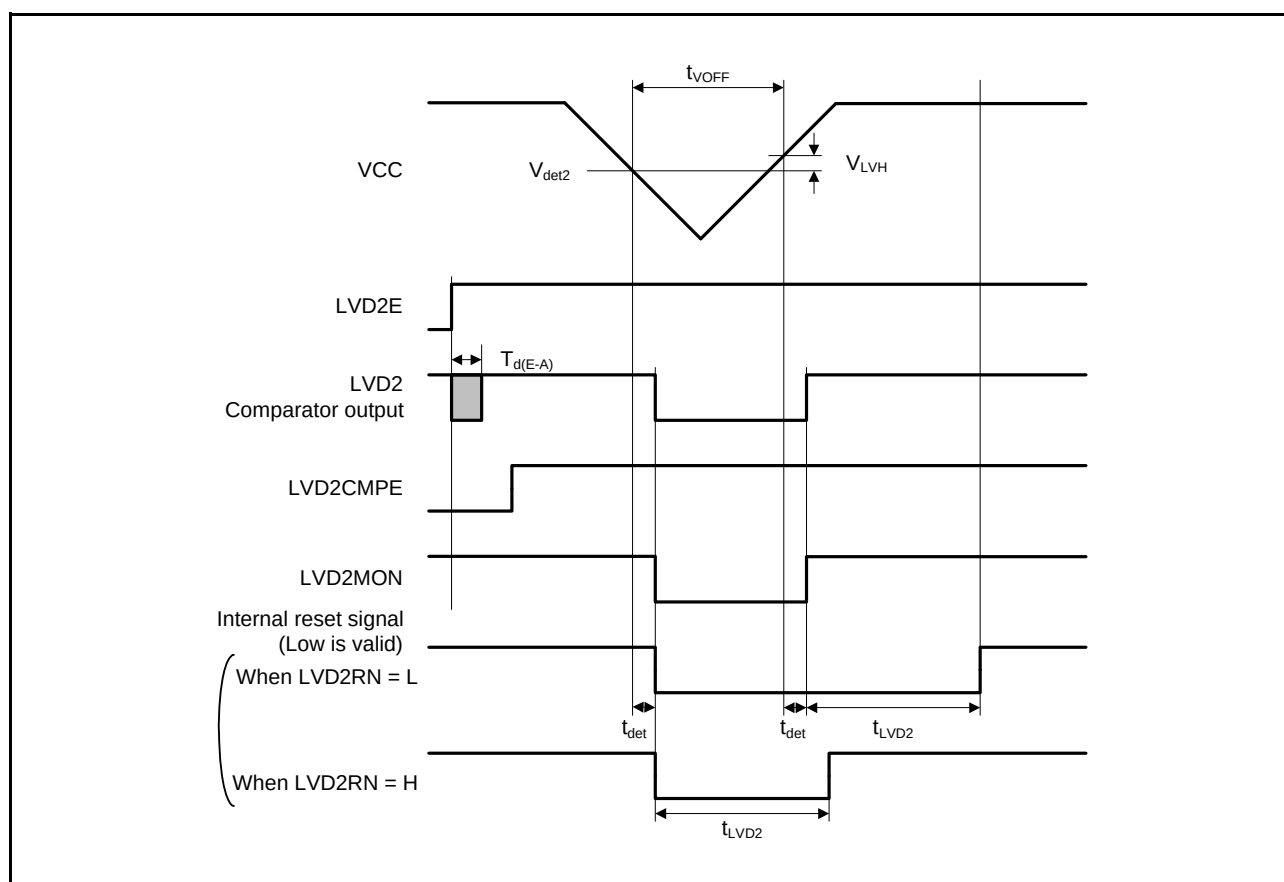


Figure 5.86 Voltage Detection Circuit Timing (V_{det2})

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

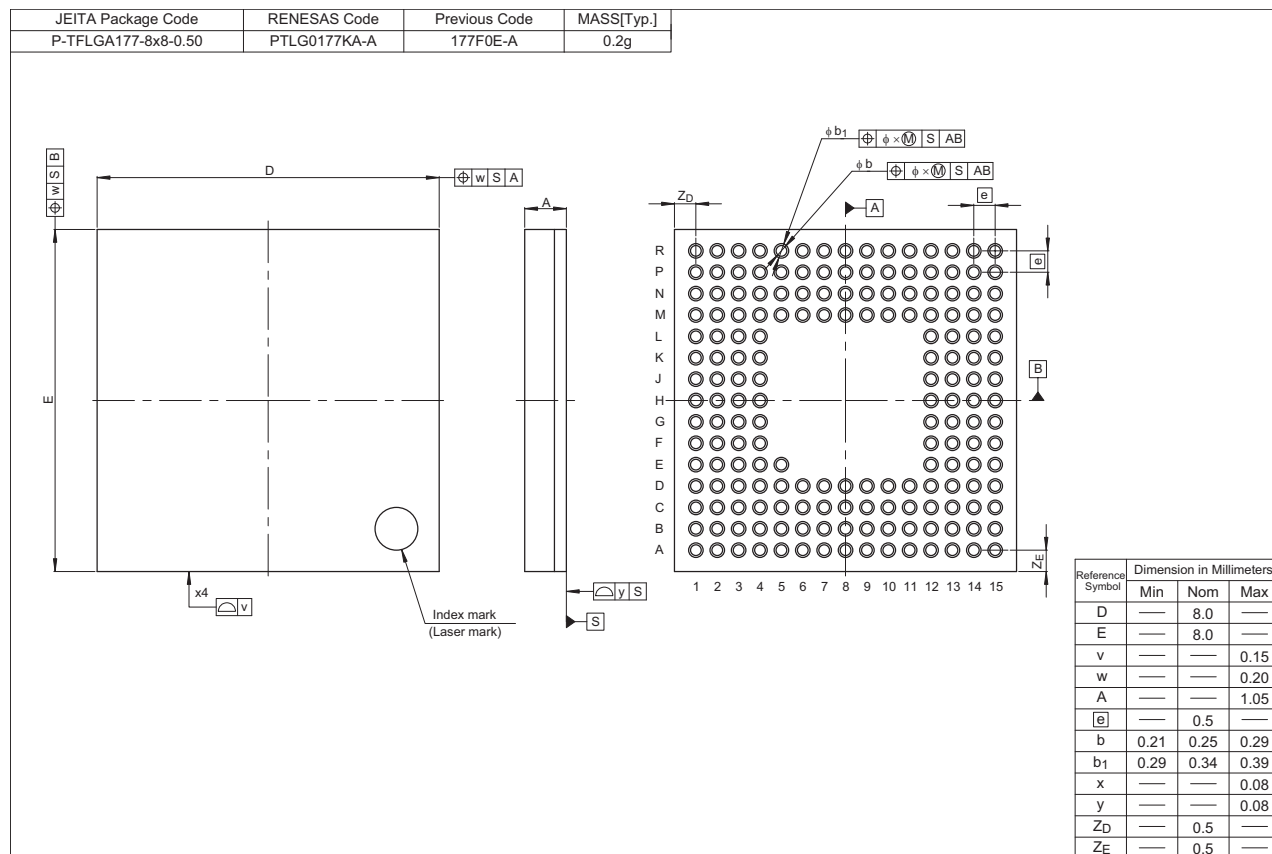


Figure A 177-Pin TFLGA (PTLG0177KA-A)

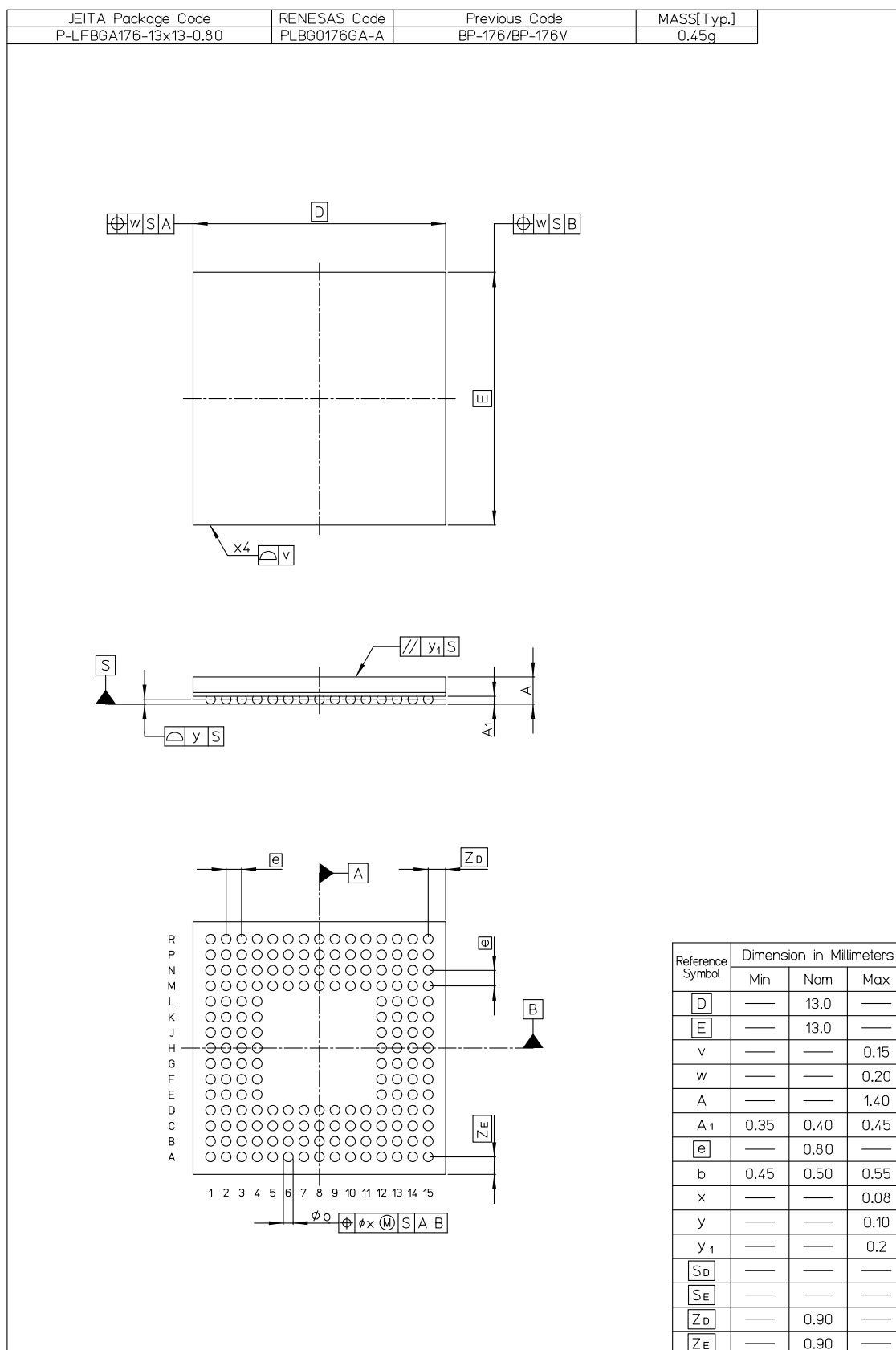


Figure B 176-Pin LFBGA (PLBG0176GA-A)

