



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mggdbg-20

Table 1.1 Outline of Specifications (10/10)

Classification	Module/Function	Description
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.

Note 2. Setting is only possible when the input sampling rate 44.1 kHz is selected.

Note 3. The product part number differs according to whether or not it supports encryption.

Note 4. The product part number differs according to whether or not it includes an SDHI (SD host interface).

Table 1.4 Pin Functions (5/8)

Classifications	Pin Name	I/O	Description
Ethernet controller	REF50CK0, REF50CK1	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timings in RMII mode.
	RMII0_CRS_DV, RMII1_CRS_DV	Input	Indicate that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1, RMII1_TXD0, RMII1_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1, RMII1_RXD0, RMII1_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN, RMII1_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode
	RMII0_RX_ER, RMII1_RX_ER	Input	Indicate an error has occurred during reception of data in RMII mode.
	ET0_CRS, ET1_CRS	Input	Carrier detection/data reception enable pins
	ET0_RX_DV, ET1_RX_DV	Input	Indicate that there are valid receive data on ET_ERXD3 to ET_ERXD0.
	ET0_EXOUT, ET1_EXOUT	Output	General-purpose external output pins
	ET0_LINKSTA ET1_LINKSTA	Input	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3, ET1_ETXD0 to ET1_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3, ET1_ERXD0 to ET1_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN, ET1_TX_EN	Output	Transmit enable pins. Function as signals indicating that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET0_TX_ER, ET1_TX_ER	Output	Transmit error pins. Function as signals notifying the PHY-LSI of an error during transmission.
	ET0_RX_ER, ET1_RX_ER	Input	Receive error pins. Function as signals to recognize an error during reception.
	ET0_TX_CLK, ET1_TX_CLK	Input	Transmit clock pins. These pins input reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET0_RX_CLK, ET1_RX_CLK	Input	Receive clock pins. These pins input reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET0_COL, ET1_COL	Input	Input collision detection signals.
	ET0_WOL, ET1_WOL	Output	Receive Magic packets.
	ET0_MDC, ET1_MDC	Output	Output reference clock signals for information transfer via ET_MDIO.
	ET0_MDIO, ET1_MDIO	I/O	Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI.

Table 1.4 Pin Functions (7/8)

Classifications	Pin Name	I/O	Description
MMC host interface	MMC_CLK-A/ MMC_CLK-B	Output	MMC clock pin
	MMC_CMD-A/ MMC_CMD-B	I/O	Command/response pin
	MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B	I/O	Transmit data/receive data
	MMC_CD-A/MMC_CD-B	Input	Card detection pin
	MMC_RES#-A/MMC_RES#-B	Output	MMC reset output pin
SD host interface	SDHI_CLK-A/SDHI_CLK-B	Output	SD clock output pin
	SDHI_CMD-A/SDHI_CMD-B	I/O	SD command output, response input signal pin
	SDHI_D3-A/SDHI_D3-B to SDHI_D0-A/SDHI_D0-B	I/O	SD data bus pins
	SDHI_CD-A/SDHI_CD-B	Input	SD card detection pin
	SDHI_WP-A/SDHI_WP-B	Input	SD write-protect signal
Parallel data capture unit	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
12-bit A/D converter	AN000 to AN007, AN100 to AN120	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	AVCC1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply.
	AVSS1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply.

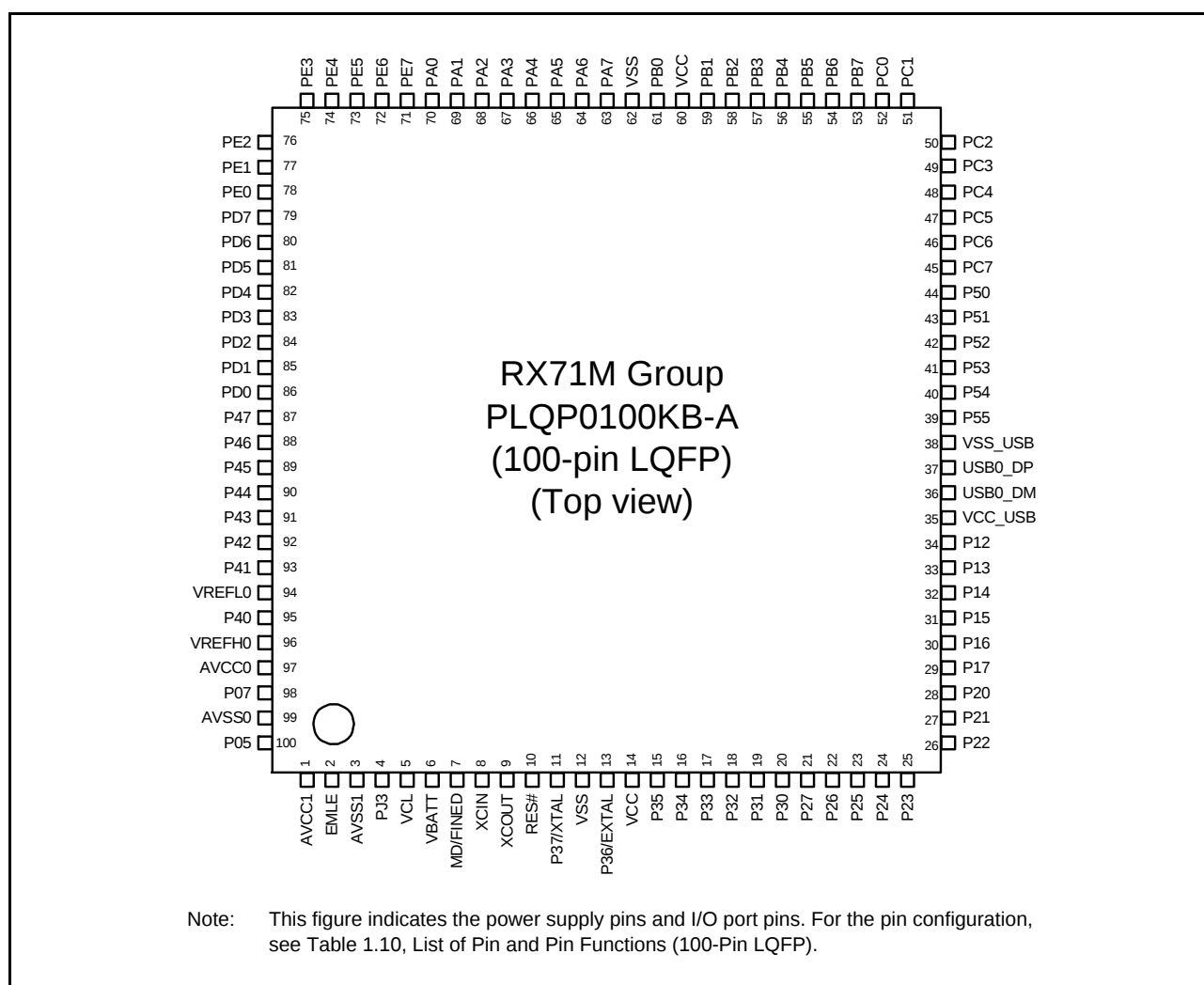
**Figure 1.9 Pin Assignment (100-Pin LQFP)**

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (6/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
141		P60	CS0#		ET1_TX_EN/ RMII1_TXD_EN			
142	VCC							
143		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
144		PG1	D25		ET1_RX_ER/ RMII1_RX_ER			
145		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
146		PG0	D24		ET1_RX_CLK/ REF50CK1			
147		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
148		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
149		P97	A23/D23		ET1_ERXD3			
150		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
151	VSS							
152		P96	A22/D22		ET1_ERXD2			
153	VCC							
154		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2_B	IRQ2	AN110
155		P95	A21/D21		ET1_ERXD1/ RMII1_RXD1			
156		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
157		P94	A20/D20		ET1_ERXD0/ RMII1_RXD0			
158		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
159		P93	A19/D19	POE0#	ET1_LINKSTA/CTS7#/ RTS7#/SS7#			AN117
160		P92	A18/D18	POE4#	ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7			AN116
161		P91	A17/D17		ET1_COL/SCK7			AN115
162	VSS							
163		P90	A16/D16		ET1_RX_DV/ TXD7/SMOSI7/SSDA7			AN114
164	VCC							
165		P47					IRQ15- DS	AN007
166		P46					IRQ14- DS	AN006
167		P45					IRQ13- DS	AN005
168		P44					IRQ12- DS	AN004
169		P43					IRQ11-DS	AN003
170		P42					IRQ10- DS	AN002

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
F13		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
G1	XTAL	P37						
G2	RES							
G3	MD/FINED							
G4	BSCANP							
G10		PA5	A5	MTIOC6B/TIOC6B1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
G11		PA6	A6	MTIC5V/MTCLKB/ GTETR-G-C/TIOCA2/ TMC13/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
G12	VCC							
G13		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
H1	EXTAL	P36						
H2	VCC							
H3	VSS							
H4	UPSEL	P35					NMI	
H10		P72	A19/CS2#		ET0_MDC			
H11		P71	A18/CS1#		ET0_MDIO			
H12		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
H13		PA7	A7	TIOC6B/PO23	MISOA-B/ET0_WOL			
J1	TRST#	P34		MTIOC0A/TMC13/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
J2		P33	EDREQ1	MTIOC0D/TIOC0D/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
J3		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOU/RTIC12/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
J4	TDI	P30		MTIOC4B/TMRI3/ PO8/RTIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS	
J10		PB3	A11	MTIOC0A/MTIOC4A/ TIOC03/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
J11		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
J12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
J13		PB1	A9	MTIOC0C/MTIOC4C/ TIOC03/TMC10/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
K1	TCK	P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/RSPCKB-A			
K2	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A			
K3	TMS	P31		MTIOC4D/TMC12/ PO9/RTIC1	CTS1#/RTS1#/SS1#/ SSLB0-A		IRQ1-DS	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
M2		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOC0B0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
M3		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
M4		P12		TMC11	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
M5	VCC_USB							
M6	VSS_USB							
M7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
M8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMC12/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
M10		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		
M11		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
M12		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
M13	VCC							
N1		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0	PIXD5	IRQ9	
N2		P20		MTIOC1A/TIOC3B/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0	PIXD4	IRQ8	
N3		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
N4		P14		MTIOC3A/MTCLKA/ TIOC3B5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
N5					USB0_DM			
N6					USB0_DP			
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
N8	VSS							
N9	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
N11		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
N12		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
N13		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			

Table 4.1 List of I/O Registers (Address Order) (16 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMRb
0008 821Ch	TMR2	Time Count Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMRb
0008 821Dh	TMR3	Time Count Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMRb
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	CRC
0008 8300h	RIIC0	I ² C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8301h	RIIC0	I ² C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8302h	RIIC0	I ² C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8303h	RIIC0	I ² C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8304h	RIIC0	I ² C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8305h	RIIC0	I ² C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8306h	RIIC0	I ² C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8307h	RIIC0	I ² C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8308h	RIIC0	I ² C Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8309h	RIIC0	I ² C Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8310h	RIIC0	I ² C Bus Bit Rate Low Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8311h	RIIC0	I ² C Bus Bit Rate High Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8312h	RIIC0	I ² C Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8313h	RIIC0	I ² C Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8340h	RIIC2	I ² C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8341h	RIIC2	I ² C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8342h	RIIC2	I ² C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8343h	RIIC2	I ² C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8344h	RIIC2	I ² C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8345h	RIIC2	I ² C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8346h	RIIC2	I ² C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8347h	RIIC2	I ² C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8348h	RIIC2	I ² C Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8349h	RIIC2	I ² C Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ah	RIIC2	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Bh	RIIC2	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ch	RIIC2	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Dh	RIIC2	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Eh	RIIC2	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Fh	RIIC2	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8350h	RIIC2	I ² C Bus Bit Rate Low Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8351h	RIIC2	I ² C Bus Bit Rate High Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8352h	RIIC2	I ² C Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8353h	RIIC2	I ² C Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8500h	MMCIF	Command Setting Register	CECMDSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8508h	MMCIF	Argument Register	CEARG	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 850Ch	MMCIF	CMD12 Argument Register	CEARGCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF

Table 4.1 List of I/O Registers (Address Order) (19 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9161h	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9170h	S12AD1	A/D Sampling State Register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9171h	S12AD1	A/D Sampling State Register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9176h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9177h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9178h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9179h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 917Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9184h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9186h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9190h	S12AD1	A/D Compare Control Register	ADCMPCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9192h	S12AD1	A/D Compare Channel Select Extended Register	ADCMPSER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9193h	S12AD1	A/D Compare Level Extended Register	ADCMPLER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9194h	S12AD1	A/D Compare Channel Select Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9196h	S12AD1	A/D Compare Channel Select Register 1	ADCMPSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9198h	S12AD1	A/D Compare Level Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ah	S12AD1	A/D Compare Level Register 1	ADCMPLR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ch	S12AD1	A/D Compare Data Register 0	ADCMPCR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Eh	S12AD1	A/D Compare Data Register 1	ADCMPCR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A0h	S12AD1	A/D Compare Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A2h	S12AD1	A/D Compare Status Register 1	ADCMPSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A4h	S12AD1	A/D Compare Status Extended Register	ADCMPSER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9E00h	QSPI	QSPI Control Register	SPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E01h	QSPI	QSPI Slave Select Polarity Register	SSLP	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E02h	QSPI	QSPI Pin Control Register	SPPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E03h	QSPI	QSPI Status Register	SPSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E04h	QSPI	QSPI Data Register	SPDR	32	8, 16, 32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E08h	QSPI	QSPI Sequence Control Register	SPSCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E09h	QSPI	QSPI Sequence Status Register	SPSSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ah	QSPI	QSPI Bit Rate Register	SPBR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Bh	QSPI	QSPI Data Control Register	SPDCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ch	QSPI	QSPI Clock Delay Register	SPCKD	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Dh	QSPI	QSPI Slave Select Negation Delay Register	SSLND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Eh	QSPI	QSPI Next-Access Delay Register	SPND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E10h	QSPI	QSPI Command Register 0	SPCMD0	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E12h	QSPI	QSPI Command Register 1	SPCMD1	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E14h	QSPI	QSPI Command Register 2	SPCMD2	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E16h	QSPI	QSPI Command Register 3	SPCMD3	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E18h	QSPI	QSPI Buffer Control Register	SPBFCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ah	QSPI	QSPI Buffer Data Count Register	SPBDCR	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ch	QSPI	QSPI Transfer Data Length Multiplier Setting Register 0	SPBMUL0	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E20h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 1	SPBMUL1	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI

Table 4.1 List of I/O Registers (Address Order) (24 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIf
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C6h	SCI6	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIf
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIf
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E0h	SCI7	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E1h	SCI7	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E2h	SCI7	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E3h	SCI7	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E4h	SCI7	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E5h	SCI7	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf

Table 4.1 List of I/O Registers (Address Order) (32 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C16Eh	MPC	P56 Pin Function Control Register	P56PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C170h	MPC	P60 Pin Function Control Register	P60PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C176h	MPC	P66 Pin Function Control Register	P66PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C177h	MPC	P67 Pin Function Control Register	P67PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Fh	MPC	P77 Pin Function Control Register	P77PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C183h	MPC	P83 Pin Function Control Register	P83PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C186h	MPC	P86 Pin Function Control Register	P86PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C187h	MPC	P87 Pin Function Control Register	P87PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C18Fh	MPC	P97 Pin Function Control Register	P97PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC

Table 4.1 List of I/O Registers (Address Order) (40 / 67)

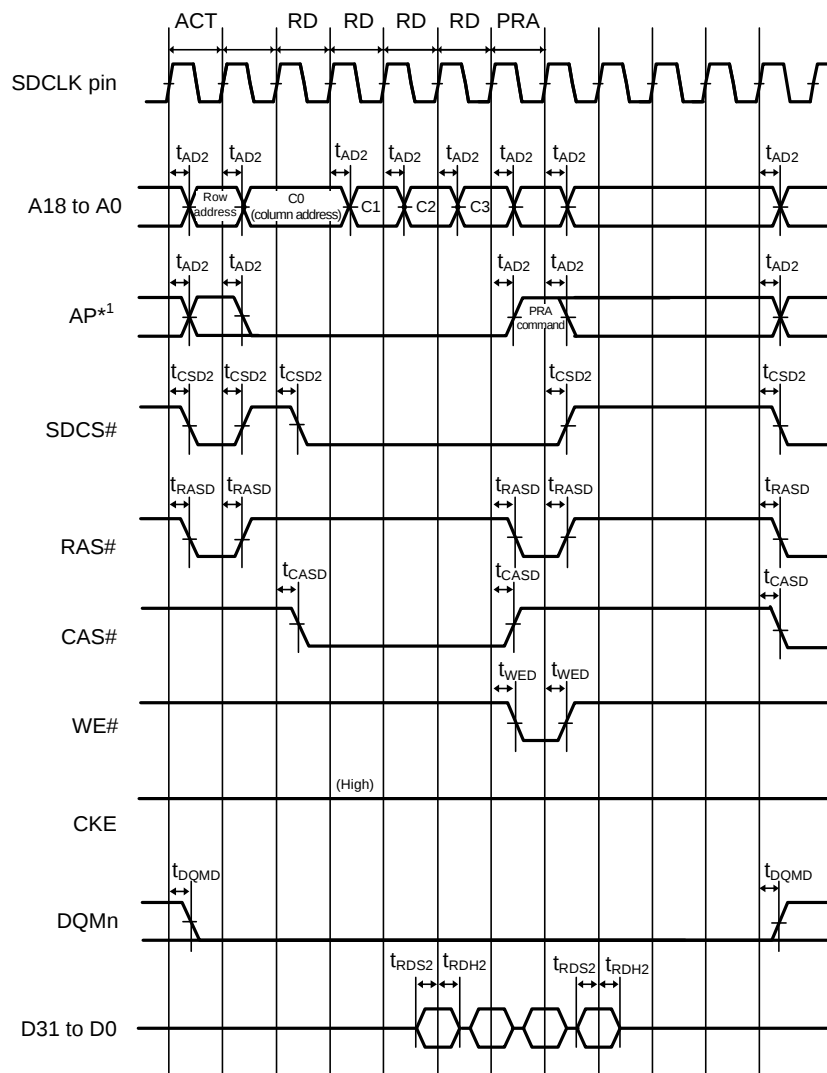
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0070h	USB0	Pipe1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0072h	USB0	Pipe2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0074h	USB0	Pipe3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0076h	USB0	Pipe4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0078h	USB0	Pipe5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 007Ah	USB0	Pipe6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 007Ch	USB0	Pipe7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 007Eh	USB0	Pipe8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb

Table 4.1 List of I/O Registers (Address Order) (48 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1406h	MTU2	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1408h	MTU2	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 140Ch	MTU2	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1600h	MTU8	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1601h	MTU8	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1602h	MTU8	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1603h	MTU8	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1604h	MTU8	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1606h	MTU8	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1608h	MTU8	Timer Counter	TCNT	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 160Ch	MTU8	Timer General Register A	TGRA	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1610h	MTU8	Timer General Register B	TGRB	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1614h	MTU8	Timer General Register C	TGRC	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1618h	MTU8	Timer General Register D	TGRD	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A00h	MTU6	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A10h	MTU6	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRb	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A31h	MTU	Timer Interrupt Skipping Counter 1B	TITCNT1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (55 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4890h	EPTPC 0	SYNFP Reception Filter Register 1	SYRFL1R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4894h	EPTPC 0	SYNFP Reception Filter Register 2	SYRFL2R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4898h	EPTPC 0	SYNFP Transmission Enable Register	SYTRENr	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A0h	EPTPC 0	Master Clock ID Register	MTCIDU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A4h	EPTPC 0	Master Clock ID Register	MTCIDL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A8h	EPTPC 0	Master Clock Port Number Register	MTPID	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C0h	EPTPC 0	SYNFP Transmission Interval Setting Register	SYTLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C4h	EPTPC 0	SYNFP Received logMessageInterval Value Indication Register	SYRLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C8h	EPTPC 0	offsetFromMaster Value Register	OFMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48CCh	EPTPC 0	offsetFromMaster Value Register	OFMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48D0h	EPTPC 0	meanPathDelay Value Register	MPDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48D4h	EPTPC 0	meanPathDelay Value Register	MPDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E0h	EPTPC 0	grandmasterPriority Field Setting Register	GMPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E4h	EPTPC 0	grandmasterClockQuality Field Setting Register	GMCQR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E8h	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48ECh	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48F0h	EPTPC 0	currentUtcOffset/timeSource Field Setting Register	CUOTSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48F4h	EPTPC 0	stepsRemoved Field Setting Register	SRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4900h	EPTPC 0	PTP-primary Message Destination MAC Address Setting Registers	PPMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4904h	EPTPC 0	PTP-primary Message Destination MAC Address Setting Registers	PPMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4908h	EPTPC 0	PTP-pdelay Message MAC Address Setting Registers	PDMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 490Ch	EPTPC 0	PTP-pdelay Message MAC Address Setting Registers	PDMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4910h	EPTPC 0	PTP Message EtherType Setting Register	PETYPER	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4920h	EPTPC 0	PTP-primary Message Destination IP Address Setting Register	PPIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4924h	EPTPC 0	PTP-pdelay Message Destination IP Address Setting Register	PDIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4928h	EPTPC 0	PTP event Message TOS Setting Register	PETOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 492Ch	EPTPC 0	PTP general Message TOS Setting Register	PGTOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4930h	EPTPC 0	PTP-primary Message TTL Setting Register	PPTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4934h	EPTPC 0	PTP-pdelay Message TTL Setting Register	PDTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4938h	EPTPC 0	PTP event Message UDP Destination Port Number Setting Register	PEUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 493Ch	EPTPC 0	PTP general Message UDP Destination Port Number Setting Register	PGUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.25 SDRAM Space Multiple Read Bus Timing

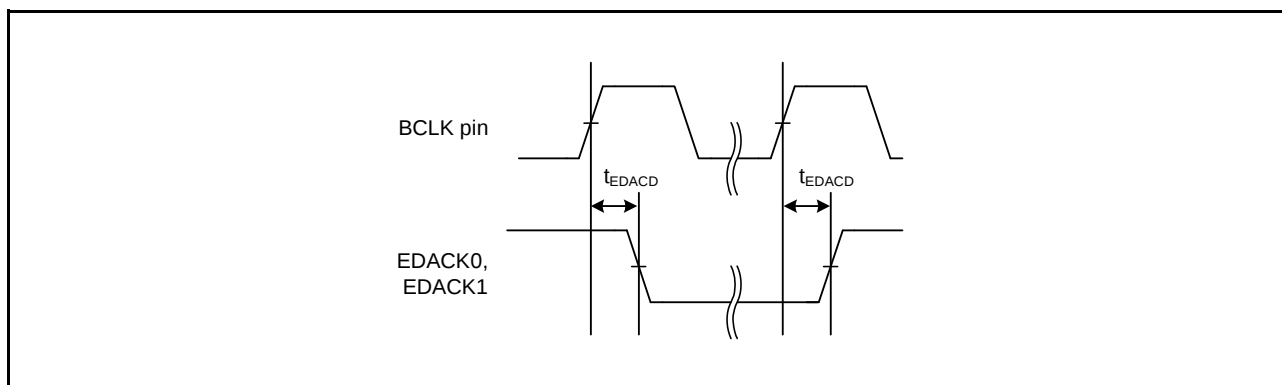


Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)

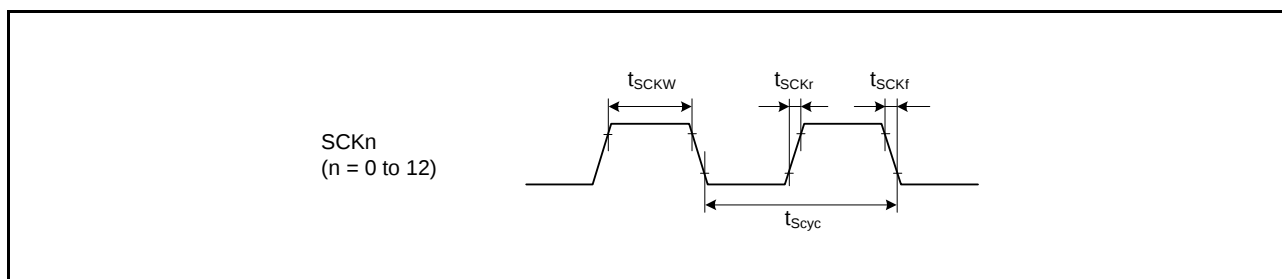


Figure 5.44 SCK Clock Input Timing

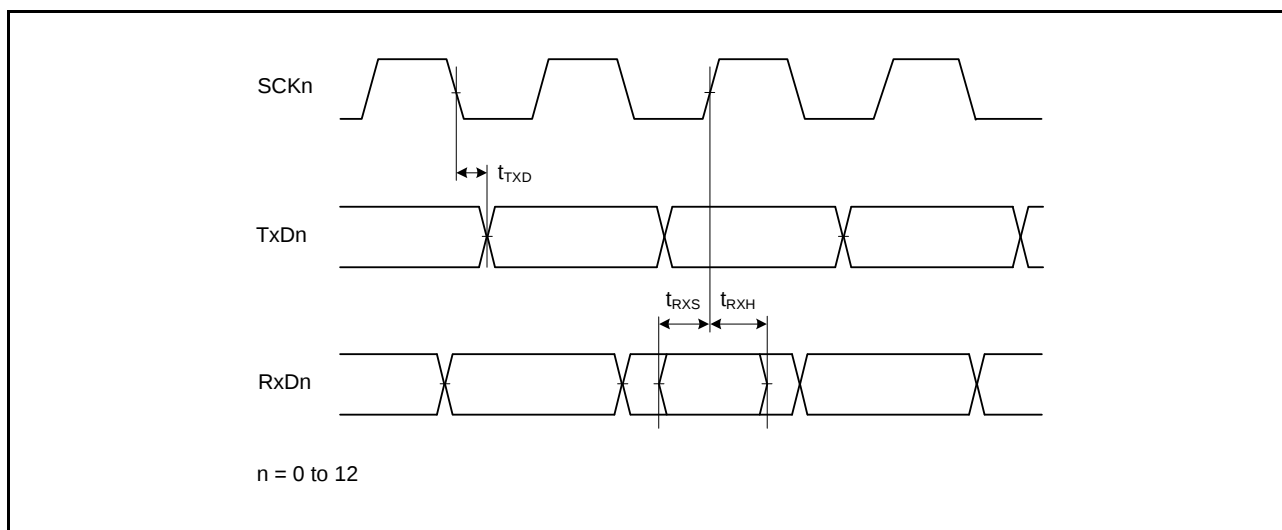


Figure 5.45 SCI Input/Output Timing: Clock Synchronous Mode

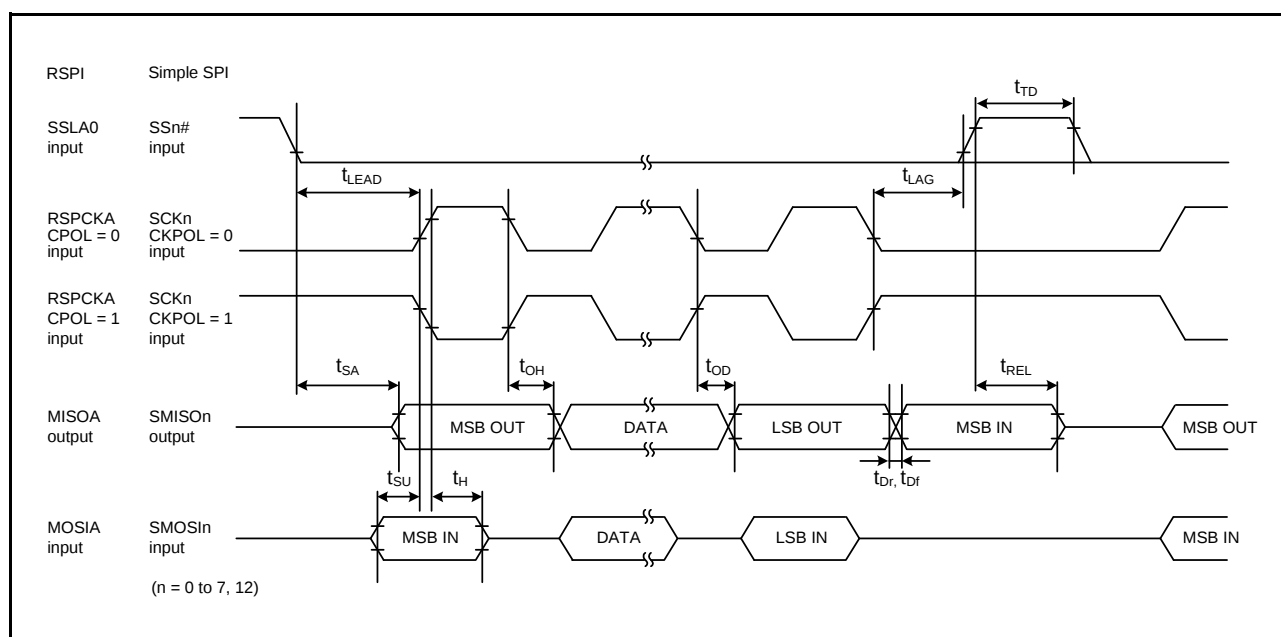


Figure 5.51 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

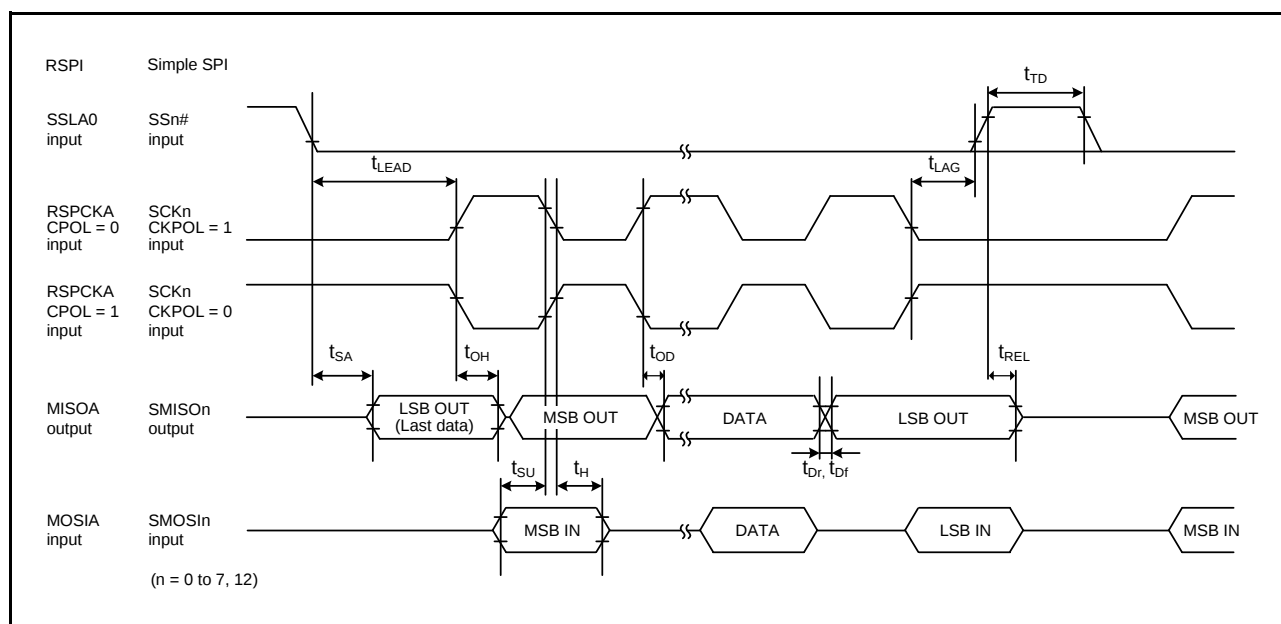


Figure 5.52 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

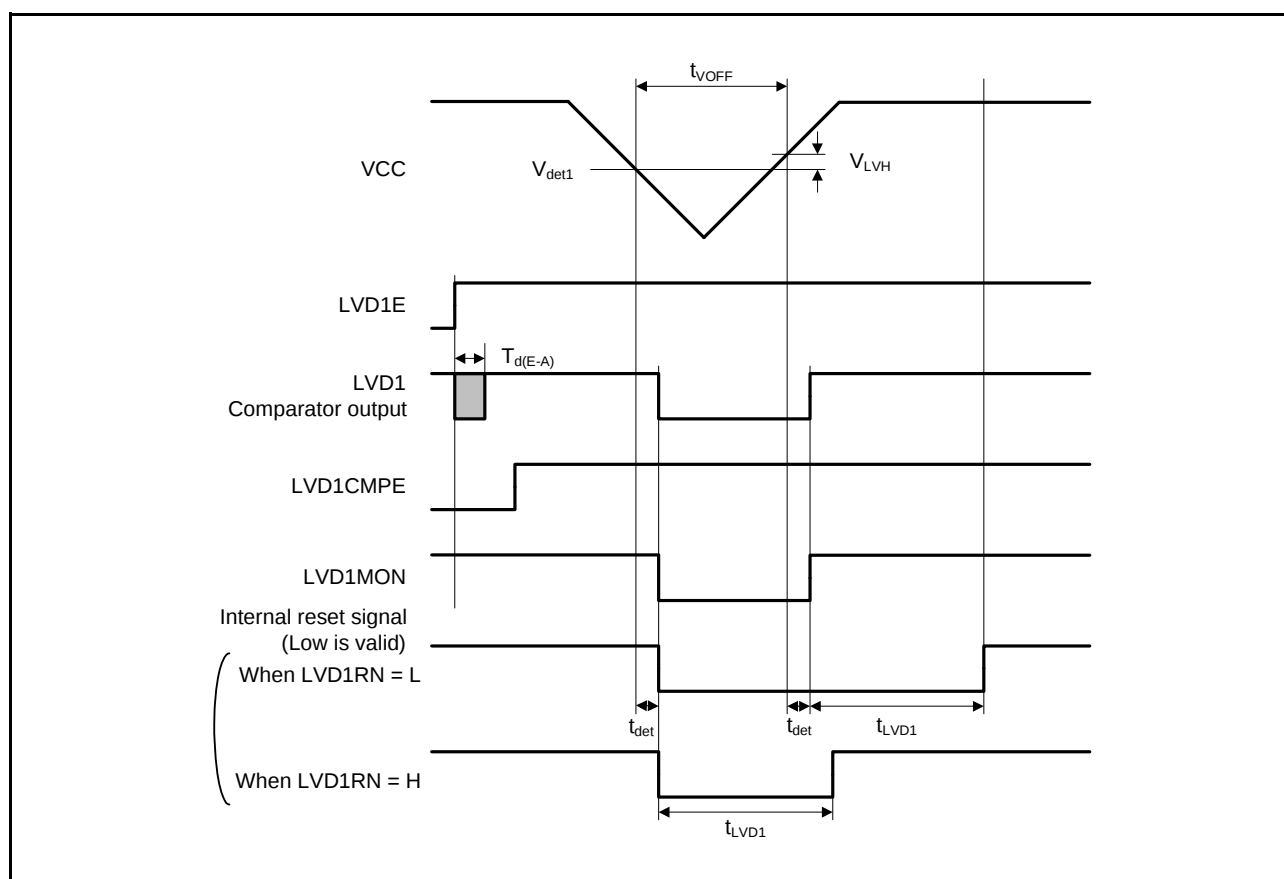


Figure 5.85 Voltage Detection Circuit Timing (V_{det1})

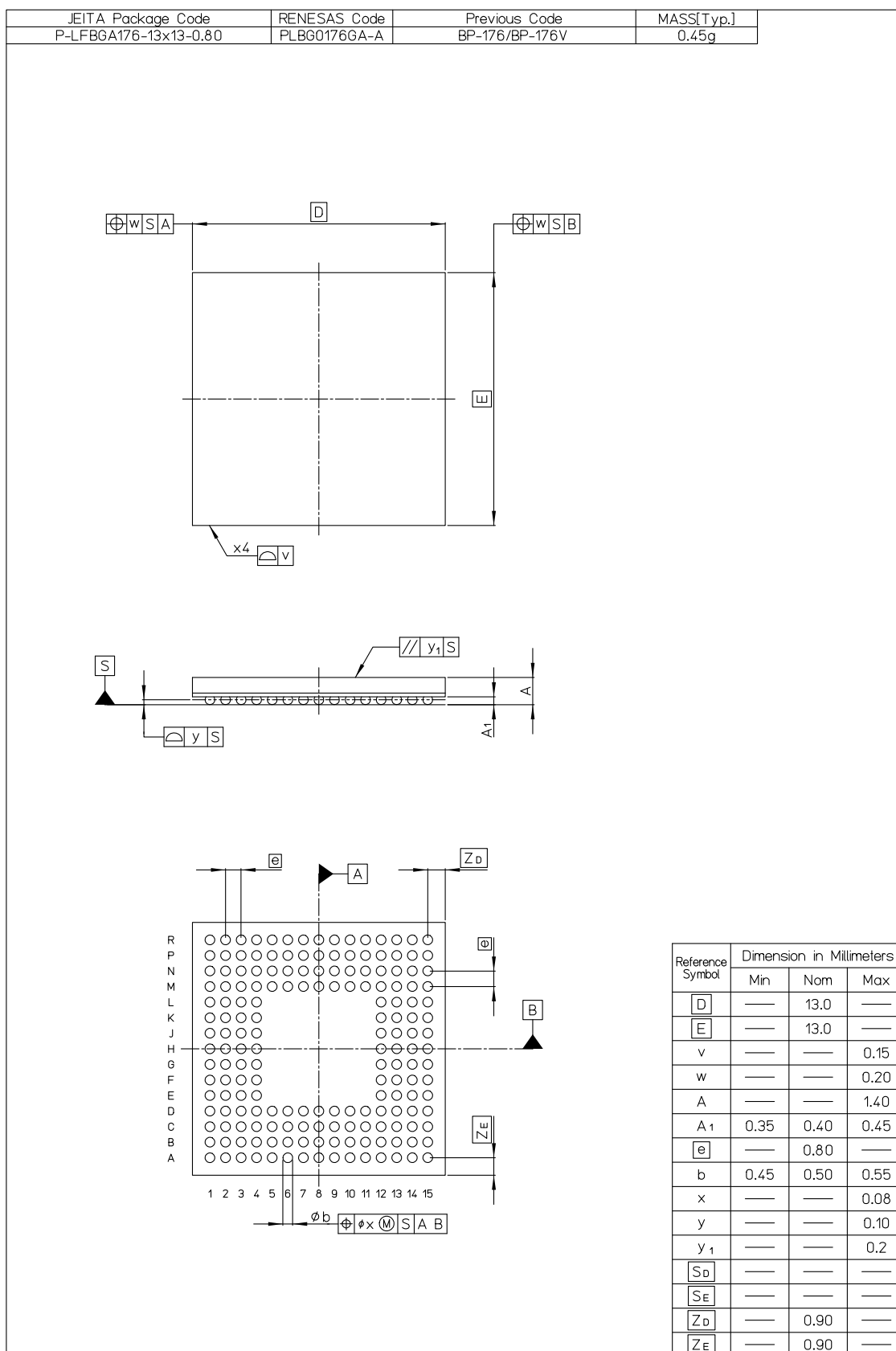


Figure B 176-Pin LFBGA (PLBG0176GA-A)