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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mgbdbg-20

Table 1.2 Comparison of Functions for Different Packages (2/2)

Functions	RX71M Group		
Package	177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins
DES	Available		
SHA	Available		
RNG	Available		
Event link controller	Available		

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
A1	AVSS0							
A2	AVCC0							
A3	VREFL0							
A4		P42					IRQ10-DS	AN002
A5		P46					IRQ14-DS	AN006
A6	VCC							
A7	VSS							
A8		P94	A20/D20		ET1_ERXD0/ RMII1_RXD0			
A9	VCC							
A10		P97	A23/D23		ET1_ERXD3			
A11		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
A12		P60	CS0#		ET1_TX_EN/ RMII1_TXD_EN			
A13		P63	CS3#/CAS#					
A14		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
A15		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXD12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
B1		P05					IRQ13	DA1
B2		P07					IRQ15	ADTRG0#
B3		P40					IRQ8-DS	AN000
B4		P41					IRQ9-DS	AN001
B5		P47					IRQ15-DS	AN007
B6		P91	A17/D17		ET1_COL/SCK7			AN115
B7		P92	A18/D18	POE4#	ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7			AN116
B8		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
B9		P96	A22/D22		ET1_ERXD2			
B10		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
B11		PG1	D25		ET1_RX_ER/ RMII1_RX_ER			
B12	VSS							
B13		P64	CS4#/WE#					
B14		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
B15		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ ET0_ERXD3	MMC_D7-B		AN101
C1	AVSS1							
C2	AVCC1							
C3	VREFH0							

Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (3/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
62		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
63	TRSYNC	P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
64	TRDATA1	P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
65	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETR-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK/	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
67		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
68		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		
69		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
70		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
71		P75	CS5#	PO20	SCK11/RTS11/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
72		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			
73		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
74	VCC							
75		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
76	VSS							
77		P73	CS3#	PO16	ET0_WOL			
78		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
79		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
80		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
81		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
82		PB3	A11	MTIOC0A/MTIOC4A/ TIOC3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
83		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/ RTS6#/ SS4#/ SS6#/ ET0_RX_CLK/ REF50CK0			
84		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
85		P72	A19/CS2#		ET0_MDC			
86		P71	A18/CS1#		ET0_MDIO			

Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (4/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
87		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
88		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
89		PA6	A6	MTIC5V/MTCLKB/ GTETRIG-C/TIOCA2/ TMC13/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
90		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
91	VCC							
92		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
93	VSS							
94		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
95		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
96		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
97		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
98		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
99		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
100		P65	CS5#/CKE					
101		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
102		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/ TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
103	VCC							
104		P70	SDCLK					
105	VSS							
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
108		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3/ SS12#/ET0_ERXD3/	MMC_D7-B		AN101
109		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXD12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
110		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
111		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
112		P64	CS4#/WE#					
113		P63	CS3#/CAS#					
114		P62	CS2#/RAS#					
115		P61	CS1#/SDCS#					

Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
116	VSS							
117		P60	CS0#					
118	VCC							
119		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
120		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO-B	IRQ6	AN106
121		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
122		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
123		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
124		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
125		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
126		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
127		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
128		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
129		P91	A17		SCK7			AN115
130	VSS							
131		P90	A16		TXD7/SMOSI7/SSDA7			AN114
132	VCC							
133		P47					IRQ15- DS	AN007
134		P46					IRQ14- DS	AN006
135		P45					IRQ13- DS	AN005
136		P44					IRQ12- DS	AN004
137		P43					IRQ11-DS	AN003
138		P42					IRQ10- DS	AN002
139		P41					IRQ9-DS	AN001
140	VREFL0							
141		P40					IRQ8-DS	AN000
142	VREFH0							
143	AVCC0							
144		P07					IRQ15	ADTRG0#

Table 4.1 List of I/O Registers (Address Order) (6 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 2BE8h	EXDMA C	Cluster Buffer Register 2	CLSB2R	32	32	1, 2 BCLK		EXDMA C a
0008 2BEC h	EXDMA C	Cluster Buffer Register 3	CLSB3R	32	32	1, 2 BCLK		EXDMA C a
0008 2BF0h	EXDMA C	Cluster Buffer Register 4	CLSB4R	32	32	1, 2 BCLK		EXDMA C a
0008 2BF4h	EXDMA C	Cluster Buffer Register 5	CLSB5R	32	32	1, 2 BCLK		EXDMA C a
0008 2BF8h	EXDMA C	Cluster Buffer Register 6	CLSB6R	32	32	1, 2 BCLK		EXDMA C a
0008 2BFCh	EXDMA C	Cluster Buffer Register 7	CLSB7R	32	32	1, 2 BCLK		EXDMA C a
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1, 2 BCLK		Buses
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1, 2 BCLK		Buses
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1, 2 BCLK		Buses
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1, 2 BCLK		Buses
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1, 2 BCLK		Buses
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1, 2 BCLK		Buses
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1, 2 BCLK		Buses
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1, 2 BCLK		Buses
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1, 2 BCLK		Buses
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1, 2 BCLK		Buses
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1, 2 BCLK		Buses
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1, 2 BCLK		Buses
0008 3042h	BSC	CS4 Mode Register	CS4MOD	16	16	1, 2 BCLK		Buses
0008 3044h	BSC	CS4 Wait Control Register 1	CS4WCR1	32	32	1, 2 BCLK		Buses
0008 3048h	BSC	CS4 Wait Control Register 2	CS4WCR2	32	32	1, 2 BCLK		Buses
0008 3052h	BSC	CS5 Mode Register	CS5MOD	16	16	1, 2 BCLK		Buses
0008 3054h	BSC	CS5 Wait Control Register 1	CS5WCR1	32	32	1, 2 BCLK		Buses
0008 3058h	BSC	CS5 Wait Control Register 2	CS5WCR2	32	32	1, 2 BCLK		Buses
0008 3062h	BSC	CS6 Mode Register	CS6MOD	16	16	1, 2 BCLK		Buses
0008 3064h	BSC	CS6 Wait Control Register 1	CS6WCR1	32	32	1, 2 BCLK		Buses
0008 3068h	BSC	CS6 Wait Control Register 2	CS6WCR2	32	32	1, 2 BCLK		Buses
0008 3072h	BSC	CS7 Mode Register	CS7MOD	16	16	1, 2 BCLK		Buses
0008 3074h	BSC	CS7 Wait Control Register 1	CS7WCR1	32	32	1, 2 BCLK		Buses
0008 3078h	BSC	CS7 Wait Control Register 2	CS7WCR2	32	32	1, 2 BCLK		Buses
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1, 2 BCLK		Buses
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1, 2 BCLK		Buses
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1, 2 BCLK		Buses
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1, 2 BCLK		Buses
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK		Buses
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK		Buses
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK		Buses
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK		Buses
0008 3842h	BSC	CS4 Control Register	CS4CR	16	16	1, 2 BCLK		Buses
0008 384Ah	BSC	CS4 Recovery Cycle Register	CS4REC	16	16	1, 2 BCLK		Buses
0008 3852h	BSC	CS5 Control Register	CS5CR	16	16	1, 2 BCLK		Buses
0008 385Ah	BSC	CS5 Recovery Cycle Register	CS5REC	16	16	1, 2 BCLK		Buses
0008 3862h	BSC	CS6 Control Register	CS6CR	16	16	1, 2 BCLK		Buses
0008 386Ah	BSC	CS6 Recovery Cycle Register	CS6REC	16	16	1, 2 BCLK		Buses
0008 3872h	BSC	CS7 Control Register	CS7CR	16	16	1, 2 BCLK		Buses
0008 387Ah	BSC	CS7 Recovery Cycle Register	CS7REC	16	16	1, 2 BCLK		Buses

Table 4.1 List of I/O Registers (Address Order) (10 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 77A6h	ICU	Software Configurable Interrupt B Select Register 166	SLIBR166	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77A7h	ICU	Software Configurable Interrupt B Select Register 167	SLIBR167	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77A8h	ICU	Software Configurable Interrupt B Select Register 168	SLIBR168	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77A9h	ICU	Software Configurable Interrupt B Select Register 169	SLIBR169	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77AAh	ICU	Software Configurable Interrupt B Select Register 170	SLIBR170	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77ABh	ICU	Software Configurable Interrupt B Select Register 171	SLIBR171	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77ACh	ICU	Software Configurable Interrupt B Select Register 172	SLIBR172	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77ADh	ICU	Software Configurable Interrupt B Select Register 173	SLIBR173	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77AEh	ICU	Software Configurable Interrupt B Select Register 174	SLIBR174	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77AFh	ICU	Software Configurable Interrupt B Select Register 175	SLIBR175	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B0h	ICU	Software Configurable Interrupt B Select Register 176	SLIBR176	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B1h	ICU	Software Configurable Interrupt B Select Register 177	SLIBR177	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B2h	ICU	Software Configurable Interrupt B Select Register 178	SLIBR178	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B3h	ICU	Software Configurable Interrupt B Select Register 179	SLIBR179	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B4h	ICU	Software Configurable Interrupt B Select Register 180	SLIBR180	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B5h	ICU	Software Configurable Interrupt B Select Register 181	SLIBR181	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B6h	ICU	Software Configurable Interrupt B Select Register 182	SLIBR182	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B7h	ICU	Software Configurable Interrupt B Select Register 183	SLIBR183	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B8h	ICU	Software Configurable Interrupt B Select Register 184	SLIBR184	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77B9h	ICU	Software Configurable Interrupt B Select Register 185	SLIBR185	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77BAh	ICU	Software Configurable Interrupt B Select Register 186	SLIBR186	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77BBh	ICU	Software Configurable Interrupt B Select Register 187	SLIBR187	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77BCh	ICU	Software Configurable Interrupt B Select Register 188	SLIBR188	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77BDh	ICU	Software Configurable Interrupt B Select Register 189	SLIBR189	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77BEh	ICU	Software Configurable Interrupt B Select Register 190	SLIBR190	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77BFh	ICU	Software Configurable Interrupt B Select Register 191	SLIBR191	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77C0h	ICU	Software Configurable Interrupt B Select Register 192	SLIBR192	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77C1h	ICU	Software Configurable Interrupt B Select Register 193	SLIBR193	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77C2h	ICU	Software Configurable Interrupt B Select Register 194	SLIBR194	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77C3h	ICU	Software Configurable Interrupt B Select Register 195	SLIBR195	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77C4h	ICU	Software Configurable Interrupt B Select Register 196	SLIBR196	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77C5h	ICU	Software Configurable Interrupt B Select Register 197	SLIBR197	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77C6h	ICU	Software Configurable Interrupt B Select Register 198	SLIBR198	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77C7h	ICU	Software Configurable Interrupt B Select Register 199	SLIBR199	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77C8h	ICU	Software Configurable Interrupt B Select Register 200	SLIBR200	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (11 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 77C9h	ICU	Software Configurable Interrupt B Select Register 201	SLIBR201	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77CAh	ICU	Software Configurable Interrupt B Select Register 202	SLIBR202	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77CBh	ICU	Software Configurable Interrupt B Select Register 203	SLIBR203	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77CCh	ICU	Software Configurable Interrupt B Select Register 204	SLIBR204	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77CDh	ICU	Software Configurable Interrupt B Select Register 205	SLIBR205	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77CEh	ICU	Software Configurable Interrupt B Select Register 206	SLIBR206	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77CFh	ICU	Software Configurable Interrupt B Select Register 207	SLIBR207	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7830h	ICU	Group AL0 Interrupt Request Register	GRPAL0	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7834h	ICU	Group AL1 Interrupt Request Register	GRPAL1	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7870h	ICU	Group AL0 Interrupt Request Enable Register	GENAL0	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7874h	ICU	Group AL1 Interrupt Request Enable Register	GENAL1	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7900h	ICU	Software Configurable Interrupt A Request Register 0	PIAR0	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7901h	ICU	Software Configurable Interrupt A Request Register 1	PIAR1	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7902h	ICU	Software Configurable Interrupt A Request Register 2	PIAR2	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7903h	ICU	Software Configurable Interrupt A Request Register 3	PIAR3	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7904h	ICU	Software Configurable Interrupt A Request Register 4	PIAR4	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7905h	ICU	Software Configurable Interrupt A Request Register 5	PIAR5	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7906h	ICU	Software Configurable Interrupt A Request Register 6	PIAR6	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7907h	ICU	Software Configurable Interrupt A Request Register 7	PIAR7	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7908h	ICU	Software Configurable Interrupt A Request Register 8	PIAR8	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7909h	ICU	Software Configurable Interrupt A Request Register 9	PIAR9	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 790Ah	ICU	Software Configurable Interrupt A Request Register A	PIARA	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 790Bh	ICU	Software Configurable Interrupt A Request Register B	PIARB	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D0h	ICU	Software Configurable Interrupt A Select Register 208	SLIAR208	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D1h	ICU	Software Configurable Interrupt A Select Register 209	SLIAR209	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D2h	ICU	Software Configurable Interrupt A Select Register 210	SLIAR210	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D3h	ICU	Software Configurable Interrupt A Select Register 211	SLIAR211	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D4h	ICU	Software Configurable Interrupt A Select Register 212	SLIAR212	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D5h	ICU	Software Configurable Interrupt A Select Register 213	SLIAR213	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D6h	ICU	Software Configurable Interrupt A Select Register 214	SLIAR214	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D7h	ICU	Software Configurable Interrupt A Select Register 215	SLIAR215	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D8h	ICU	Software Configurable Interrupt A Select Register 216	SLIAR216	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D9h	ICU	Software Configurable Interrupt A Select Register 217	SLIAR217	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DAh	ICU	Software Configurable Interrupt A Select Register 218	SLIAR218	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DBh	ICU	Software Configurable Interrupt A Select Register 219	SLIAR219	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (14 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 811Ah	TPU0	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Ch	TPU0	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Eh	TPU0	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8120h	TPU1	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8121h	TPU1	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8122h	TPU1	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8124h	TPU1	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8125h	TPU1	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8126h	TPU1	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8128h	TPU1	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 812Ah	TPU1	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8130h	TPU2	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8131h	TPU2	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8132h	TPU2	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8134h	TPU2	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8135h	TPU2	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8136h	TPU2	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8138h	TPU2	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 813Ah	TPU2	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8140h	TPU3	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81E6h	PPG0	PPG Output Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG Output Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E8h	PPG0	Next Data Enable Registers H	NDERH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E9h	PPG0	Next Data Enable Registers L	NDERL	8	8	2, 3 PCLKB	2 ICLK	PPG

Table 4.1 List of I/O Registers (Address Order) (24 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIf
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C6h	SCI6	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIf
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIf
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E0h	SCI7	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E1h	SCI7	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E2h	SCI7	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E3h	SCI7	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E4h	SCI7	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf
0008 A0E5h	SCI7	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIf

Table 4.1 List of I/O Registers (Address Order) (34 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C289h	SYSTEM	Deep Standby Interrupt Flag Register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Bh	SYSTEM	Deep Standby Interrupt Edge Register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Dh	SYSTEM	Deep Standby Interrupt Edge Register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-Speed On-Chip Oscillator Power Supply Control Register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Registers 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	RTCd

Table 4.1 List of I/O Registers (Address Order) (51 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 218Ah	GPT1	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 218Ch	GPT1	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 218Eh	GPT1	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2190h	GPT1	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2192h	GPT1	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2194h	GPT1	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2196h	GPT1	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2198h	GPT1	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 219Ah	GPT1	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 219Ch	GPT1	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 219Eh	GPT1	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21A0h	GPT1	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21A4h	GPT1	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21A8h	GPT1	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21B0h	GPT1	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2200h	GPT2	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2204h	GPT2	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2206h	GPT2	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2208h	GPT2	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 220Ch	GPT2	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 220Eh	GPT2	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2210h	GPT2	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2212h	GPT2	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2214h	GPT2	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2216h	GPT2	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2218h	GPT2	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 221Ch	GPT2	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 221Eh	GPT2	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2220h	GPT2	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2224h	GPT2	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa

Table 4.1 List of I/O Registers (Address Order) (55 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4890h	EPTPC 0	SYNFP Reception Filter Register 1	SYRFL1R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4894h	EPTPC 0	SYNFP Reception Filter Register 2	SYRFL2R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4898h	EPTPC 0	SYNFP Transmission Enable Register	SYTRENr	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A0h	EPTPC 0	Master Clock ID Register	MTCIDU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A4h	EPTPC 0	Master Clock ID Register	MTCIDL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A8h	EPTPC 0	Master Clock Port Number Register	MTPID	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C0h	EPTPC 0	SYNFP Transmission Interval Setting Register	SYTLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C4h	EPTPC 0	SYNFP Received logMessageInterval Value Indication Register	SYRLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C8h	EPTPC 0	offsetFromMaster Value Register	OFMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48CCh	EPTPC 0	offsetFromMaster Value Register	OFMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48D0h	EPTPC 0	meanPathDelay Value Register	MPDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48D4h	EPTPC 0	meanPathDelay Value Register	MPDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E0h	EPTPC 0	grandmasterPriority Field Setting Register	GMPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E4h	EPTPC 0	grandmasterClockQuality Field Setting Register	GMCQR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E8h	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48ECh	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48F0h	EPTPC 0	currentUtcOffset/timeSource Field Setting Register	CUOTSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48F4h	EPTPC 0	stepsRemoved Field Setting Register	SRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4900h	EPTPC 0	PTP-primary Message Destination MAC Address Setting Registers	PPMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4904h	EPTPC 0	PTP-primary Message Destination MAC Address Setting Registers	PPMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4908h	EPTPC 0	PTP-pdelay Message MAC Address Setting Registers	PDMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 490Ch	EPTPC 0	PTP-pdelay Message MAC Address Setting Registers	PDMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4910h	EPTPC 0	PTP Message EtherType Setting Register	PETYPER	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4920h	EPTPC 0	PTP-primary Message Destination IP Address Setting Register	PPIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4924h	EPTPC 0	PTP-pdelay Message Destination IP Address Setting Register	PDIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4928h	EPTPC 0	PTP event Message TOS Setting Register	PETOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 492Ch	EPTPC 0	PTP general Message TOS Setting Register	PGTOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4930h	EPTPC 0	PTP-primary Message TTL Setting Register	PPTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4934h	EPTPC 0	PTP-pdelay Message TTL Setting Register	PDTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4938h	EPTPC 0	PTP event Message UDP Destination Port Number Setting Register	PEUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 493Ch	EPTPC 0	PTP general Message UDP Destination Port Number Setting Register	PGUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa

Table 5.9 Operating Frequency (Low-Speed Operating Mode 2)

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	32	—	264	kHz
	Peripheral module clock (PCLKA)			—	—	264	
	Peripheral module clock (PCLKB)			—	—	264	
	Peripheral module clock (PCLKC)* ¹			—	—	264	
	Peripheral module clock (PCLKD)* ¹			—	—	264	
	Flash-IF clock (FCLK)			32	—	264	
	External bus clock (BCLK)	Packages with 177 to 144 pins only		—	—	264	
		Package with 100 pins only		—	—	264	
	BCLK pin output	Packages with 177 to 144 pins only		—	—	264	
		Package with 100 pins only		—	—	264	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	264	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	264	

Note 1. The 12-bit A/D converter cannot be used.

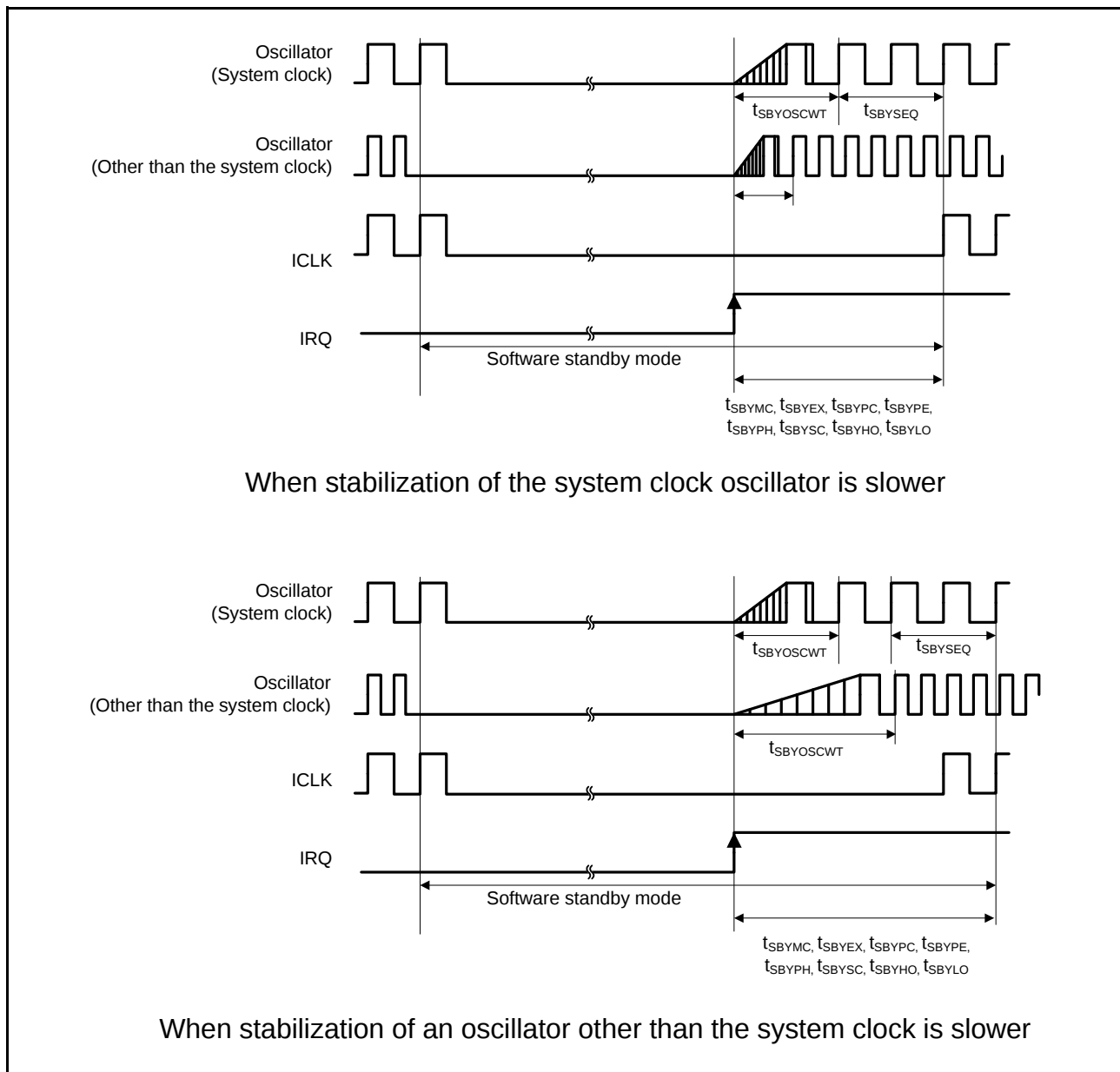


Figure 5.12 Software Standby Mode Cancellation Timing

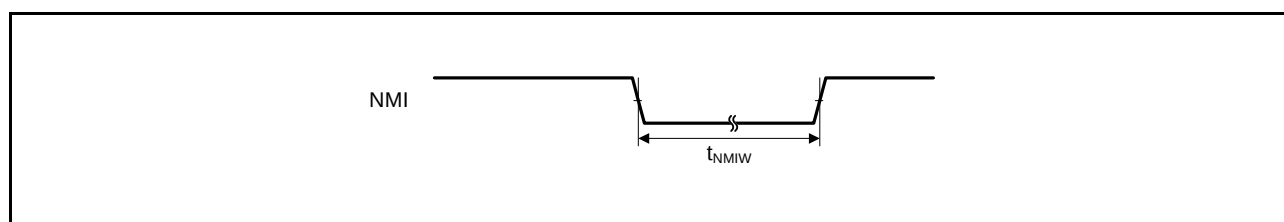
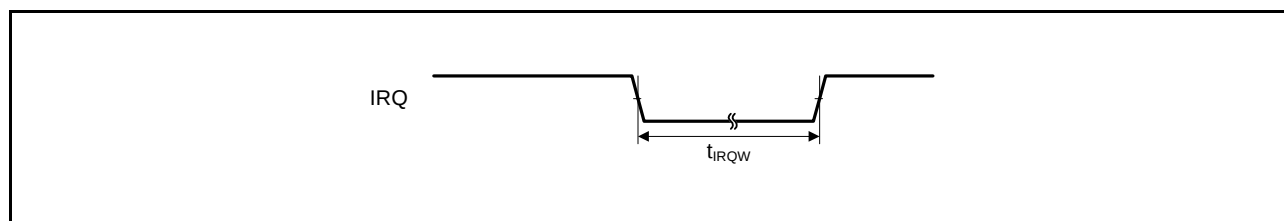
5.3.4 Control Signal Timing

Table 5.20 Control Signal Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PLCKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{PBcyc} \times 2 \leq 200$ ns, Figure 5.14
		$t_{PBcyc} \times 2$	—	—	ns	$t_{PBcyc} \times 2 > 200$ ns, Figure 5.14
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{PBcyc} \times 2 \leq 200$ ns, Figure 5.15
		$t_{PBcyc} \times 2$	—	—	ns	$t_{PBcyc} \times 2 > 200$ ns, Figure 5.15

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.14 NMI Interrupt Input Timing****Figure 5.15 IRQ Interrupt Input Timing**

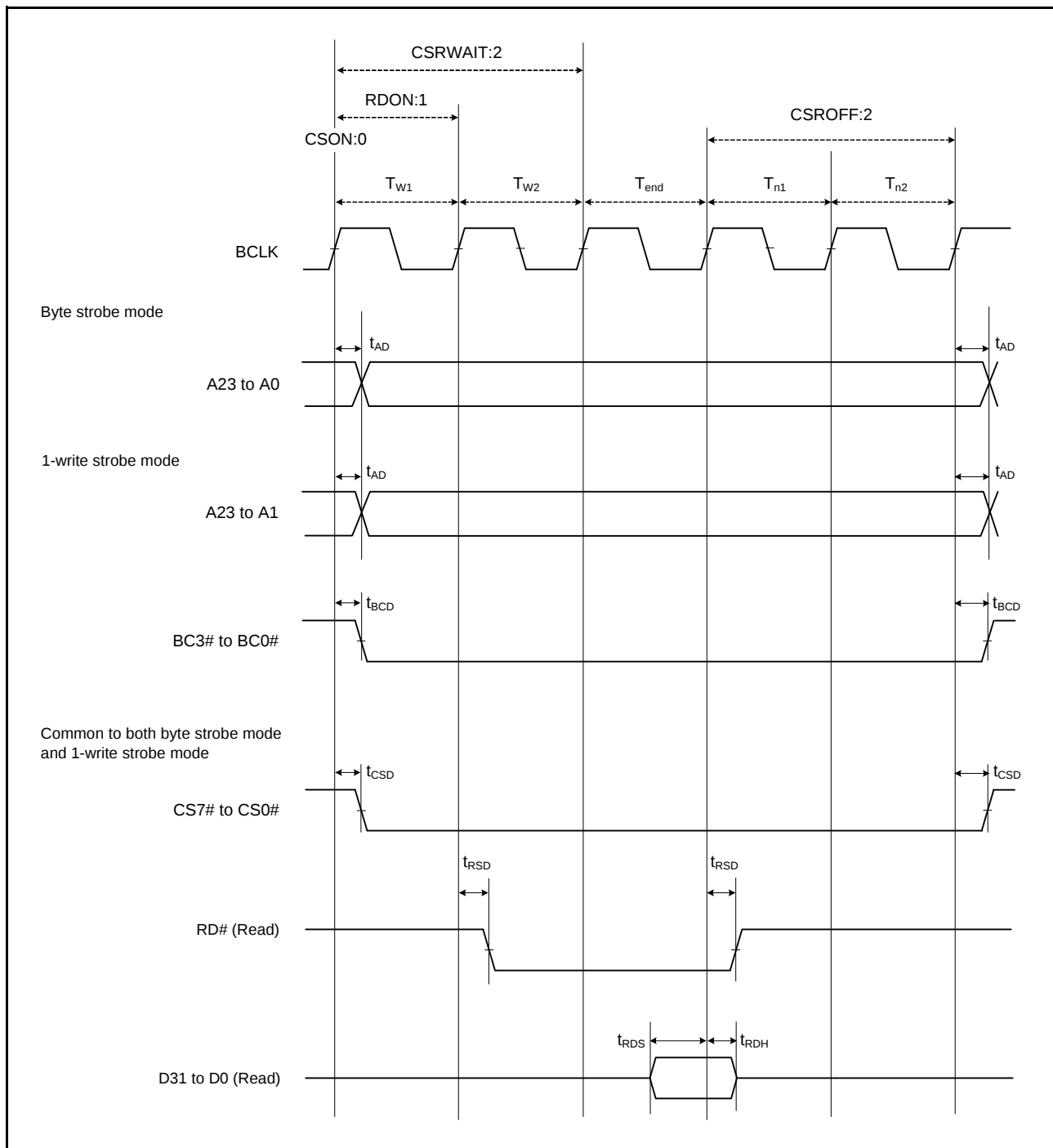
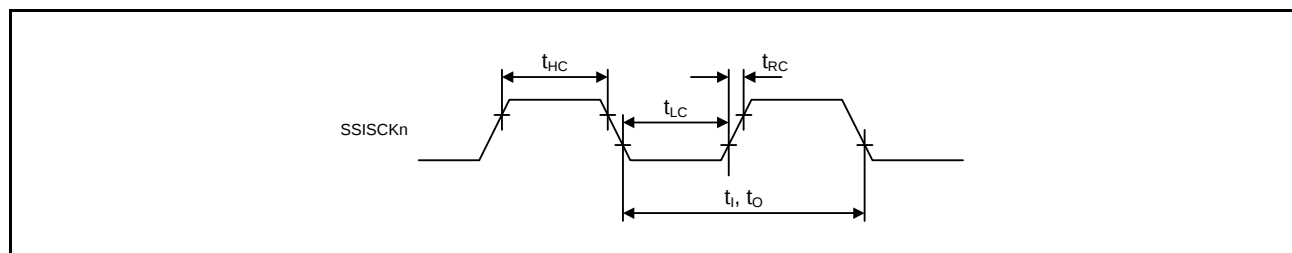
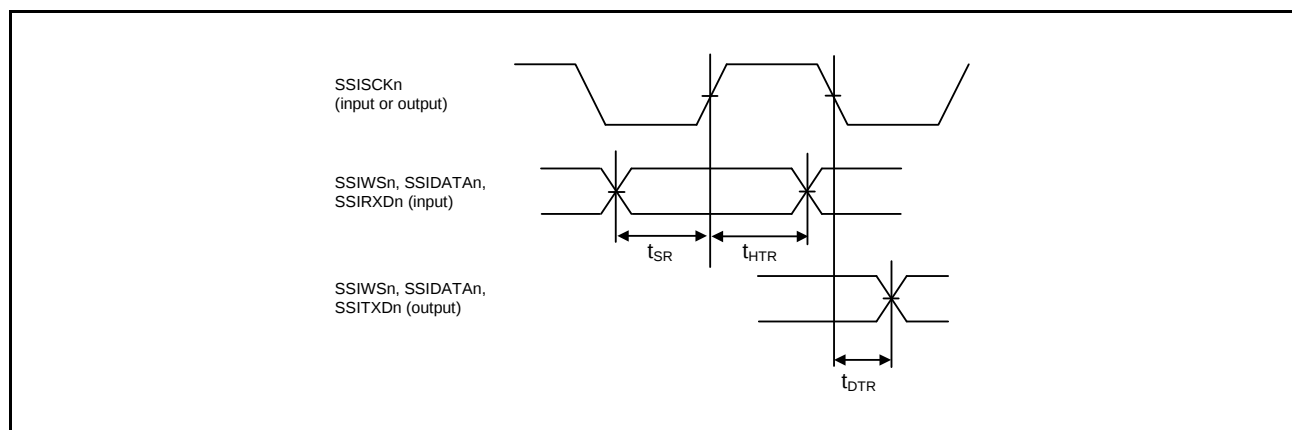


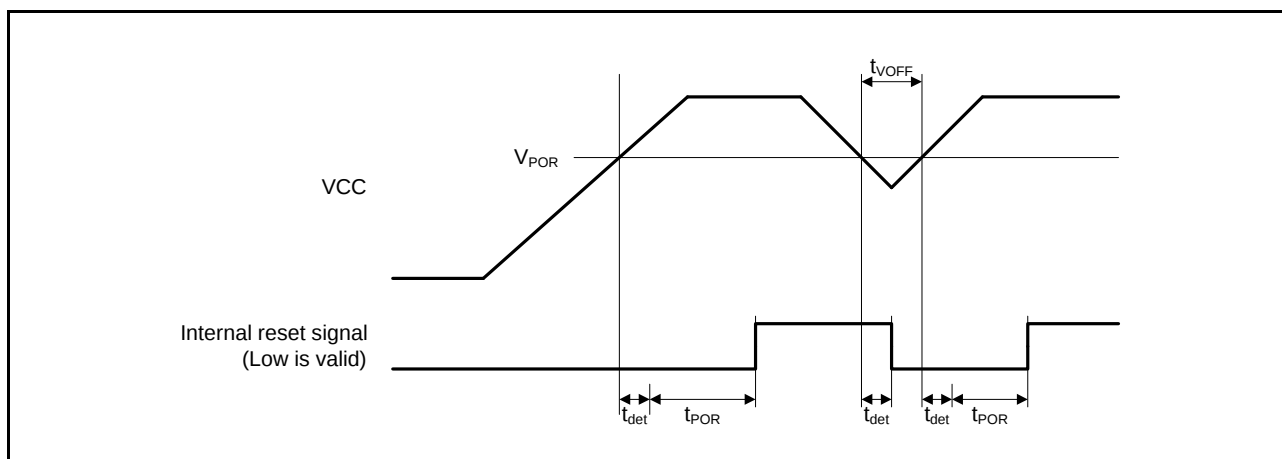
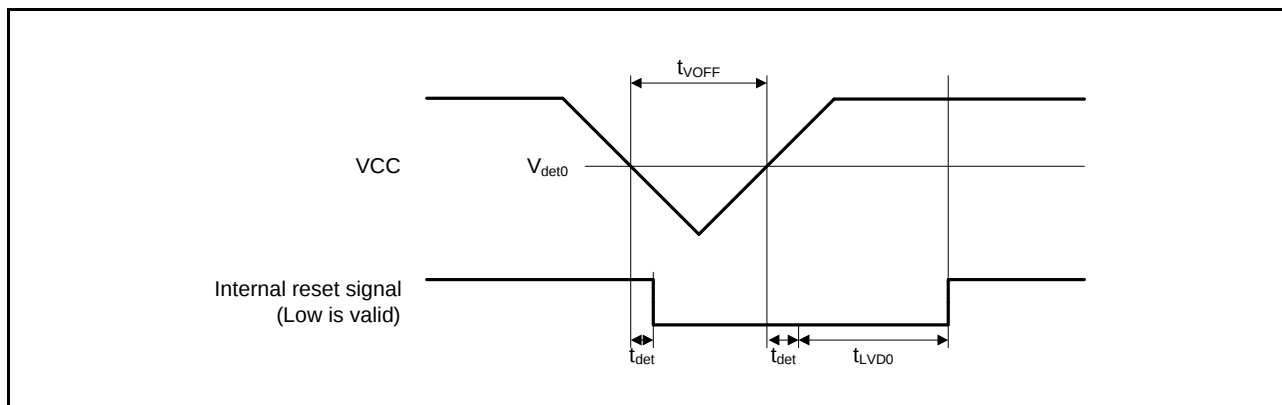
Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

Table 5.38 Serial Sound Interface Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
SSI	AUDIO_CLK input frequency	t_{AUDIO}	—	50	MHz
	Output clock cycle	t_O	150	64000	ns
	Input clock cycle	t_I	150	64000	ns
	Clock high level	t_{HC}	60	—	ns
	Clock low level	t_{LC}	60	—	ns
	Clock rising time	t_{RC}	—	25	ns
	Data delay time	t_{DTR}	—5	25	ns
	Setup time	t_{SR}	25	—	ns
	Hold time	t_{HTR}	25	—	ns
	WS change edge SSIDATA output delay	t_{DTRW}	—	25	ns

**Figure 5.57 Clock Input/Output Timing****Figure 5.58 Transmit/Receive Timing (SSISCKn Rising Synchronous)**

**Figure 5.83 Power-on Reset Timing****Figure 5.84 Voltage Detection Circuit Timing (V_{det0})**

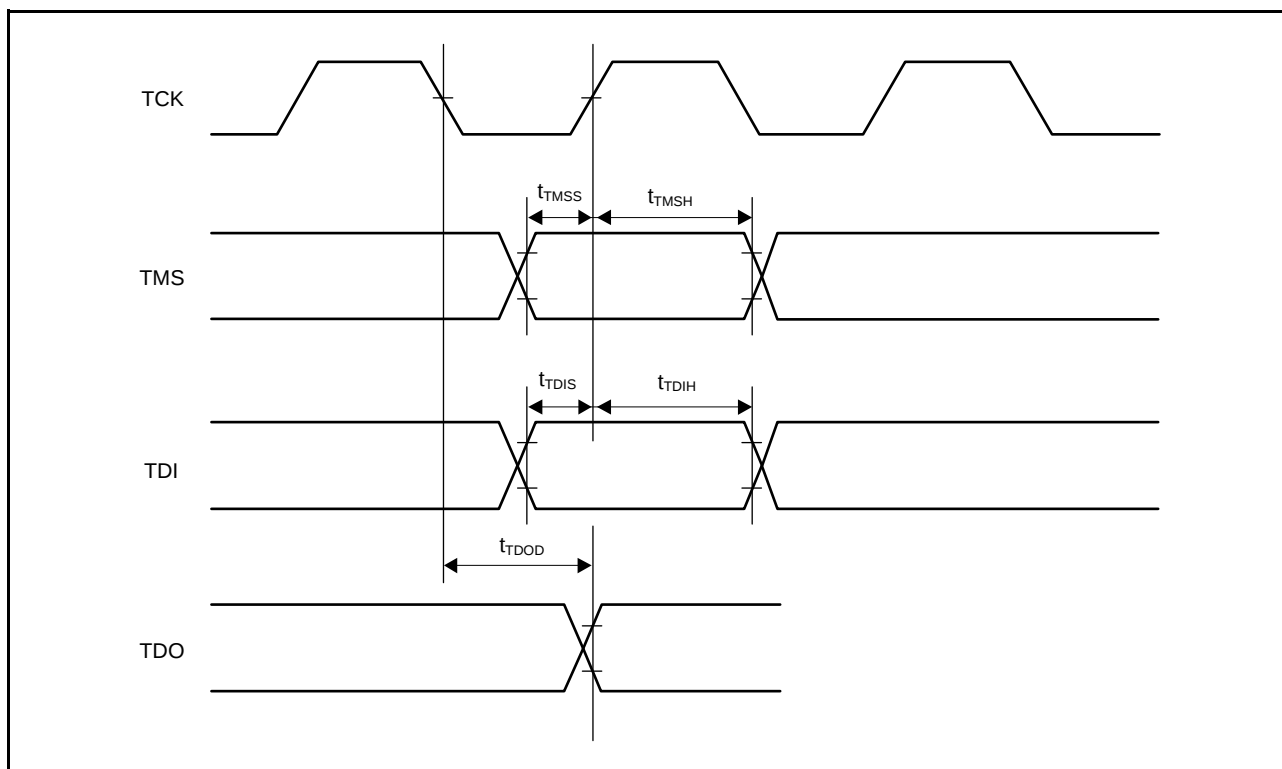


Figure 5.92 Boundary Scan Input/Output Timing