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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mg hdfc-v0

Table 1.1 Outline of Specifications (5/10)

Classification	Module/Function	Description
Timers	General PWM timer (GPTa)	• 16 bits × 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Four clock sources independently selectable for all channels (PCLKA/1, PCLKA/4, PCLKA/8, PCLKA/16) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • Digital filter function for signals on the input capture and external trigger pins • Event linking by the ELC
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units • Pulse output with the MTU or TPU output as a trigger • Maximum of 32 pulse-output possible
	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCd)	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTa)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC

Table 1.2 Comparison of Functions for Different Packages (2/2)

Functions	RX71M Group		
Package	177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins
DES	Available		
SHA	Available		
RNG	Available		
Event link controller	Available		

Table 1.3 List of Products (3/3)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX71M	R5F571MFCDLK	PTLG0145KA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDLK	PTLG0145KA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDLK	PTLG0145KA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDLK	PTLG0145KA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDLJ	PTLG0100JA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDLJ	PTLG0100JA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDLJ	PTLG0100JA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDLJ	PTLG0100JA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDLJ	PTLG0100JA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDLJ	PTLG0100JA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDLJ	PTLG0100JA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDLJ	PTLG0100JA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDLJ	PTLG0100JA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDLJ	PTLG0100JA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDLJ	PTLG0100JA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDLJ	PTLG0100JA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDLJ	PTLG0100JA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDLJ	PTLG0100JA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDLJ	PTLG0100JA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDLJ	PTLG0100JA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available

Note 1. Under planning

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCiG, SCiH, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
J14		PA7	A7	TIOCB2/PO23	MISOA-B/ ET0_WOL			
J15		PA6	A6	MTIC5V/MTCLKB/ GTETR-G-C/TIOCA2/ TMC13/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
K1		P33	EDREQ1	MTIOC0D/TIOC0D/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOU/RTICIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/ SSCL1			
K4	TCK	PF1			SCK1			
K12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
K13		P71	A18/CS1#		ET0_MDIO			
K14	VCC							
K15		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
L1		P31		MTIOC4D/TMC12/ PO9/RTIC1	CTS1#/RTS1#/ SS1#/ET1_MDC/ SSLB0-A		IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/ PO8/RTIC0/POE8#	RXD1/SMISO1/ SSCL1/ET1_MDIO/ MISOB-A		IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/ SSDA1			
L4		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ SSIDATA1	HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
L15		P72	A19/CS2#		ET0_MDC			
M1		P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/ET1_WOL/ RSPCKB-A			
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ ET1_EXOUT/ MOSIB-A			
M3		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
M4		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (4/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
K4		P15		MTIOC0B/MTCLKB/ GTETR-B/TIOC2B/ TCLKB/TMC12/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1	PIXD0	IRQ5	
K5	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
K6		P53	BCLK					
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
K8	VCC							
K9	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
K10		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
K11		PB7	A15	MTIOC3B/TIOC5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
K12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
K13		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
L1		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1	HSYNC		ADTRG0#
L2		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SSO#/ SSDA3/SSISCK0	PIXD7		
L3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
L4		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
L5		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
L6		P56	EDACK1	MTIOC3C/TIOCA1				
L7		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
L8	TRCLK	P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
L9		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
L10		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETR-D/TMC11/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
L11		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
L12		P73	CS3#	PO16	ET0_WOL			
L13	VSS							
M1		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK	PIXD6		

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (3/4)

Pin Number	Power Supply Clock System Contro	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SClg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
56		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
57		PB3	A11	MTIOC0A/MTIOC4A/ TIOC03/TCLKD/ TMO0/PO27/POE11#	SCK6/ET0_RX_ER/ RMII0_RX_ER			
58		PB2	A10	TIOCC3/TCLKC/ PO26	CTS6#/RTS6#SS6#/ ET0_RX_CLK/ REF50CK0			
59		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
60	VCC							
61		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
62	VSS							
63		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
64		PA6	A6	MTIC5V/MTCLKB/ GTETRIG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
65		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
66		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
67		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
68		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
69		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
70		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
71		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
72		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/ TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
75		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3	MMC_D7-B		AN101
76		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXD12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
77		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
78		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
79		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/ QMI-B	IRQ7	AN107

Table 4.1 List of I/O Registers (Address Order) (2 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK		Clock Generation Circuit
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK		Clock Generation Circuit
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK		Clock Generation Circuit
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK		Low Power Consumption
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK		Low Power Consumption
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00A3h	SYSTEM	Sub-Clock Oscillator Wait Control Register	SOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK		Resets
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LDVA
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK		LDVA
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK		LDVA
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK		LDVA
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function
0008 1200h	RAM	RAM Operating Mode Control Register	RAMMODE	8	8	2 ICLK		RAM
0008 1201h	RAM	RAM Error Status Register	RAMSTS	8	8	2 ICLK		RAM
0008 1204h	RAM	RAM Protection Register	RAMPPCR	8	8	2 ICLK		RAM
0008 1208h	RAM	RAM Error Address Capture Register	RAMECAD	32	32	2 ICLK		RAM
0008 12C0h	ECCRAM	ECCRAM Operating Mode Control Register	ECCRAMMODE	8	8	2 ICLK		RAM
0008 12C1h	ECCRAM	ECCRAM 2-Bit Error Status Register	ECCRAM2STS	8	8	2 ICLK		RAM
0008 12C2h	ECCRAM	ECCRAM 1-Bit Error Information Update Enable Register	ECCRAM1STSEN	8	8	2 ICLK		RAM
0008 12C3h	ECCRAM	ECCRAM 1-Bit Error Status Register	ECCRAM1STS	8	8	2 ICLK		RAM
0008 12C4h	ECCRAM	ECCRAM Protection Register	ECCRAMPCR	8	8	2 ICLK		RAM
0008 12C8h	ECCRAM	ECCRAM 2-Bit Error Address Capture Register	ECCRAM2ECAD	32	32	2 ICLK		RAM
0008 12CCh	ECCRAM	ECCRAM 1-Bit Error Address Capture Register	ECCRAM1ECAD	32	32	2 ICLK		RAM
0008 12D0h	ECCRAM	ECCRAM Protection Register 2	ECCRAMPCR2	8	8	2 ICLK		RAM
0008 12D4h	ECCRAM	ECCRAM Test Control Register	ECCRAMETS	8	8	2 ICLK		RAM
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK		Buses
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK		Buses

Table 4.1 List of I/O Registers (Address Order) (13 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
0008 79FFh	ICU	Software Configurable Interrupt A Select Register 255	SLIAR255	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7A00h	ICU	Software Configurable Interrupt Selection Write Protect Register	SLIPRCR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUA
0008 7A01h	ICU	EXDMAC Start Interrupt Select Register	SELEXDR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUA
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSPTPR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8040h	DA	D/A Data Register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	R12DA
0008 8042h	DA	D/A Data Register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK	R12DA
0008 8044h	DA	D/A Control Register	DACR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8045h	DA	DADRM Format Select Register	DADPR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8046h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8048h	DA	D/A Output Amplifier Control Register	DAAMPCR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8100h	TPUA	Timer Start Register	TSTR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8101h	TPUA	Timer Synchronous Register	TSYR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8108h	TPU0	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8109h	TPU1	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Ah	TPU2	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Bh	TPU3	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Ch	TPU4	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Dh	TPU5	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8110h	TPU0	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8111h	TPU0	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8112h	TPU0	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8113h	TPU0	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8114h	TPU0	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8115h	TPU0	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8116h	TPU0	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8118h	TPU0	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa

Table 4.1 List of I/O Registers (Address Order) (18 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 907Ch	S12AD	A/D Sample-and-Hold Circuit Operating Mode Select Register	ADSHMSR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9084h	S12AD	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9086h	S12AD	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9090h	S12AD	A/D Compare Control Register	ADCMPCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9094h	S12AD	A/D Compare Channel Select Register 0	ADCMPANSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9098h	S12AD	A/D Compare Level Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 909Ch	S12AD	A/D Compare Data Register 0	ADCMPCR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 909Eh	S12AD	A/D Compare Data Register 1	ADCMPCR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 90A0h	S12AD	A/D Compare Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9100h	S12AD1	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9104h	S12AD1	A/D Channel Select Register A0	ADANSA0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9106h	S12AD1	A/D Channel Select Register A1	ADANSA1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9108h	S12AD1	A/D-Converted Value Addition/Average Mode Select Register 0	ADADS0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 910Ah	S12AD1	A/D-Converted Value Addition/Average Mode Select Register 1	ADADS1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 910Ch	S12AD1	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 910Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9110h	S12AD1	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9112h	S12AD1	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9114h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9116h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9118h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 911Ah	S12AD1	A/D Temperature Sensor Data Register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 911Ch	S12AD1	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 911Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9120h	S12AD1	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9122h	S12AD1	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9124h	S12AD1	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9126h	S12AD1	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9128h	S12AD1	A/D Data Register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 912Ah	S12AD1	A/D Data Register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 912Ch	S12AD1	A/D Data Register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 912Eh	S12AD1	A/D Data Register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9130h	S12AD1	A/D Data Register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9132h	S12AD1	A/D Data Register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9134h	S12AD1	A/D Data Register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9136h	S12AD1	A/D Data Register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9138h	S12AD1	A/D Data Register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Ah	S12AD1	A/D Data Register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Ch	S12AD1	A/D Data Register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Eh	S12AD1	A/D Data Register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9140h	S12AD1	A/D Data Register 16	ADDR16	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9142h	S12AD1	A/D Data Register 17	ADDR17	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9144h	S12AD1	A/D Data Register 18	ADDR18	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9146h	S12AD1	A/D Data Register 19	ADDR19	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9148h	S12AD1	A/D Data Register 20	ADDR20	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9160h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK	S12ADC

Table 4.1 List of I/O Registers (Address Order) (27 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B131h	ELC	Event Link Setting Register 33	ELSR33	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B133h	ELC	Event Link Setting Register 35	ELSR35	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B134h	ELC	Event Link Setting Register 36	ELSR36	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B135h	ELC	Event Link Setting Register 37	ELSR37	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B136h	ELC	Event Link Setting Register 38	ELSR38	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B139h	ELC	Event Link Setting Register 41	ELSR41	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Ah	ELC	Event Link Setting Register 42	ELSR42	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Bh	ELC	Event Link Setting Register 43	ELSR43	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Ch	ELC	Event Link Setting Register 44	ELSR44	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Dh	ELC	Event Link Setting Register 45	ELSR45	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Fh	ELC	Event Link Option Setting Register F	ELOPF	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B141h	ELC	Event Link Option Setting Register H	ELOPH	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B142h	ELC	Event Link Option Setting Register I	ELOPI	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B143h	ELC	Event Link Option Setting Register J	ELOPJ	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B309h	SCI12	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Ah	SCI12	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Bh	SCI12	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Ch	SCI12	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B321h	SCI12	Control Register 0	CR0	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B322h	SCI12	Control Register 1	CR1	8	8	2, 3 PCLKB	2 ICLK	SCIh

Table 4.1 List of I/O Registers (Address Order) (34 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C289h	SYSTEM	Deep Standby Interrupt Flag Register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Bh	SYSTEM	Deep Standby Interrupt Edge Register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Dh	SYSTEM	Deep Standby Interrupt Edge Register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-Speed On-Chip Oscillator Power Supply Control Register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Registers 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	RTCd

Table 4.1 List of I/O Registers (Address Order) (35 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C428h	RTC	RTC Control Register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ah	RTC	Frequency Register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ch	RTC	Frequency Register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C440h	RTC	Time Capture Control Register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C442h	RTC	Time Capture Control Register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C444h	RTC	Time Capture Control Register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	Second Capture Register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	BCNT0 Capture Register 0	BCNT0CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	Minute Capture Register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	BCNT1 Capture Register 0	BCNT1CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	Hour Capture Register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	BCNT2 Capture Register 0	BCNT2CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	Date Capture Register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	BCNT3 Capture Register 0	BCNT3CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ch	RTC	Month Capture Register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C462h	RTC	Second Capture Register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C462h	RTC	BCNT0 Capture Register 1	BCNT0CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C464h	RTC	Minute Capture Register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C464h	RTC	BCNT1 Capture Register 1	BCNT1CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C466h	RTC	Hour Capture Register 1	RHRCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C466h	RTC	BCNT2 Capture Register 1	BCNT2CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ah	RTC	Date Capture Register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ah	RTC	BCNT3 Capture Register 1	BCNT3CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ch	RTC	Month Capture Register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C472h	RTC	Second Capture Register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C472h	RTC	BCNT0 Capture Register 2	BCNT0CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C474h	RTC	Minute Capture Register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C474h	RTC	BCNT1 Capture Register 2	BCNT1CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C476h	RTC	Hour Capture Register 2	RHRCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C476h	RTC	BCNT2 Capture Register 2	BCNT2CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ah	RTC	Date Capture Register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ah	RTC	BCNT3 Capture Register 2	BCNT3CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ch	RTC	Month Capture Register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C4C0h	POE3	Input Level Control/Status Register 1	ICSR1	16	16	2, 3 PCLKB	2 ICLK	POE3
0008 C4C2h	POE3	Output Level Control/Status Register 1	OCSR1	16	16	2, 3 PCLKB	2 ICLK	POE3

Table 4.1 List of I/O Registers (Address Order) (63 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
000D 0456h	USBA	USB Request Value Register	USBVAL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0458h	USBA	USB Request Index Register	USBINDX	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 045Ah	USBA	USB Request Length Register	USBLENG	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 045Ch	USBA	DCP Configuration Register	DCPCFG	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 045Eh	USBA	DCP Maximum Packet Size Register	DCPMAXP	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0460h	USBA	DCP Control Register	DCPCTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0464h	USBA	Pipe Window Select Register	PIPESEL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0468h	USBA	Pipe Configuration Register	PIPECFG	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 046Ah	USBA	Pipe Buffer Register	PIPEBUF	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 046Ch	USBA	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 046Eh	USBA	Pipe Cycle Control Register	PIPEPERI	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa

which writing proceed) or data flash memory during program execution in the code flash memory.

Note 6. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.

Note 7. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 2.7 to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,

VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,

VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,

T_a = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current*1	During 12-bit A/D conversion (unit 0)		I _{ACC}	—	0.7	1.1	mA	IAVCC0_AD
	During 12-bit A/D conversion (unit 0) with the channel-dedicated sample-and-hold circuits for 3 channels operating			—	2.2	3.3	mA	IAVCC0_AD+SH
	During 12-bit A/D conversion (unit 1)			—	0.7	1.1	mA	IAVCC1_AD
	During 12-bit A/D conversion (unit 1) with the temperature sensor operating			—	0.7	2.3	mA	IAVCC1_AD+TEMP
	During D/A conversion (per unit)	Without AMP output		—	0.24	0.4	mA	IAVCC1_DA
		With AMP output		—	0.45	0.7	mA	
	Waiting for A/D, D/A, or temperature sensor conversion (all units)			—	0.9	1.6	mA	IAVCC0 + IAVCC1
	A/D, D/A converter, temperature sensor in standby mode (all units)			—	1.3	5.0	μA	IAVCC0 + IAVCC1
Reference power supply current	During 12-bit A/D conversion (unit 0)		I _{REFH}	—	70	120	μA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.5	μA	IVREFH0
	12-bit A/D converter in standby mode (unit 0)			—	0.07	0.5	μA	IVREFH0
USB operating current	Low speed	USBb	I _{CCUSBLS}	—	3.5	6.5	mA	VCC_USB
		USBA		—	10.5	13.5	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 0)
		USBA		—	2.8	3.6	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 1)
	Full speed	USBb	I _{CCUSBFS}	—	4.0	10.0	mA	VCC_USB
		USBA		—	14.0	22.0	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 0)
		USBA		—	6.5	13.0	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 1)
	High speed	USBA	I _{CCUSBHS}	—	50.0	65.0	mA	VCC_USBA = AVCC_USBA
	Standby mode (direct power down)	USBA	I _{CCUSBSBY}	—	0.1	3.0	μA	VCC_USBA = AVCC_USBA
RAM standby voltage			V _{RAM}	2.7	—	—	V	
VCC rising gradient			SrVCC	8.4	—	20000	μs/V	
VCC falling gradient*2			SfVCC	8.4	—	—	μs/V	

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D conversion (unit 1) and D/A conversion.

Note 2. This applies when V_{BATT} is used.

Table 5.15 HOCO Clock Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,

$V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,

$V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,

$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.61	16	16.39	MHz	$-20^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$
		17.56	18	18.44	MHz	
		19.52	20	20.48	MHz	
		15.52	16	16.48	MHz	$-40^{\circ}\text{C} \leq T_a < -20^{\circ}\text{C}$
		17.46	18	18.54	MHz	
		19.40	20	20.60	MHz	
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	μs	Figure 5.8
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150	μs	Figure 5.9

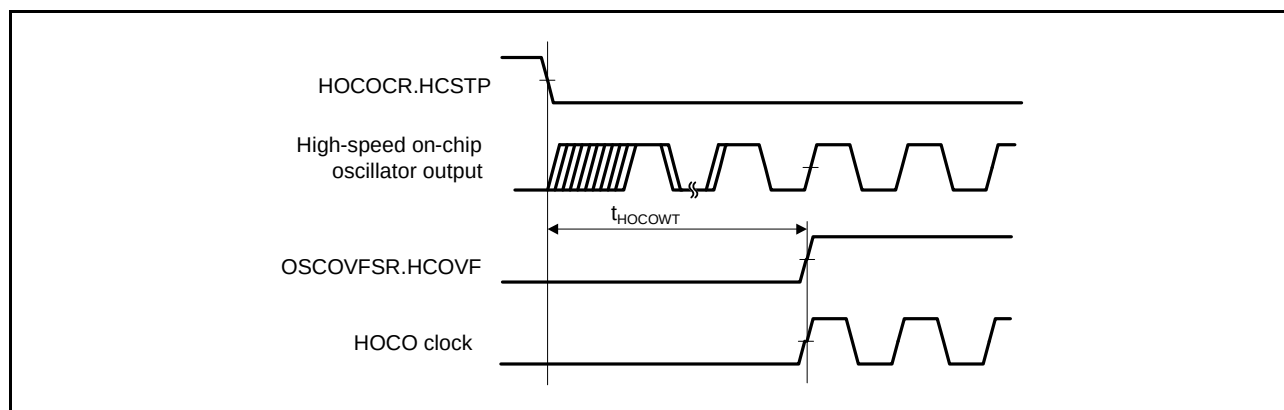


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

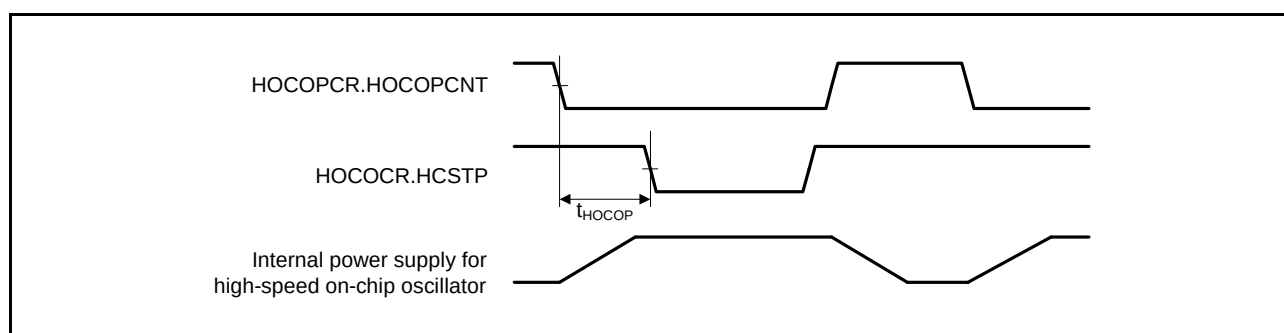


Figure 5.9 High-Speed On-Chip Oscillator Power Supply Control Timing

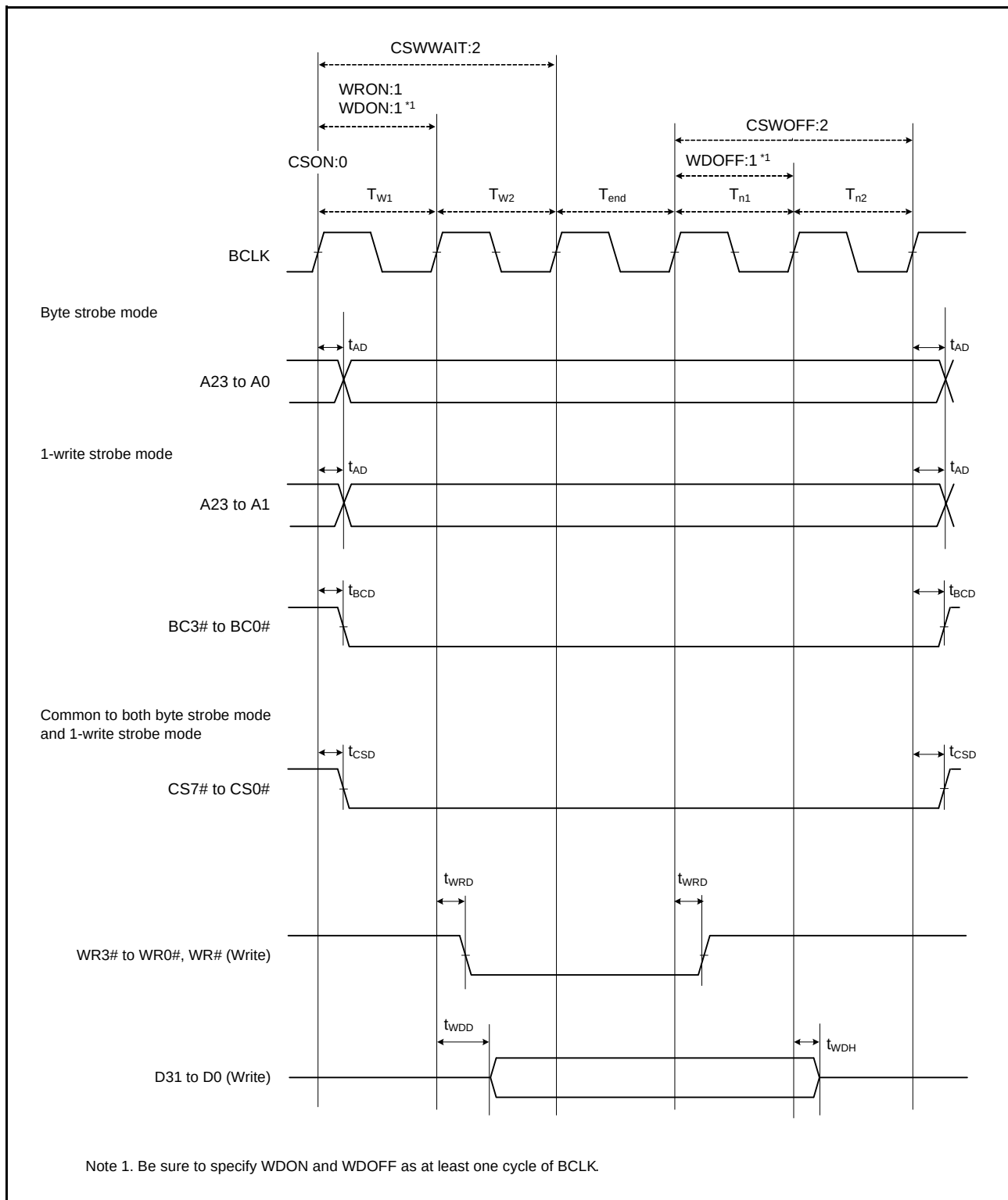


Figure 5.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

Table 5.33 RSPI Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{PAcyc}	Figure 5.46
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output	t_{SPCKr}	—	5	ns	Figure 5.47 to Figure 5.52
		Input	t_{SPCKf}	—	1	μs	
	Data input setup time	Master	t_{SU}	6	—	ns	
		Slave		$8.3 - t_{PAcyc}$	—		
	Data input hold time	Master	PCLKA division ratio set to 1/2 t_{HF}	0	—	ns	
			PCLKA division ratio set to a value other than 1/2 t_H	t_{PAcyc}	—		
		Slave		$8.3 + 2 \times t_{PAcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{PAcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{PAcyc}	
	Data output delay time	Master	t_{OD}	—	6.3	ns	
		Slave		—	$3 \times t_{PAcyc} + 20$		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns	
		Slave		$4 \times t_{PAcyc}$	—		
	MOSI and MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	5	ns	Figure 5.51, Figure 5.52
		Input		—	1	μs	
	SSL rise/fall time	Output	t_{SSLr}	—	5	ns	
		Input	t_{SSLf}	—	1	μs	
	Slave access time		t_{SA}	—	4	t_{PAcyc}	
	Slave output release time		t_{REL}	—	3	t_{PAcyc}	

Note 1. t_{PAcyc} : PCLKA cycle

Note 2. We recommend using pins that have a letter ("A", "B", etc.) to indicate group membership appended to their names as groups. For the RSPI interface, the AC portion of the electrical characteristics is measured for each group.

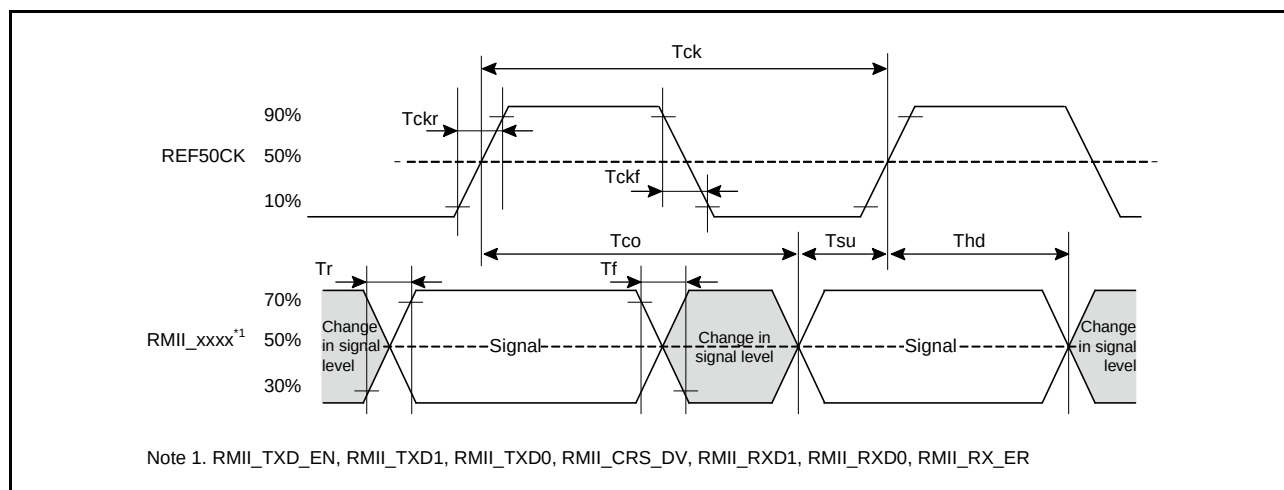


Figure 5.62 Timing with the REF50CK and RMII Signals

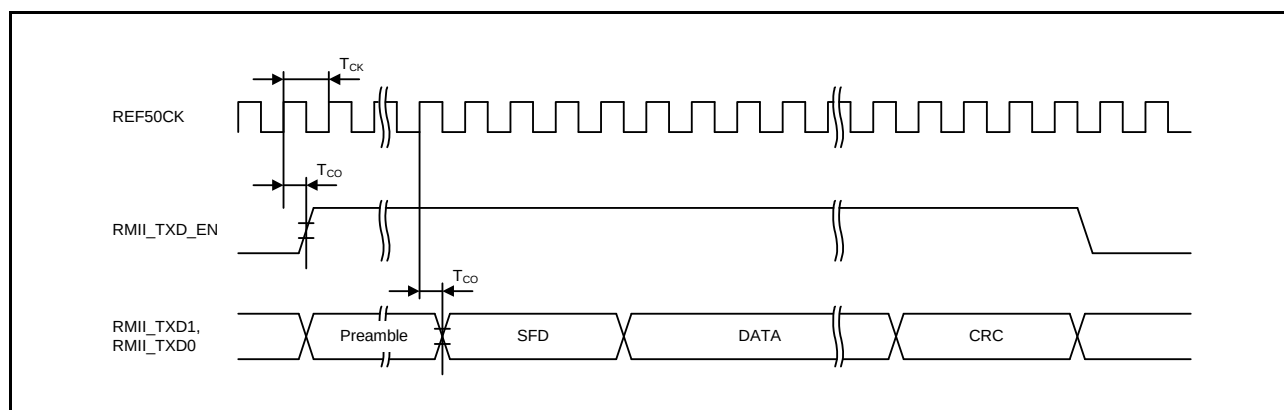


Figure 5.63 RMII Transmission Timing

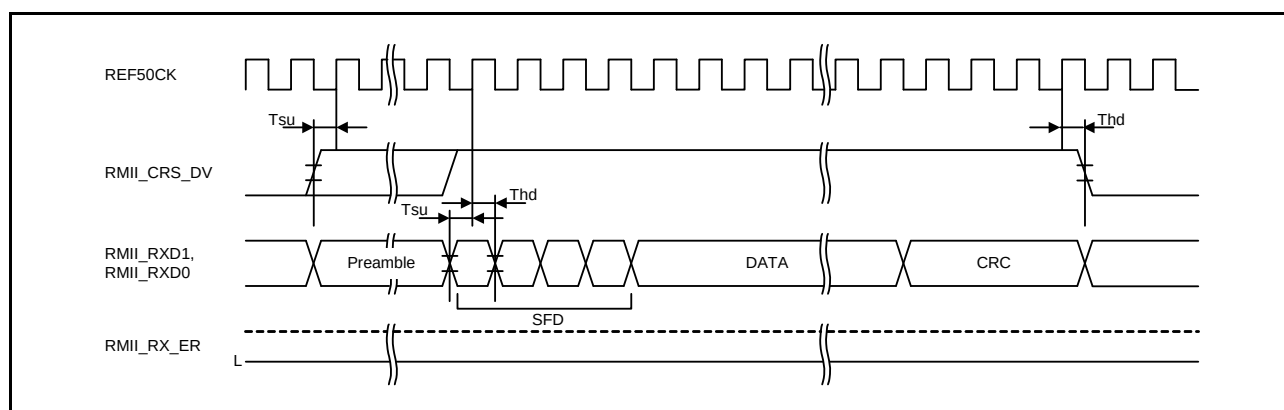


Figure 5.64 RMII Reception Timing (Normal Operation)

5.6 D/A Conversion Characteristics

Table 5.49 D/A Conversion Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V,
 $2.7 \leq V_{REFH0} \leq AVCC0$, $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Without AMP output	Absolute accuracy	—	—	± 6.0	LSB	2-M Ω resistive load 10-bit conversion
	DNL differential nonlinearity error	—	± 1.0	± 2.0	LSB	2-M Ω resistive load
	RO output resistance	—	7.5	—	k Ω	
	Conversion time	—	—	3.0	μ s	20-pF capacitive load
With AMP output	Resistive load	5	—	—	k Ω	
	Capacitive load	—	—	50	pF	
	Output voltage range	0.2	—	$AVCC1 - 0.2$	V	
	DNL differential nonlinearity error	—	± 1.0	± 2.0	LSB	
	INL integral nonlinearity error	—	± 2.0	± 4.0	LSB	
	Conversion time	—	—	4.0	μ s	

5.7 Temperature Sensor Characteristics

Table 5.50 Temperature Sensor Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	± 1	—	$^{\circ}$ C	
Temperature slope	—	4.1	—	mV/ $^{\circ}$ C	
Output voltage (at 25 $^{\circ}$ C)	—	1.24	—	V	
Temperature sensor start time	—	—	30	μ s	
Sampling time	4.15	—	—	μ s	ADSSTRT.SST[7:0] = 250 states

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