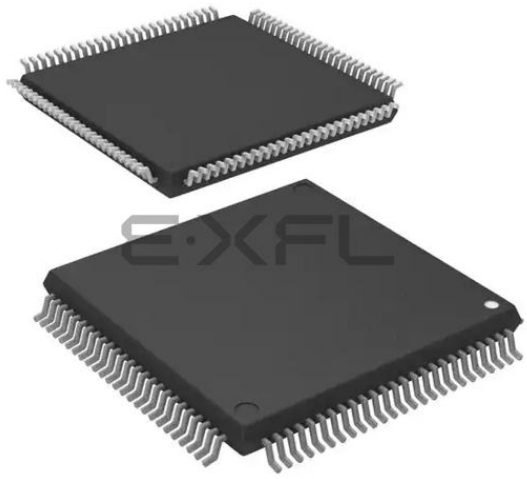
# Renesas Electronics America Inc - R5F571MJCDFP#30 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | RXv2 |
| Core Size | 32-Bit Single-Core |
| Speed | 240MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 78 |
| Program Memory Size | 3MB (3M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x12b, 14x12b; D/A 1x12 |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LFQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mjcdfp-30 |

**Table 1.4 Pin Functions (4/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Serial communications interface (SCIg) | • Asynchronous mode/clock synchronous mode | | |
| | SCK0 to SCK7 | I/O | Input/output pins for the clock |
| | RXD0 to RXD7 | Input | Input pins for received data |
| | TXD0 to TXD7 | Output | Output pins for transmitted data |
| | CTS0# to CTS7# | Input | Input pins for controlling the start of transmission and reception |
| | RTS0# to RTS7# | Output | Output pins for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL0 to SSCL7 | I/O | Input/output pins for the $I^2C$ clock |
| | SSDA0 to SSDA7 | I/O | Input/output pins for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK0 to SCK7 | I/O | Input/output pins for the clock |
| | SMISO0 to SMISO7 | I/O | Input/output pins for slave transmission of data |
| | SMOSI0 to SMOSI7 | I/O | Input/output pins for master transmission of data |
| | SS0# to SS7# | Input | Chip-select input pins |
| Serial communications interface (SCIh) | • Asynchronous mode/clock synchronous mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | RXD12 | Input | Input pin for received data |
| | TXD12 | Output | Output pin for transmitted data |
| | CTS12# | Input | Input pin for controlling the start of transmission and reception |
| | RTS12# | Output | Output pin for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL12 | I/O | Input/output pin for the $I^2C$ clock |
| | SSDA12 | I/O | Input/output pin for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | SMISO12 | I/O | Input/output pin for slave transmission of data |
| | SMOSI12 | I/O | Input/output pin for master transmission of data |
| | SS12# | Input | Chip-select input pin |
| | • Extended serial mode | | |
| | RXDX12 | Input | Input pin for received data |
| | TXDX12 | Output | Output pin for transmitted data |
| | SIOX12 | I/O | Input/output pin for received or transmitted data |
| Serial communications interface with FIFO (SCIFA) | SCK8 to SCK11 | I/O | Input/output pins for the clock |
| | RXD8 to RXD11 | Input | Input pins for received data |
| | TXD8 to TXD11 | Output | Output pins for transmitted data |
| | CTS8# to CTS11# | Input | Input pins for controlling the start of transmission and reception |
| | RTS8# to RTS11# | Output | Output pins for controlling the start of transmission and reception |
| $I^2C$ bus interface | SCL0[FM+], SCL2 | I/O | Input/output pins for clocks. Bus can be directly driven by the N-channel open drain |
| | SDA0[FM+], SDA2 | I/O | Input/output pins for data. Bus can be directly driven by the N-channel open drain |

**Table 1.4 Pin Functions (8/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| I/O ports | P00 to P03, P05, P07 | I/O | 6-bit input/output pins |
| | P10 to P17 | I/O | 8-bit input/output pins |
| | P20 to P27 | I/O | 8-bit input/output pins |
| | P30 to P37 | I/O | 8-bit input/output pins (P35: input pin) |
| | P40 to P47 | I/O | 8-bit input/output pins |
| | P50 to P56 | I/O | 7-bit input/output pins<br>(176-pin devices have only P50 to P53) |
| | P60 to P67 | I/O | 8-bit input/output pins |
| | P70 to P77 | I/O | 8-bit input/output pins |
| | P80 to P83, P86, P87 | I/O | 6-bit input/output pins |
| | P90 to P97 | I/O | 8-bit input/output pins |
| | PA0 to PA7 | I/O | 8-bit input/output pins |
| | PB0 to PB7 | I/O | 8-bit input/output pins |
| | PC0 to PC7 | I/O | 8-bit input/output pins |
| | PD0 to PD7 | I/O | 8-bit input/output pins |
| | PE0 to PE7 | I/O | 8-bit input/output pins |
| | PF0 to PF5 | I/O | 6-bit input/output pins |
| | PG0 to PG7 | I/O | 8-bit input/output pins |
| | PJ3, PJ5 | I/O | 2-bit input/output pins |

Note: Note the following regarding pin names. For details, see section 1.5, Pin Assignments.

- We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the RSPI, QSPI, SDHI, and MMC interfaces, the AC portion of the electrical characteristics is measured for each group.
- Pins that have "-DS" appended to their names can be used as triggers for release from deep software standby.
- RIIC pin functions that have [FM+] appended to their names support fast-mode plus.

**Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (6/7)**

| Pin Number 176-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 141 | | P60 | CS0# | | ET1_TX_EN/ RMII1_TXD_EN | | | |
| 142 | VCC | | | | | | | |
| 143 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B | IRQ7 | AN107 |
| 144 | | PG1 | D25 | | ET1_RX_ER/ RMII1_RX_ER | | | |
| 145 | | PD6 | D6[A6/D6] | MTIC5V/MTIOC8A/ POE4# | | MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B | IRQ6 | AN106 |
| 146 | | PG0 | D24 | | ET1_RX_CLK/ REF50CK1 | | | |
| 147 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/ POE10# | | MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B | IRQ5 | AN113 |
| 148 | | PD4 | D4[A4/D4] | MTIOC8B/POE11# | | MMC_CMD-B/ SDHI_CMD-B/ QSSL-B | IRQ4 | AN112 |
| 149 | | P97 | A23/D23 | | ET1_ERXD3 | | | |
| 150 | | PD3 | D3[A3/D3] | MTIOC8D/ GTIOC0A-E/POE8#/ TOC2 | | MMC_D3-B/ SDHI_D3-B/ QIO3-B | IRQ3 | AN111 |
| 151 | VSS | | | | | | | |
| 152 | | P96 | A22/D22 | | ET1_ERXD2 | | | |
| 153 | VCC | | | | | | | |
| 154 | | PD2 | D2[A2/D2] | MTIOC4D/ GTIOC0B-E/TIC2 | CRX0 | MMC_D2-B/ SDHI_D2-B/ QIO2_B | IRQ2 | AN110 |
| 155 | | P95 | A21/D21 | | ET1_ERXD1/ RMII1_RXD1 | | | |
| 156 | | PD1 | D1[A1/D1] | MTIOC4B/ GTIOC1A-E/POE0# | CTX0 | | IRQ1 | AN109 |
| 157 | | P94 | A20/D20 | | ET1_ERXD0/ RMII1_RXD0 | | | |
| 158 | | PD0 | D0[A0/D0] | GTIOC1B-E/POE4# | | | IRQ0 | AN108 |
| 159 | | P93 | A19/D19 | POE0# | ET1_LINKSTA/CTS7#/ RTS7#/SS7# | | | AN117 |
| 160 | | P92 | A18/D18 | POE4# | ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7 | | | AN116 |
| 161 | | P91 | A17/D17 | | ET1_COL/SCK7 | | | AN115 |
| 162 | VSS | | | | | | | |
| 163 | | P90 | A16/D16 | | ET1_RX_DV/ TXD7/SMOSI7/SSDA7 | | | AN114 |
| 164 | VCC | | | | | | | |
| 165 | | P47 | | | | | IRQ15-DS | AN007 |
| 166 | | P46 | | | | | IRQ14-DS | AN006 |
| 167 | | P45 | | | | | IRQ13-DS | AN005 |
| 168 | | P44 | | | | | IRQ12-DS | AN004 |
| 169 | | P43 | | | | | IRQ11-DS | AN003 |
| 170 | | P42 | | | | | IRQ10-DS | AN002 |

**Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (7/7)**

| Pin Number 176-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 171 | | P41 | | | | | IRQ9-DS | AN001 |
| 172 | VREFL0 | | | | | | | |
| 173 | | P40 | | | | | IRQ8-DS | AN000 |
| 174 | VREFH0 | | | | | | | |
| 175 | AVCC0 | | | | | | | |
| 176 | | P07 | | | | | IRQ15 | ADTRG0# |

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| C9 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B | IRQ7 | AN107 |
| C10 | | P63 | CS3#/CAS# | | | | | |
| C11 | | PE0 | D8[A8/D8] | MTIOC3D/ GTIOC2B-A | SCK12/SSLB1-B | MMC_D4-B | | ANEX0 |
| C12 | | P70 | SDCLK | | | | | |
| C13 | VSS | | | | | | | |
| D1 | | P00 | | TMRI0 | TXD6/SMOSI6/SSDA6 | | IRQ8 | AN118 |
| D2 | | PF5 | | | | | IRQ4 | |
| D3 | | P03 | | | | | IRQ11 | DA0 |
| D4 | | P01 | | TMCI0 | RXD6/SMISO6/SSCL6 | | IRQ9 | AN119 |
| D5 | VCC | | | | | | | |
| D6 | | P93 | A19 | POE0# | CTS7#/RTS7#/SS7# | | | AN117 |
| D7 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/ POE10# | | MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B | IRQ5 | AN113 |
| D8 | | P60 | CS0# | | | | | |
| D9 | | P64 | CS4#/WE# | | | | | |
| D10 | | PE7 | D15[A15/D15] | MTIOC6A/ GTIOC3A-E/TOC1 | MISOB-B | MMC_RES#-B/ SDHI_WP-B | IRQ7 | AN105 |
| D11 | VCC | | | | | | | |
| D12 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B/ GTIOC0A-A | ET0_RX_CLK/ REF50CK0/ RSPCKB-B | | IRQ5 | AN103 |
| D13 | | PE6 | D14[A14/D14] | TIOC6C/GTIOC3B-E/ TIC1 | MOSIB-B | MMC_CD-B/ SDHI_CD-B | IRQ6 | AN104 |
| E1 | VSS | | | | | | | |
| E2 | VCL | | | | | | | |
| E3 | | PJ5 | | POE8# | CTS2#/RTS2#/SS2# | | | |
| E4 | EMLE | | | | | | | |
| E5 | | P44 | | | | | IRQ12-DS | AN004 |
| E10 | | PA0 | A0/BC0# | MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16 | SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN | | | |
| E11 | | P66 | CS6#/DQM0 | MTIOC7D/ GTIOC2B-C | CTX2 | | | |
| E12 | | P65 | CS5#/CKE | | | | | |
| E13 | | P67 | CS7#/DQM1 | MTIOC7C/ GTIOC1B-C | CRX2 | | IRQ15 | |
| F1 | XCIN | | | | | | | |
| F2 | XCOUT | | | | | | | |
| F3 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/CTS6#/ RTS6#/CTS0#/RTS0#/ SS6#/SS0# | | | |
| F4 | VBATT | | | | | | | |
| F10 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19 | RXD5/SMISO5/ SSCL5/ET0_MDIO | | IRQ6-DS | |
| F11 | VSS | | | | | | | |
| F12 | | PA1 | A1 | MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17 | SCK5/SSLA2-B/ ET0_WOL | | IRQ11 | |

**Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (2/5)**

| Pin Number 144-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 36 | | P21 | | MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0 | PIXD5 | IRQ9 | |
| 37 | | P20 | | MTIOC1A/TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0 | PIXD4 | IRQ8 | |
| 38 | | P17 | | MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8# | SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0 | PIXD3 | IRQ7 | ADTRG1# |
| 39 | | P87 | | MTIOC4C/ GTIOC1B-B/TIOCA2 | TXD10 | PIXD2 | | |
| 40 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT | TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | | IRQ6 | ADTRG0# |
| 41 | | P86 | | MTIOC4D/ GTIOC2B-B/TIOCA0 | RXD10 | PIXD1 | | |
| 42 | | P15 | | MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13 | RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1 | PIXD0 | IRQ5 | |
| 43 | | P14 | | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15 | CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA | | IRQ4 | |
| 44 | | P13 | | MTIOC0B/TIOCA5/ TMO3/PO13 | TXD2/SMOSI2/ SSDA2/SDA0[FM+] | | IRQ3 | ADTRG1# |
| 45 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/SCL0[FM+] | | IRQ2 | |
| 46 | VCC_USB | | | | | | | |
| 47 | | | | | USB0_DM | | | |
| 48 | | | | | USB0_DP | | | |
| 49 | VSS_USB | | | | | | | |
| 50 | | P56 | EDACK1 | MTIOC3C/TIOCA1 | | | | |
| 51 | TRDATA3 | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | CRX1/ET0_EXOUT | | IRQ10 | |
| 52 | TRDATA2 | P54 | ALE/EDACK0 | MTIOC4B/TMCI1 | CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA | | | |
| 53 | | P53 | BCLK | | | | | |
| 54 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | |
| 55 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2-A | | | |
| 56 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | |
| 57 | VSS | | | | | | | |
| 58 | TRCLK | P83 | EDACK1 | MTIOC4C/ GTIOC0A-D | CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10 | | | |
| 59 | VCC | | | | | | | |
| 60 | UB | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF | TXD8/MISOA-A/ ET0_COL | MMC_D7-A | IRQ14 | |
| 61 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30 | RXD8/MOSIA-A/ ET0_ETXD3 | MMC_D6-A | IRQ13 | |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (1/4)**

| Pin Number 100-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| A1 | P05 | | | | | | IRQ13 | DA1 |
| A2 | AVCC1 | | | | | | | |
| A3 | | P07 | | | | | IRQ15 | ADTRG0# |
| A4 | VREFL0 | | | | | | | |
| A5 | | P43 | | | | | IRQ11-DS | AN003 |
| A6 | | PD0 | D0[A0/D0] | GTIOC1B-E/POE4# | | | IRQ0 | AN108 |
| A7 | | PD4 | D4[A4/D4] | MTIOC8B/POE11# | | MMC_CMD-B/ SDHI_CMD-B/ QSSL-B | IRQ4 | AN112 |
| A8 | | PE0 | D8[A8/D8] | MTIOC3D/GTIOC2B-A | SCK12/SSLB1-B | MMC_D4-B | | ANEX0 |
| A9 | | PE1 | D9[A9/D9] | MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | | ANEX1 |
| A10 | | PE2 | D10[A10/ D10] | MTIOC4A/GTIOC0B-A/PO23/TIC3 | RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B | MMC_D6-B | IRQ7-DS | AN100 |
| B1 | EMLE | | | | | | | |
| B2 | AVSS0 | | | | | | | |
| B3 | AVCC0 | | | | | | | |
| B4 | | P40 | | | | | IRQ8-DS | AN000 |
| B5 | | P44 | | | | | IRQ12-DS | AN004 |
| B6 | | PD1 | D1[A1/D1] | MTIOC4B/GTIOC1A-E/POE0# | CTX0 | | IRQ1 | AN109 |
| B7 | | PD3 | D3[A3/D3] | MTIOC8D/GTIOC0A-E/POE8#/TOC2 | | MMC_D3-B/ SDHI_D3-B/ QIO3-B | IRQ3 | AN111 |
| B8 | | PD6 | D6[A6/D6] | MTIC5V/MTIOC8A/ POE4# | | MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO-B | IRQ6 | AN106 |
| B9 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | MMC_D1-B/ SDHI_D1-B/ QIO1/QMI-B | IRQ7 | AN107 |
| B10 | | PE3 | D11[A11/ D11] | MTIOC4B/GTIOC2A-A/PO26/POE8#/TOC3 | CTS12#/RTS12#/ SS12#/ET0_ERXD3 | MMC_D7-B | | AN101 |
| C1 | VCL | | | | | | | |
| C2 | AVSS1 | | | | | | | |
| C3 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/CTS6#/ RTS6#/CTS0#/RTS0#/ SS6#/SS0# | | | |
| C4 | VREFH0 | | | | | | | |
| C5 | | P42 | | | | | IRQ10-DS | AN002 |
| C6 | | P47 | | | | | IRQ15-DS | AN007 |
| C7 | | PD2 | D2[A2/D2] | MTIOC4D/GTIOC0B-E/TIC2 | CRX0 | MMC_D2-B/ SDHI_D2-B/ QIO2-B | IRQ2 | AN110 |

**Table 4.1 List of I/O Registers (Address Order) (2 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 003Ch | SYSTEM | Oscillation Stabilization Flag Register | OSCOVFSR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0040h | SYSTEM | Oscillation Stop Detection Control Register | OSTDCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0041h | SYSTEM | Oscillation Stop Detection Status Register | OSTDSR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 00A0h | SYSTEM | Operating Power Control Register | OPCCR | 8 | 8 | 3 ICLK | | Low Power Consumption |
| 0008 00A1h | SYSTEM | Sleep Mode Return Clock Source Switching Register | RSTCKCR | 8 | 8 | 3 ICLK | | Low Power Consumption |
| 0008 00A2h | SYSTEM | Main Clock Oscillator Wait Control Register | MOSCWTCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 00A3h | SYSTEM | Sub-Clock Oscillator Wait Control Register | SOSCWTCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 00C0h | SYSTEM | Reset Status Register 2 | RSTSR2 | 8 | 8 | 3 ICLK | | Resets |
| 0008 00C2h | SYSTEM | Software Reset Register | SWRR | 16 | 16 | 3 ICLK | | Resets |
| 0008 00E0h | SYSTEM | Voltage Monitoring 1 Circuit Control Register 1 | LVD1CR1 | 8 | 8 | 3 ICLK | | LDVA |
| 0008 00E1h | SYSTEM | Voltage Monitoring 1 Circuit Status Register | LVD1SR | 8 | 8 | 3 ICLK | | LDVA |
| 0008 00E2h | SYSTEM | Voltage Monitoring 2 Circuit Control Register 1 | LVD2CR1 | 8 | 8 | 3 ICLK | | LDVA |
| 0008 00E3h | SYSTEM | Voltage Monitoring 2 Circuit Status Register | LVD2SR | 8 | 8 | 3 ICLK | | LDVA |
| 0008 03FEh | SYSTEM | Protect Register | PRCR | 16 | 16 | 3 ICLK | | Register Write Protection Function |
| 0008 1200h | RAM | RAM Operating Mode Control Register | RAMMODE | 8 | 8 | 2 ICLK | | RAM |
| 0008 1201h | RAM | RAM Error Status Register | RAMSTS | 8 | 8 | 2 ICLK | | RAM |
| 0008 1204h | RAM | RAM Protection Register | RAMPRCR | 8 | 8 | 2 ICLK | | RAM |
| 0008 1208h | RAM | RAM Error Address Capture Register | RAMECAD | 32 | 32 | 2 ICLK | | RAM |
| 0008 12C0h | ECCRAM | ECCRAM Operating Mode Control Register | ECCRAMMODE | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C1h | ECCRAM | ECCRAM 2-Bit Error Status Register | ECCRAM2STS | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C2h | ECCRAM | ECCRAM 1-Bit Error Information Update Enable Register | ECCRAM1STSEN | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C3h | ECCRAM | ECCRAM 1-Bit Error Status Register | ECCRAM1STS | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C4h | ECCRAM | ECCRAM Protection Register | ECCRAMPRCR | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C8h | ECCRAM | ECCRAM 2-Bit Error Address Capture Register | ECCRAM2ECAD | 32 | 32 | 2 ICLK | | RAM |
| 0008 12CCh | ECCRAM | ECCRAM 1-Bit Error Address Capture Register | ECCRAM1ECAD | 32 | 32 | 2 ICLK | | RAM |
| 0008 12D0h | ECCRAM | ECCRAM Protection Register 2 | ECCRAMPRCR2 | 8 | 8 | 2 ICLK | | RAM |
| 0008 12D4h | ECCRAM | ECCRAM Test Control Register | ECCRAMETST | 8 | 8 | 2 ICLK | | RAM |
| 0008 1300h | BSC | Bus Error Status Clear Register | BERCLR | 8 | 8 | 2 ICLK | | Buses |
| 0008 1304h | BSC | Bus Error Monitoring Enable Register | BEREN | 8 | 8 | 2 ICLK | | Buses |
| 0008 1308h | BSC | Bus Error Status Register 1 | BERSR1 | 8 | 8 | 2 ICLK | | Buses |

**Table 4.1 List of I/O Registers (Address Order) (15 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 81EAh | PPG0 | Output Data Registers H | PODRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81EBh | PPG0 | Output Data Registers L | PODRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81ECh | PPG0 | Next Data Registers H*1 | NDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81EDh | PPG0 | Next Data Registers L*2 | NDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81EEh | PPG0 | Next Data Registers H*1 | NDRH2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81EFh | PPG0 | Next Data Registers L*2 | NDRL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F0h | PPG1 | PPG Trigger Select Register | PTRSLR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F6h | PPG1 | PPG Output Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F7h | PPG1 | PPG Output Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F8h | PPG1 | Next Data Enable Registers H | NDERH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F9h | PPG1 | Next Data Enable Registers L | NDERL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FAh | PPG1 | Output Data Registers H | PODRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FBh | PPG1 | Output Data Registers L | PODRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FCh | PPG1 | Next Data Registers H*3 | NDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FDh | PPG1 | Next Data Registers L*4 | NDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FEh | PPG1 | Next Data Registers H*3 | NDRH2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FFh | PPG1 | Next Data Registers L*4 | NDRL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 8200h | TMR0 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8201h | TMR1 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8202h | TMR0 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8203h | TMR1 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8204h | TMR0 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8204h | TMR01 | Time Constant Register A | TCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8205h | TMR1 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8206h | TMR0 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8206h | TMR01 | Time Constant Register B | TCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8207h | TMR1 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8208h | TMR0 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8208h | TMR01 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8209h | TMR1 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 820Ah | TMR0 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 820Ah | TMR01 | Timer Counter Control Register | TCCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 820Bh | TMR1 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 820Ch | TMR0 | Time Count Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 820Dh | TMR1 | Time Count Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8210h | TMR2 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8211h | TMR3 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8212h | TMR2 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8213h | TMR3 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8214h | TMR2 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8214h | TMR23 | Time Constant Register A | TCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8215h | TMR3 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8216h | TMR2 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8216h | TMR23 | Time Constant Register B | TCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8217h | TMR3 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8218h | TMR2 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8218h | TMR23 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 8219h | TMR3 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 821Ah | TMR2 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMRb |
| 0008 821Ah | TMR23 | Timer Counter Control Register | TCCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMRb |

**Table 4.1 List of I/O Registers (Address Order) (20 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 9E24h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 2 | SPBMUL2 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E28h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 3 | SPBMUL3 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 A000h | SCI0 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A001h | SCI0 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A002h | SCI0 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A003h | SCI0 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A004h | SCI0 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A005h | SCI0 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A006h | SCI0 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A007h | SCI0 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A008h | SCI0 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A009h | SCI0 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Ah | SCI0 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Bh | SCI0 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Ch | SCI0 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Dh | SCI0 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Eh | SCI0 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Fh | SCI0 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A00Eh | SCI0 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A010h | SCI0 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A011h | SCI0 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A010h | SCI0 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A012h | SCI0 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A020h | SCI1 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A021h | SCI1 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A022h | SCI1 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A023h | SCI1 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A024h | SCI1 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A025h | SCI1 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A026h | SCI1 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A027h | SCI1 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |

**Table 4.1 List of I/O Registers (Address Order) (31 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C0EDh | PORTD | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EEh | PORTE | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0F0h | PORTG | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C100h | MPC | CS Output Enable Register | PFCSE | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C102h | MPC | CS Output Pin Select Register 0 | PFCSS0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C103h | MPC | CS Output Pin Select Register 1 | PFCSS1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C104h | MPC | Address Output Enable Register 0 | PFAOE0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C105h | MPC | Address Output Enable Register 1 | PFAOE1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C106h | MPC | External Bus Control Register 0 | PFBCR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C107h | MPC | External Bus Control Register 1 | PFBCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C10Eh | MPC | Ethernet Control Register | PFENET | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C11Fh | MPC | Write-Protect Register | PWPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C140h | MPC | P00 Pin Function Control Register | P00PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C141h | MPC | P01 Pin Function Control Register | P01PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C142h | MPC | P02 Pin Function Control Register | P02PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C143h | MPC | P03 Pin Function Control Register | P03PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C145h | MPC | P05 Pin Function Control Register | P05PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C147h | MPC | P07 Pin Function Control Register | P07PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C148h | MPC | P10 Pin Function Control Register | P10PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C149h | MPC | P11 Pin Function Control Register | P11PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Ah | MPC | P12 Pin Function Control Register | P12PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Bh | MPC | P13 Pin Function Control Register | P13PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Ch | MPC | P14 Pin Function Control Register | P14PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Dh | MPC | P15 Pin Function Control Register | P15PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Eh | MPC | P16 Pin Function Control Register | P16PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Fh | MPC | P17 Pin Function Control Register | P17PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C150h | MPC | P20 Pin Function Control Register | P20PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C151h | MPC | P21 Pin Function Control Register | P21PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C152h | MPC | P22 Pin Function Control Register | P22PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C153h | MPC | P23 Pin Function Control Register | P23PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C154h | MPC | P24 Pin Function Control Register | P24PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C155h | MPC | P25 Pin Function Control Register | P25PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C156h | MPC | P26 Pin Function Control Register | P26PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C157h | MPC | P27 Pin Function Control Register | P27PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C158h | MPC | P30 Pin Function Control Register | P30PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C159h | MPC | P31 Pin Function Control Register | P31PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C15Ah | MPC | P32 Pin Function Control Register | P32PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C15Bh | MPC | P33 Pin Function Control Register | P33PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C15Ch | MPC | P34 Pin Function Control Register | P34PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C160h | MPC | P40 Pin Function Control Register | P40PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C161h | MPC | P41 Pin Function Control Register | P41PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C162h | MPC | P42 Pin Function Control Register | P42PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C163h | MPC | P43 Pin Function Control Register | P43PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C164h | MPC | P44 Pin Function Control Register | P44PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C165h | MPC | P45 Pin Function Control Register | P45PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C166h | MPC | P46 Pin Function Control Register | P46PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C167h | MPC | P47 Pin Function Control Register | P47PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C168h | MPC | P50 Pin Function Control Register | P50PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C169h | MPC | P51 Pin Function Control Register | P51PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Ah | MPC | P52 Pin Function Control Register | P52PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |

**Table 4.1 List of I/O Registers (Address Order) (35 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C414h | RTC | Binary Counter 2 Alarm Register | BCNT2AR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C416h | RTC | Day-of-Week Alarm Register | RWKAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C416h | RTC | Binary Counter 3 Alarm Register | BCNT3AR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C418h | RTC | Date Alarm Register | RDAYAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C418h | RTC | Binary Counter 0 Alarm Enable Register | BCNT0AER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Ah | RTC | Month Alarm Register | RMONAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Ah | RTC | Binary Counter 1 Alarm Enable Register | BCNT1AER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Ch | RTC | Year Alarm Register | RYRAR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Ch | RTC | Binary Counter 2 Alarm Enable Register | BCNT2AER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Eh | RTC | Year Alarm Enable Register | RYRAREN | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Eh | RTC | Binary Counter 3 Alarm Enable Register | BCNT3AER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C422h | RTC | RTC Control Register 1 | RCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C424h | RTC | RTC Control Register 2 | RCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C426h | RTC | RTC Control Register 3 | RCR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C428h | RTC | RTC Control Register 4 | RCR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C42Ah | RTC | Frequency Register H | RFRH | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C42Ch | RTC | Frequency Register L | RFRL | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C42Eh | RTC | Time Error Adjustment Register | RADJ | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C440h | RTC | Time Capture Control Register 0 | RTCCR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C442h | RTC | Time Capture Control Register 1 | RTCCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C444h | RTC | Time Capture Control Register 2 | RTCCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C452h | RTC | Second Capture Register 0 | RSECCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C452h | RTC | BCNT0 Capture Register 0 | BCNT0CP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C454h | RTC | Minute Capture Register 0 | RMINCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C454h | RTC | BCNT1 Capture Register 0 | BCNT1CP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C456h | RTC | Hour Capture Register 0 | RHRCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C456h | RTC | BCNT2 Capture Register 0 | BCNT2CP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C45Ah | RTC | Date Capture Register 0 | RDAYCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C45Ah | RTC | BCNT3 Capture Register 0 | BCNT3CP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C45Ch | RTC | Month Capture Register 0 | RMONCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C462h | RTC | Second Capture Register 1 | RSECCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C462h | RTC | BCNT0 Capture Register 1 | BCNT0CP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C464h | RTC | Minute Capture Register 1 | RMINCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C464h | RTC | BCNT1 Capture Register 1 | BCNT1CP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C466h | RTC | Hour Capture Register 1 | RHRCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C466h | RTC | BCNT2 Capture Register 1 | BCNT2CP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C46Ah | RTC | Date Capture Register 1 | RDAYCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C46Ah | RTC | BCNT3 Capture Register 1 | BCNT3CP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C46Ch | RTC | Month Capture Register 1 | RMONCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C472h | RTC | Second Capture Register 2 | RSECCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C472h | RTC | BCNT0 Capture Register 2 | BCNT0CP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C474h | RTC | Minute Capture Register 2 | RMINCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C474h | RTC | BCNT1 Capture Register 2 | BCNT1CP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C476h | RTC | Hour Capture Register 2 | RHRCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C476h | RTC | BCNT2 Capture Register 2 | BCNT2CP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C47Ah | RTC | Date Capture Register 2 | RDAYCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C47Ah | RTC | BCNT3 Capture Register 2 | BCNT3CP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C47Ch | RTC | Month Capture Register 2 | RMONCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C4C0h | POE3 | Input Level Control/Status Register 1 | ICSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3 |
| 0008 C4C2h | POE3 | Output Level Control/Status Register 1 | OCSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3 |

## 5.2 DC Characteristics

**Table 5.2 DC Characteristics (1)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | IRQ input pin*1<br>MTU input pin*1<br>GPT input pin*1<br>POE3 input pin*1<br>TPU input pin*1<br>TMR input pin*1<br>SCI input pin*1<br>ADTRG# input pin*1<br>QSPI input pin*1<br>RES#, NMI, TCK | $V_{IH}$ | VCC × 0.8 | — | VCC + 0.3 | V | |
| | | $V_{IL}$ | –0.3 | — | VCC × 0.2 | | |
| | | $\Delta V_T$ | VCC × 0.06 | — | — | | |
| | RIIC input pin (except for SMBus) | $V_{IH}$ | VCC × 0.7 | — | 5.8 | | |
| | | $V_{IL}$ | –0.3 | — | VCC × 0.3 | | |
| | | $\Delta V_T$ | VCC × 0.05 | — | — | | |
| | Ports for 5 V tolerant*2 | $V_{IH}$ | VCC × 0.8 | — | 5.8 | | |
| | | $V_{IL}$ | –0.3 | — | VCC × 0.2 | | |
| | Other input pins excluding ports for 5 V tolerant*3 | $V_{IH}$ | VCC × 0.8 | — | VCC + 0.3 | | |
| | | $V_{IL}$ | –0.3 | — | VCC × 0.2 | | |
| Input high voltage (except for Schmitt trigger input pin) | MD pin, EMLE | $V_{IH}$ | VCC × 0.9 | — | VCC + 0.3 | V | |
| | EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SSI input pin, SDHI input pin, MMC input pin, PDC input pin | | VCC × 0.8 | — | VCC + 0.3 | | |
| | ETHERC input pin | | 2.3 | — | VCC + 0.3 | | |
| | XCIN*3 | | VCC × 0.8 | — | VCC + 0.3 | | |
| | D0 to D31 | | VCC × 0.7 | — | VCC + 0.3 | | |
| | RIIC (SMBus) | | 2.1 | — | VCC + 0.3 | | |
| Input low voltage (except for Schmitt trigger input pin) | MD pin, EMLE | $V_{IL}$ | –0.3 | — | VCC × 0.1 | V | |
| | EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SSI input pin, SDHI input pin, MMC input pin, PDC input pin | | –0.3 | — | VCC × 0.2 | | |
| | XCIN*3 | | –0.3 | — | VCC × 0.2 | | |
| | D0 to D31 | | –0.3 | — | VCC × 0.3 | | |
| | RIIC (SMBus) | | –0.3 | — | 0.8 | | |

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.
Note 3. For P32, P31, P30, and XCIN, input as follows when the $V_{BATT}$ power supply is selected.
VIH Min. = $V_{BATT}$ × 0.8, VIH Max. = $V_{BATT}$ + 0.3, VIL Min. = –0.3, VIL Max. = $V_{BATT}$ × 0.2 ($V_{BATT}$ = 2.0 to 3.6 V)

which writing proceed) or data flash memory during program execution in the code flash memory.
Note 6. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.
Note 7. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

### Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Analog power supply current*1 | During 12-bit A/D conversion (unit 0) | | $AI_{CC}$ | — | 0.7 | 1.1 | mA | IAVCC0_AD |
| | During 12-bit A/D conversion (unit 0) with the channel-dedicated sample-and-hold circuits for 3 channels operating | | | — | 2.2 | 3.3 | mA | IAVCC0_AD+SH |
| | During 12-bit A/D conversion (unit 1) | | | — | 0.7 | 1.1 | mA | IAVCC1_AD |
| | During 12-bit A/D conversion (unit 1) with the temperature sensor operating | | | — | 0.7 | 2.3 | mA | IAVCC1_AD+TEMP |
| | During D/A conversion (per unit) | Without AMP output | | — | 0.24 | 0.4 | mA | IAVCC1_DA |
| | | With AMP output | | — | 0.45 | 0.7 | mA | |
| | Waiting for A/D, D/A, or temperature sensor conversion (all units) | | | — | 0.9 | 1.6 | mA | IAVCC0 + IAVCC1 |
| | A/D, D/A converter, temperature sensor in standby mode (all units) | | | — | 1.3 | 5.0 | µA | IAVCC0 + IAVCC1 |
| Reference power supply current | During 12-bit A/D conversion (unit 0) | | $AI_{REFH}$ | — | 70 | 120 | µA | IVREFH0 |
| | Waiting for 12-bit A/D conversion (unit 0) | | | — | 0.07 | 0.5 | µA | IVREFH0 |
| | 12-bit A/D converter in standby mode (unit 0) | | | — | 0.07 | 0.5 | µA | IVREFH0 |
| USB operating current | Low speed | USBb | $I_{CCUSBLS}$ | — | 3.5 | 6.5 | mA | VCC_USB |
| | | USBA | | — | 10.5 | 13.5 | mA | VCC_USBA = AVCC_USBA (PHYSET.HSEB = 0) |
| | | USBA | | — | 2.8 | 3.6 | mA | VCC_USBA = AVCC_USBA (PHYSET.HSEB = 1) |
| | Full speed | USBb | $I_{CCUSBFS}$ | — | 4.0 | 10.0 | mA | VCC_USB |
| | | USBA | | — | 14.0 | 22.0 | mA | VCC_USBA = AVCC_USBA (PHYSET.HSEB = 0) |
| | | USBA | | — | 6.5 | 13.0 | mA | VCC_USBA = AVCC_USBA (PHYSET.HSEB = 1) |
| | High speed | USBA | $I_{CCUSBHS}$ | — | 50.0 | 65.0 | mA | VCC_USBA = AVCC_USBA |
| | Standby mode (direct power down) | USBA | $I_{CCUSBSBY}$ | — | 0.1 | 3.0 | µA | VCC_USBA = AVCC_USBA |
| RAM standby voltage | | | $V_{RAM}$ | 2.7 | — | — | V | |
| VCC rising gradient | | | SrVCC | 8.4 | — | 20000 | µs/V | |
| VCC falling gradient*2 | | | SfVCC | 8.4 | — | — | µs/V | |

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D conversion (unit 1) and D/A conversion.
Note 2. This applies when $V_{BATT}$ is used.

## 5.3.1 Reset Timing

**Table 5.10 Reset Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RES# pulse width | Power-on | $t_{RESWP}$ | 1 | — | — | ms | Figure 5.1 |
| | Deep software standby mode | $t_{RESWD}$ | 0.6 | — | — | ms | Figure 5.2 |
| | Software standby mode, low-speed operating mode 2 | $t_{RESWS}$ | 0.3 | — | — | ms | |
| | Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory | $t_{RESWF}$ | 200 | — | — | µs | |
| | Other than above | $t_{RESW}$ | 200 | — | — | µs | |
| Waiting time after release from the RES# pin reset | | $t_{RESWT}$ | 62 | — | 63 | $t_{Lcyc}$ | Figure 5.1 |
| Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset) | | $t_{RESW2}$ | 108 | — | 116 | $t_{Lcyc}$ | |

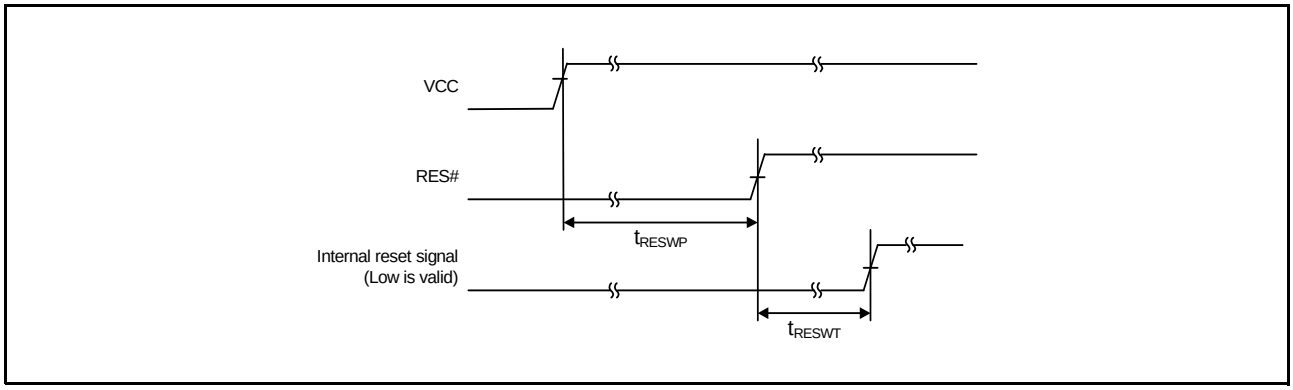



**Figure 5.1 Reset Input Timing at Power-On**

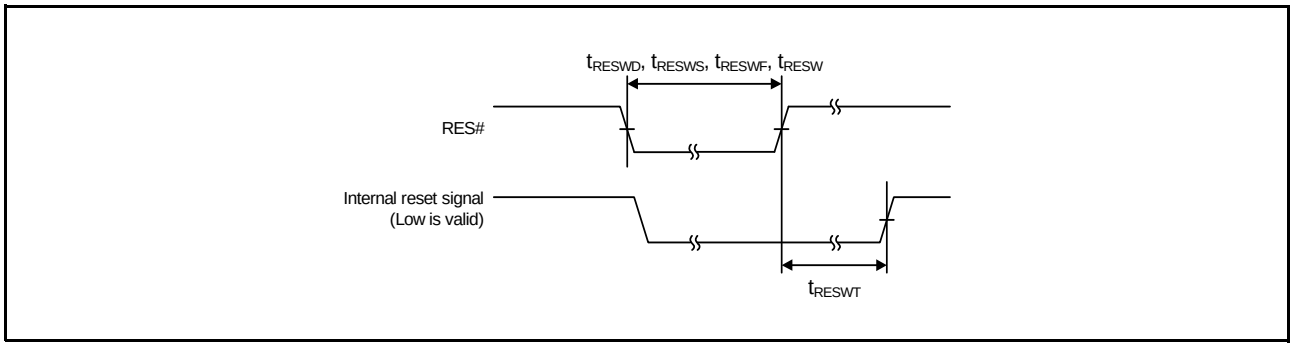



**Figure 5.2 Reset Input Timing**

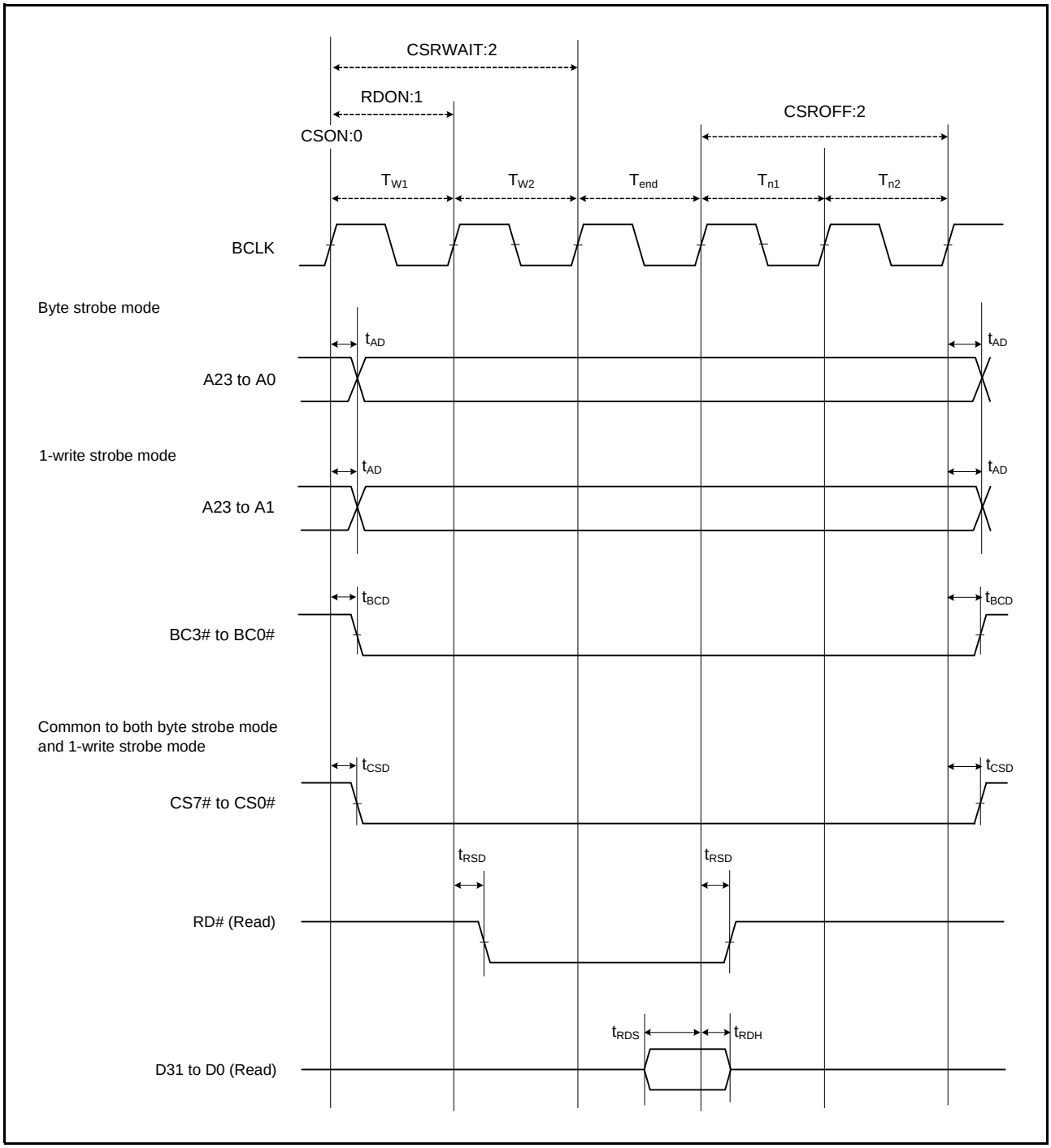
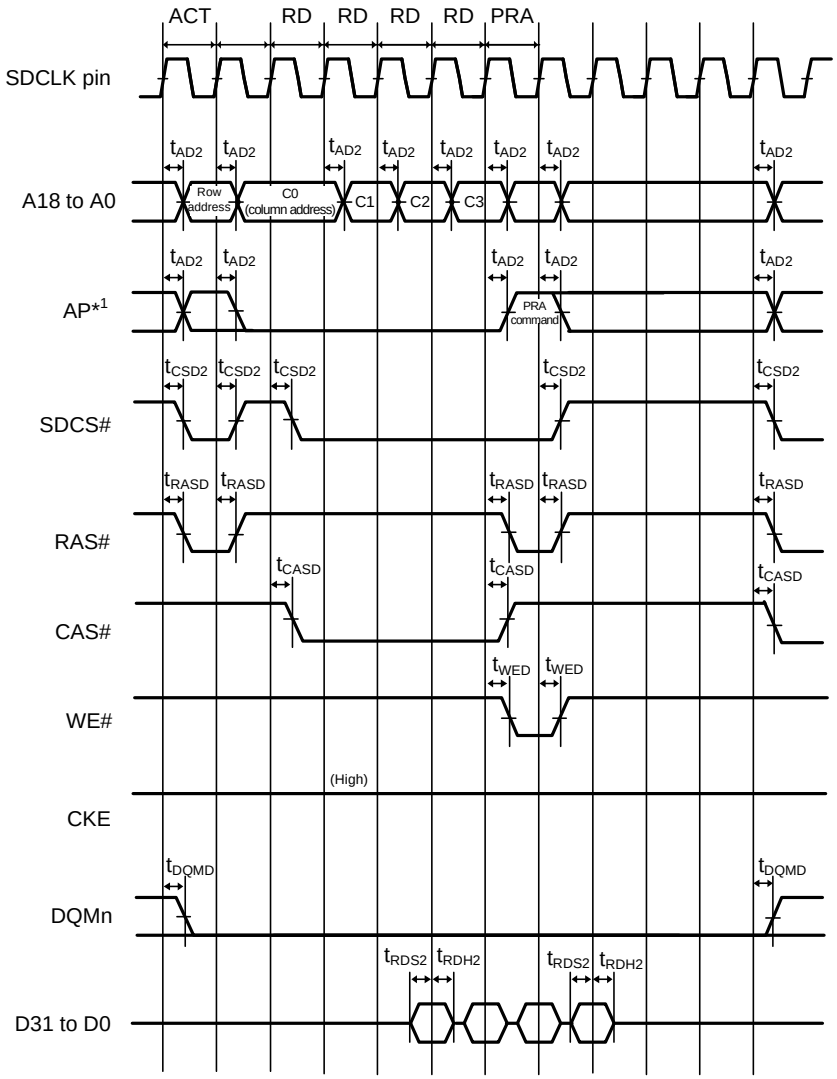
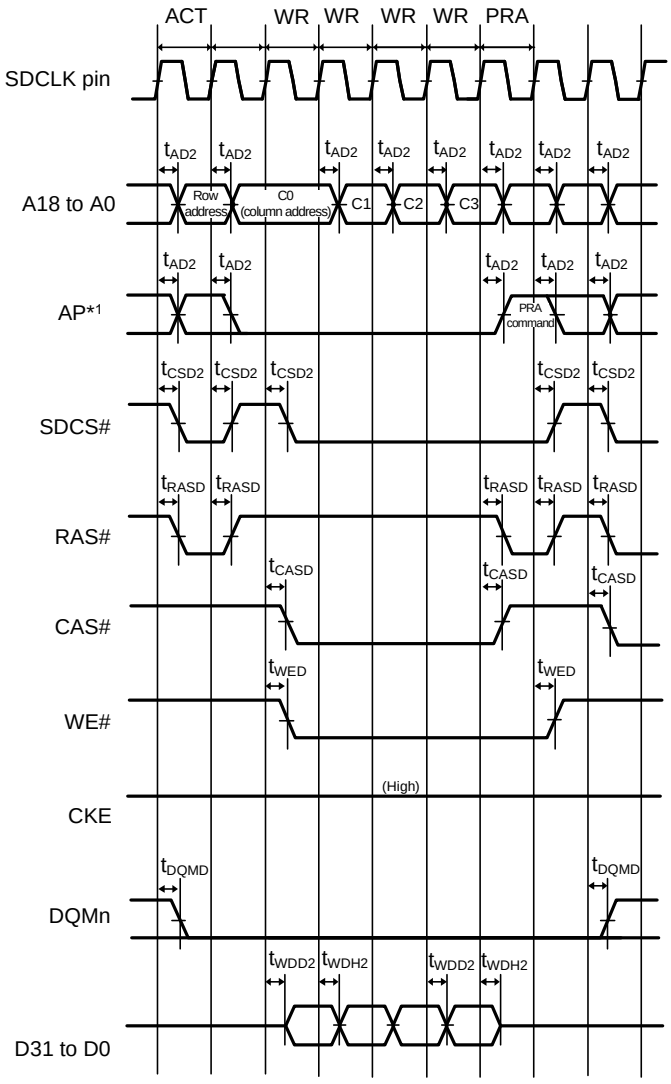



**Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)**




Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.25 SDRAM Space Multiple Read Bus Timing**




Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.26 SDRAM Space Multiple Write Bus Timing**

### Table 5.34 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | $t_{SPcyc}$ | 4 | 65536 | $t_{PBcyc}$ | Figure 5.46 |
| | SCK clock cycle input (slave) | | 8 | 65536 | | |
| | SCK clock high pulse width | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | $t_{SPCKr}$, $t_{SPCKf}$ | — | 20 | ns | |
| | Data input setup time | $t_{SU}$ | 33.3 | — | ns | Figure 5.47 to Figure 5.52 |
| | Data input hold time | $t_H$ | 33.3 | — | ns | |
| | SS input setup time | $t_{LEAD}$ | 1 | — | $t_{SPcyc}$ | |
| | SS input hold time | $t_{LAG}$ | 1 | — | $t_{SPcyc}$ | |
| | Data output delay time | $t_{OD}$ | — | 33.3 | ns | |
| | Data output hold time | $t_{OH}$ | –10 | — | ns | |
| | Data rise/fall time | $t_{Dr}$, $t_{Df}$ | — | 16.6 | ns | |
| | SS input rise/fall time | $t_{SSLr}$, $t_{SSLf}$ | — | 16.6 | ns | |
| | Slave access time | $t_{SA}$ | — | 5 | $t_{PAcyc}$ | Figure 5.51, Figure 5.52 |
| | Slave output release time | $t_{REL}$ | — | 5 | $t_{PAcyc}$ | |

Note 1. $t_{PBcyc}$: PCLKB cycle

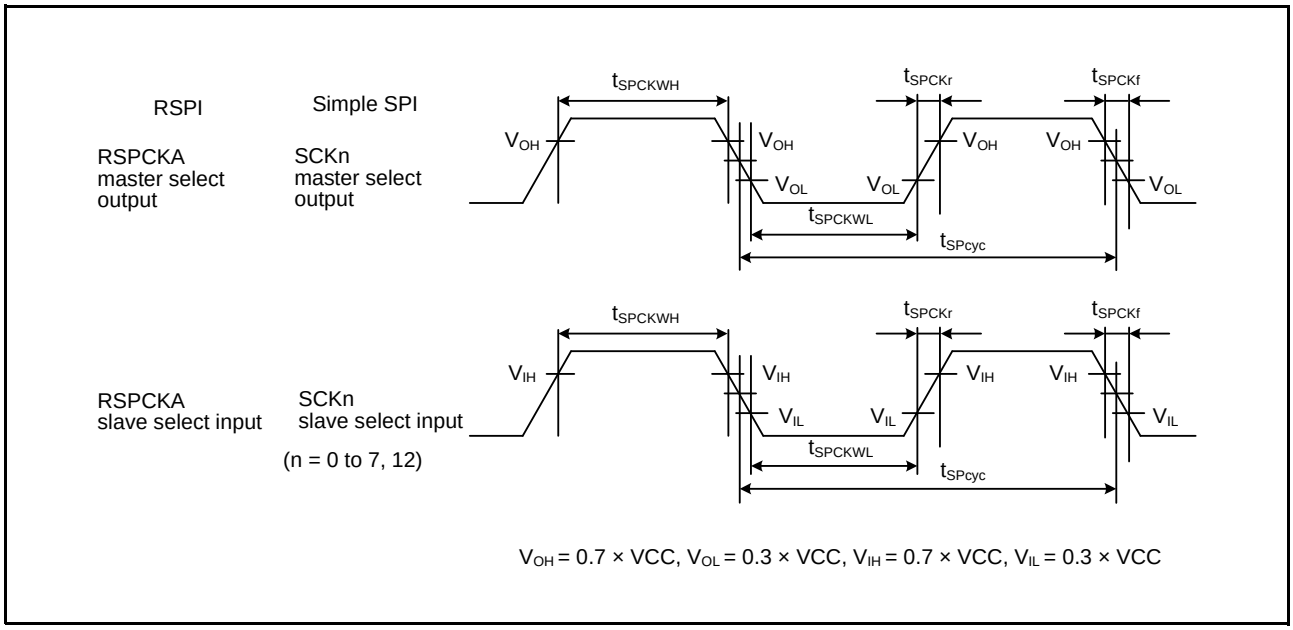



**Figure 5.46 RSPI Clock Timing and Simple SPI Clock Timing**

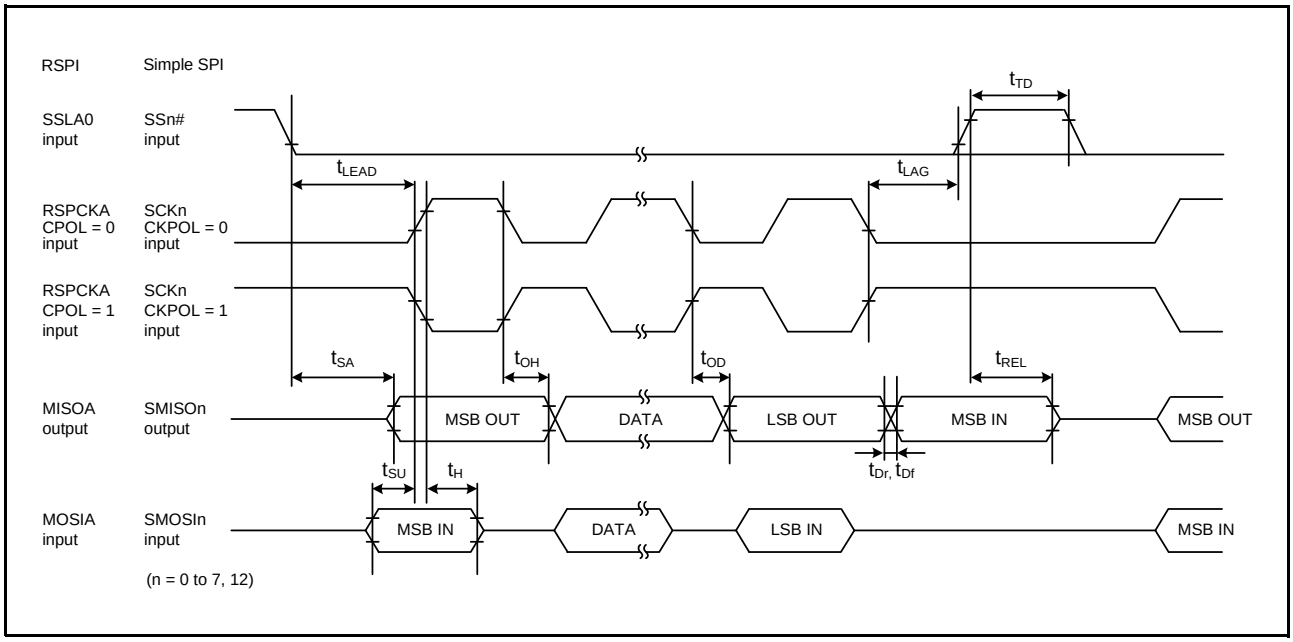



**Figure 5.51 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)**

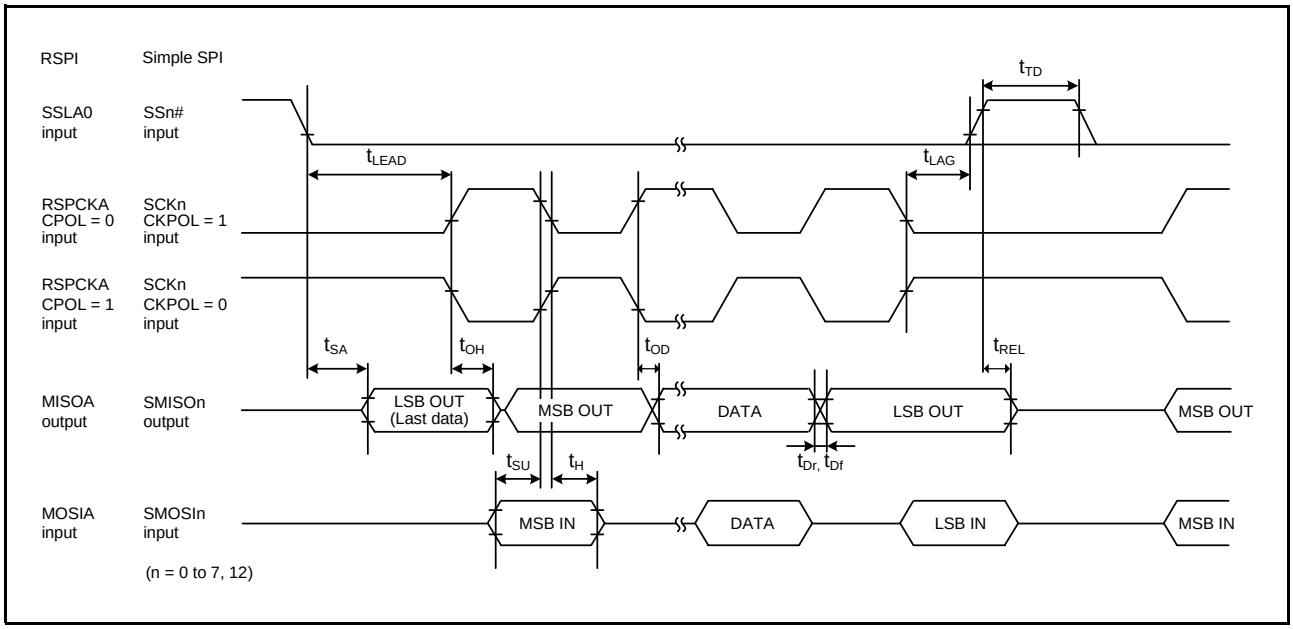



**Figure 5.52 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)**