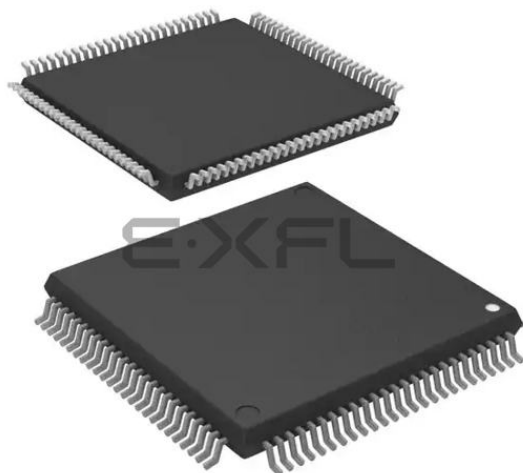




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Details

Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 14x12b; D/A 1x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mjcdfp-v0

Table 1.2 Comparison of Functions for Different Packages (1/2)

Functions		RX71M Group		
Package		177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins
External bus	External bus width	32 bits	16 bits	
	SDRAM area controller	Available		Not supported
DMA	DMA controller	Ch. 0 to 7		
	Data transfer controller	Available		
	EXDMA controller	Ch. 0 and 1		
Timers	16-bit timer pulse unit	Ch. 0 to 5		
	Multi-function timer pulse unit 3	Ch. 0 to 8		
	General-purpose PWM timer	Ch. 0 to 3		
	Port output enable 3	Available		
	Programmable pulse generator	Ch. 0 and 1		
	8-bit timers	Ch. 0 to 3		
	Compare match timer	Ch. 0 to 3		
	Compare match timer W	Ch. 0 and 1		
	Realtime clock	Available		
	Watchdog timer	Available		
	Independent watchdog timer	Available		
	Communication function	Ethernet controller	Ch. 0 and 1	Ch. 0
PTP controller for ethernet controller		Available		
DMAC controller for ethernet		Ch. 0 and 1 (ETHERC) Ch. 2 (EPTPC)	Ch. 0 (ETHERC) and 2 (EPTPC)	
USB 2.0 FS host/function module		Ch. 0		
USB 2.0 HS host/function module with battery charging		Available	Not supported	
Serial communications interfaces (SCIg)		Ch. 0 to 7		Ch. 0 to 3, 5 and 6
Serial communications interfaces (SCIh)		Ch. 12		
Serial communications interfaces with FIFO		Ch. 8 to 11		Ch. 8 and 9
I ² C bus interfaces		Ch. 0 and 2		
Serial peripheral interface		Ch. 0 and 1		
CAN module		Ch. 0 to 2		Ch. 0 and 1
Quad serial peripheral interface		Ch. 0		
Serial sound interfaces		Ch. 0 and 1		
Sampling rate converter		Available		
SD host interface		Ch. 0		
MMC host interface		Ch. 0		
Parallel data capture unit		Available		Not supported
12-bit A/D converter		AN000 to 007 (unit 0: 8 channels) AN100 to 120 (unit 1: 21 channels)		AN000 to 007 (unit 0: 8 channels) AN100 to 113 (unit 1: 14 channels)
12-bit D/A converter		Ch. 0 and 1		Ch. 1
Temperature sensor		Available		
CRC calculator		Available		
Data operation circuit		Available		
Clock frequency accuracy measurement circuit		Available		
AES		Available		

Table 1.3 List of Products (2/3)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX71M	R5F571MFCDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDLC	PTLG0177KA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDLC	PTLG0177KA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDLC	PTLG0177KA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDLCL	PTLG0177KA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDLC	PTLG0177KA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDLCL	PTLG0177KA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDLC	PTLG0177KA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDLCL	PTLG0177KA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDLCL	PTLG0177KA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDLCL	PTLG0177KA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDLC	PTLG0177KA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDLCL	PTLG0177KA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDLCL	PTLG0177KA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDLCL	PTLG0177KA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDLCL	PTLG0177KA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDLCL	PTLG0177KA-A*1	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDLK	PTLG0145KA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDLK	PTLG0145KA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDLK	PTLG0145KA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDLK	PTLG0145KA-A*1	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDLK	PTLG0145KA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDLK	PTLG0145KA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDLK	PTLG0145KA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDLK	PTLG0145KA-A*1	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDLK	PTLG0145KA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDLK	PTLG0145KA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDLC	PTLG0145KA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDLK	PTLG0145KA-A*1	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available

RX71M Group											
PTLG0100JA-A (100-Pin TFLGA)											
(Upper Perspective View)											
	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD/ FINED	RES#	P35	P30	P16	P17	P20	3
2	AVCC1	AVSS0	AVSS1	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (100-Pin TFLGA).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (5/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
110		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ ET0_MDIO		IRQ6-DS	
111	TRDATA3	PG7	D31		ET1_TX_ER			
112		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
113	TRDATA2	PG6	D30		ET1_ETXD3			
114		PA1	A1/DQM3	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOC0B/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
115	VCC							
116	TRCLK	PG5	D29		ET1_ETXD2			
117	VSS							
118		PA0	A0/BC0#/ DQM2	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
119	TRSYNC	PG4	D28		ET1_ETXD1/ RMII1_TXD1			
120		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
121	TRDATA1	PG3	D27		ET1_ETXD0/ RMII1_TXD0			
122		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
123	TRDATA0	PG2	D26		ET1_TX_CLK			
124		P65	CS5#/CKE					
125		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
126		PE6	D14[A14/D14]	MTIOC6C/ GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
127	VCC							
128		P70	SDCLK					
129	VSS							
130		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
131		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
132		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ ET0_ERXD3	MMC_D7-B		AN101
133		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RDX12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
134		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TDX12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
135		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
136		P64	CS4#/WE#					
137		P63	CS3#/CAS#					
138		P62	CS2#/RAS#					
139		P61	CS1#/SDCS#					
140	VSS							

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (7/7)

Pin Number				Timer	Communication	Memory Interface Camera Interface		
176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	(QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
171		P41					IRQ9-DS	AN001
172	VREFL0							
173		P40					IRQ8-DS	AN000
174	VREFH0							
175	AVCC0							
176		P07					IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (4/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
K4		P15		MTIOC0B/MTCLKB/ GTETR-B/TIOC2B/ TCLKB/TMC12/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1	PIXD0	IRQ5	
K5	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
K6		P53	BCLK					
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
K8	VCC							
K9	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
K10		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
K11		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
K12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
K13		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
L1		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1	HSYNC		ADTRG0#
L2		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SSO#/ SSDA3/SSISCK0	PIXD7		
L3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
L4		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
L5		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
L6		P56	EDACK1	MTIOC3C/TIOCA1				
L7		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
L8	TRCLK	P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
L9		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
L10		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETR-D/TMC11/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
L11		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
L12		P73	CS3#	PO16	ET0_WOL			
L13	VSS							
M1		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK	PIXD6		

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (4/4)

Pin Number	Power Supply Clock System Contro	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
80		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
81		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
82		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
83		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
84		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
85		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
86		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
87		P47					IRQ15-DS	AN007
88		P46					IRQ14-DS	AN006
89		P45					IRQ13-DS	AN005
90		P44					IRQ12-DS	AN004
91		P43					IRQ11-DS	AN003
92		P42					IRQ10-DS	AN002
93		P41					IRQ9-DS	AN001
94	VREFL0							
95		P40					IRQ8-DS	AN000
96	VREFH0							
97	AVCC0							
98		P07					IRQ15	ADTRG0#
99	AVSS0							
100	P05						IRQ13	DA1

Table 4.1 List of I/O Registers (Address Order) (34 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C289h	SYSTEM	Deep Standby Interrupt Flag Register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Bh	SYSTEM	Deep Standby Interrupt Edge Register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Dh	SYSTEM	Deep Standby Interrupt Edge Register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-Speed On-Chip Oscillator Power Supply Control Register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LDVA
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Registers 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	RTCd

Table 4.1 List of I/O Registers (Address Order) (40 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0070h	USB0	Pipe1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0072h	USB0	Pipe2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0074h	USB0	Pipe3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0076h	USB0	Pipe4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0078h	USB0	Pipe5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 007Ah	USB0	Pipe6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 007Ch	USB0	Pipe7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 007Eh	USB0	Pipe8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb

Table 4.1 List of I/O Registers (Address Order) (41 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
000A 0080h	USB0	Pipe9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 009Ah	USB0	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 009Ch	USB0	Pipe4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 009Eh	USB0	Pipe4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00A0h	USB0	Pipe5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00A2h	USB0	Pipe5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00F0h	USB0	PHY Cross Point Adjustment Register	PHYSLEW	32	32	9 PCLKB or more	Frequency with 1 + 9 $\times$ (frequency ratio of ICLK/PCLKB) ^{*5}	USBb

Table 4.1 List of I/O Registers (Address Order) (46 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1201h	MTU4	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1210h	MTU3	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1212h	MTU4	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1218h	MTU3	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1224h	MTU3	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1228h	MTU4	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 122Ch	MTU3	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1231h	MTU	Timer Interrupt Skipping Counter 1A	TITCNT1A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1234h	MTU	Timer Dead Time Enable Register A	TDERA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1236h	MTU	Timer Output Level Buffer Register A	TOLBRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 123Ch	MTU	Timer Interrupt Skipping Counter 2A	TITCNT2A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 124Ch	MTU3	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 124Dh	MTU4	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (50 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 200Ch	GPT	General PWM Timer Write-Protection Register	GTWP	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 200Eh	GPT	General PWM Timer Sync Register	GTSYNC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register	GTBDR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2018h	GPT	General PWM Timer Start Write-Protection Register	GTSWP	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2100h	GPT0	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2104h	GPT0	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2106h	GPT0	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2108h	GPT0	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 210Ah	GPT0	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 210Ch	GPT0	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 210Eh	GPT0	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2110h	GPT0	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2112h	GPT0	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2114h	GPT0	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2116h	GPT0	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2118h	GPT0	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 211Ah	GPT0	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 211Ch	GPT0	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 211Eh	GPT0	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2120h	GPT0	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2124h	GPT0	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2126h	GPT0	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2128h	GPT0	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 212Ch	GPT0	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 212Eh	GPT0	A/D Converter Start Request Timing Buffer Register B	GTADTB RB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2130h	GPT0	A/D Converter Start Request Timing Double-Buffer Register B	GTADTD RB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2134h	GPT0	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2136h	GPT0	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2138h	GPT0	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 213Ah	GPT0	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 213Ch	GPT0	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 213Eh	GPT0	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2140h	GPT0	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2142h	GPT0	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2180h	GPT1	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2182h	GPT1	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2184h	GPT1	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2186h	GPT1	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2188h	GPT1	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa

Table 4.1 List of I/O Registers (Address Order) (52 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 2228h	GPT2	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2230h	GPT2	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTa
000C 4000h	EPTPC	MINT Interrupt Source Status Register	MIESR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPCa

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Schmitt trigger input voltage	IRQ input pin*1	V_{IH}	$VCC \times 0.8$	—	$VCC + 0.3$	V		
	MTU input pin*1	V_{IL}	−0.3	—	$VCC \times 0.2$			
	GPT input pin*1	ΔV_T	$VCC \times 0.06$	—	—			
	POE3 input pin*1							
	TPU input pin*1							
	TMR input pin*1							
	SCI input pin*1							
	ADTRG# input pin*1							
	QSPI input pin*1	RIIC input pin (except for SMBus)	V_{IH}	$VCC \times 0.7$	—			5.8
	RES#, NMI, TCK		V_{IL}	−0.3	—			$VCC \times 0.3$
			ΔV_T	$VCC \times 0.05$	—			—
	Ports for 5 V tolerant*2		V_{IH}	$VCC \times 0.8$	—			5.8
	V_{IL}		−0.3	—	$VCC \times 0.2$			
Other input pins excluding ports for 5 V tolerant*3	V_{IH}		$VCC \times 0.8$	—	$VCC + 0.3$			
	V_{IL}	−0.3	—	$VCC \times 0.2$				
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	$VCC \times 0.9$	—	$VCC + 0.3$	V		
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SSI input pin, SDHI input pin, MMC input pin, PDC input pin		$VCC \times 0.8$	—	$VCC + 0.3$			
	ETHERC input pin		2.3	—	$VCC + 0.3$			
	XCIN*3		$VCC \times 0.8$	—	$VCC + 0.3$			
	D0 to D31		$VCC \times 0.7$	—	$VCC + 0.3$			
	RIIC (SMBus)		2.1	—	$VCC + 0.3$			
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	−0.3	—	$VCC \times 0.1$	V		
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SSI input pin, SDHI input pin, MMC input pin, PDC input pin		−0.3	—	$VCC \times 0.2$			
	XCIN*3		−0.3	—	$VCC \times 0.2$			
	D0 to D31		−0.3	—	$VCC \times 0.3$			
	RIIC (SMBus)		−0.3	—	0.8			

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.

Note 2. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 3. For P32, P31, P30, and XCIN, input as follows when the V_{BATT} power supply is selected.

V_{IH} Min. = $V_{BATT} \times 0.8$, V_{IH} Max. = $V_{BATT} + 0.3$, V_{IL} Min. = -0.3 , V_{IL} Max. = $V_{BATT} \times 0.2$ ($V_{BATT} = 2.0$ to 3.6 V)

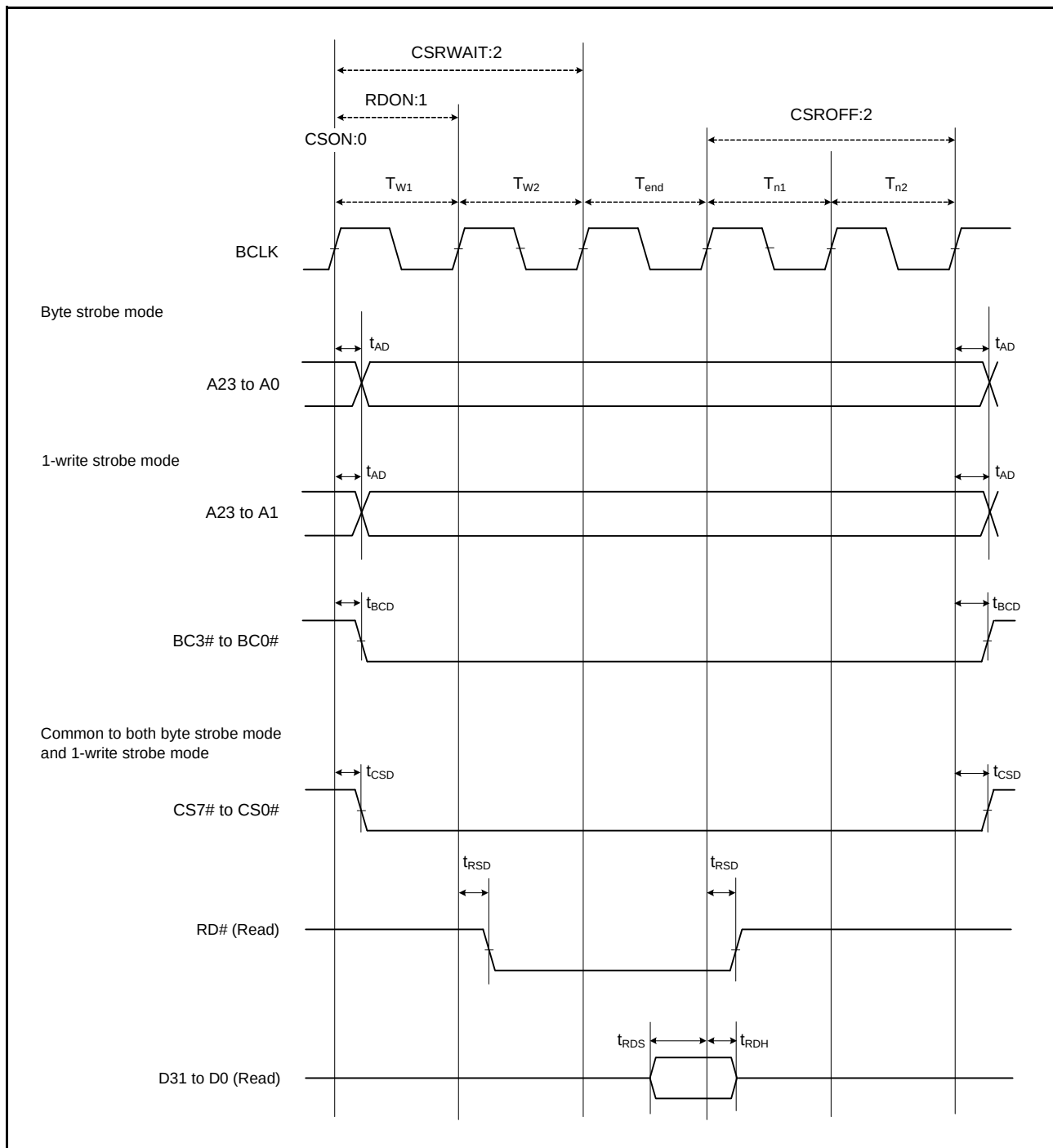
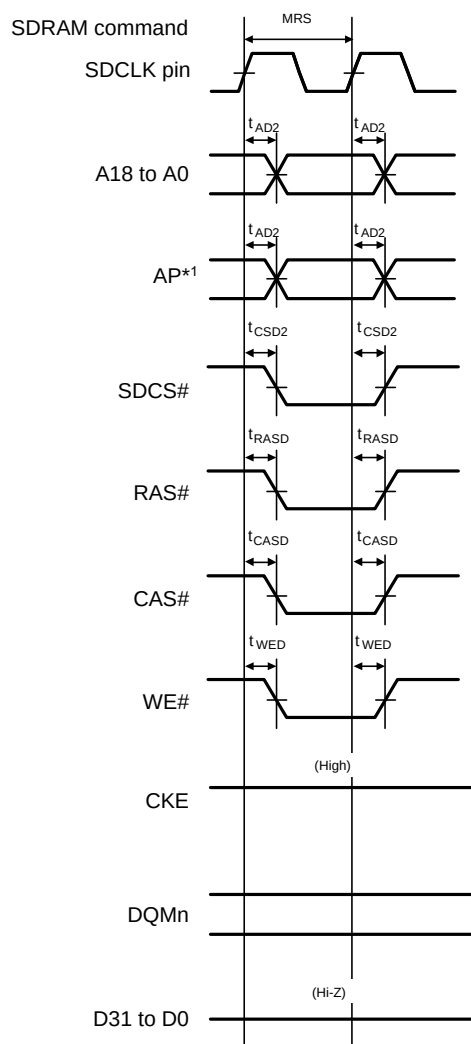


Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.28 SDRAM Space Mode Register Set Bus Timing

Table 5.55 Data Flash Memory Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,

$V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V

$V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,

Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{DP4}	—	0.66	3.8	—	0.3	1.7	ms
Erase time	64 bytes	t_{DE64}	—	5.4	18	—	3	10	ms
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	30	μs
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	Times
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t_{DSESD1}	—	—	216	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t_{DSESD2}	—	—	300	—	—	300	μs
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	—	—	300	μs
Forced stop command		t_{FD}	—	TBD	32	—	—	20	μs
Data hold time*3		t_{DDRP}	10	—	—	10	—	—	Year

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 100000$), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

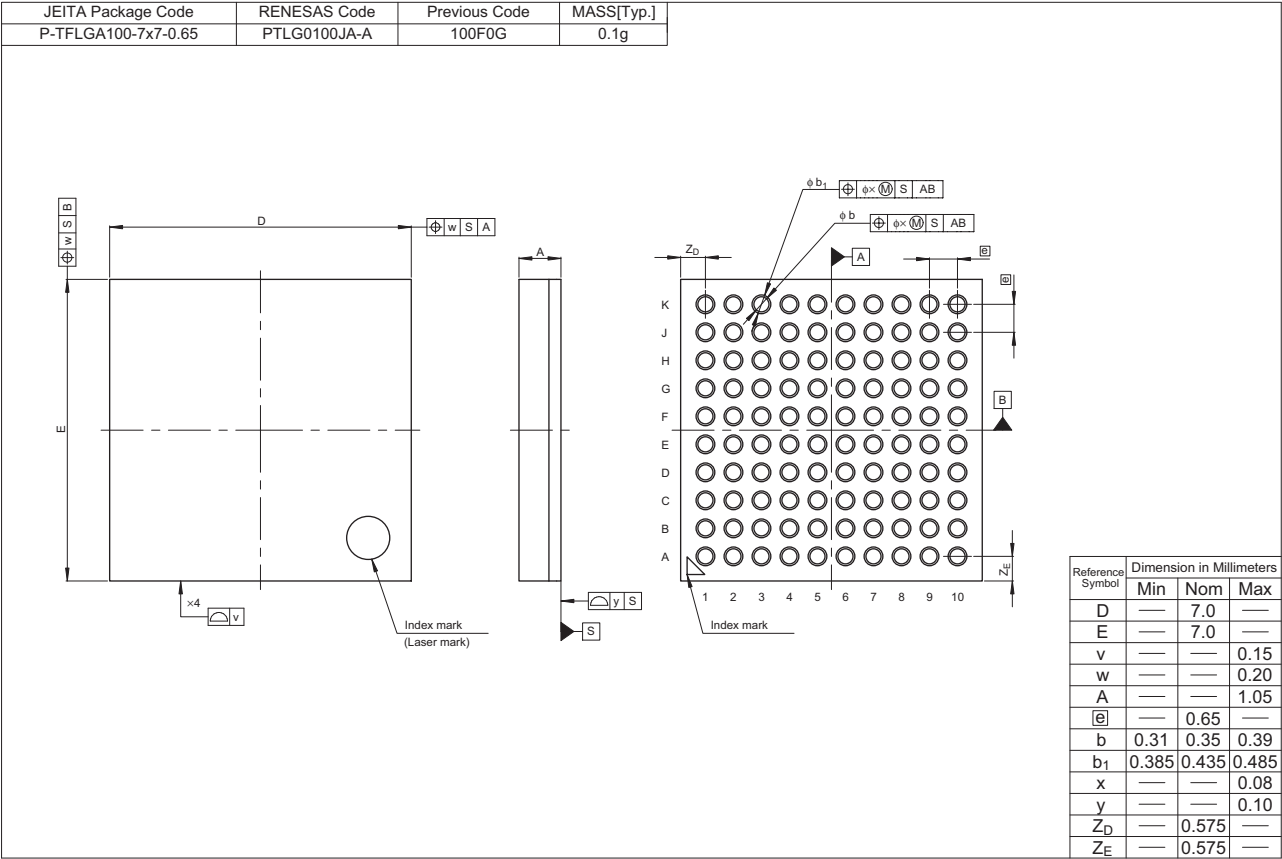


Figure F 100-Pin TFLGA (PTLG0100JA-A)

REVISION HISTORY	RX71M Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jan 15, 2015	—	First edition, issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.