Renesas Electronics America Inc - R5F571MJGDFC#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mjgdfc-v0

Table 1.2 Comparison of Functions for Different Packages (2/2)

Functions	RX71M Group		
Package	**177 Pins, 176 Pins**	**145 Pins, 144 Pins**	**100 Pins**
DES	Available		
SHA	Available		
RNG	Available		
Event link controller	Available		

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strove signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU or GPT in the high impedance state

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	RXD0 to RXD7	Input	Input pins for received data
	TXD0 to TXD7	Output	Output pins for transmitted data
	CTS0# to CTS7#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS7#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL7	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA7	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	SMISO0 to SMISO7	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI7	I/O	Input/output pins for master transmission of data
	SS0# to SS7#	Input	Chip-select input pins
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface with FIFO (SCIFA)	SCK8 to SCK11	I/O	Input/output pins for the clock
	RXD8 to RXD11	Input	Input pins for received data
	TXD8 to TXD11	Output	Output pins for transmitted data
	CTS8# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS8# to RTS11#	Output	Output pins for controlling the start of transmission and reception
I^2C bus interface	SCL0[FM+], SCL2	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA2	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

RX71M Group
PTLG0100JA-A (100-Pin TFLGA)
(Upper Perspective View)

	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD/ FINED	RES#	P35	P30	P16	P17	P20	3
2	AVCC1	AVSS0	AVSS1	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (100-Pin TFLGA).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (1/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
A1	AVSS0							
A2		P07					IRQ15	ADTRG0#
A3		P40					IRQ8-DS	AN000
A4		P42					IRQ10-DS	AN002
A5		P45					IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7			AN114
A7		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
A8		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
A9		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
A10	VSS							
A11		P62	CS2#/RAS#					
A12		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3/	MMC_D7-B		AN101
B1	AVCC1							
B2	AVCC0							
B3		P05					IRQ13	DA1
B4	VREFL0							
B5		P43					IRQ11-DS	AN003
B6		P47					IRQ15-DS	AN007
B7		P91	A17		SCK7			AN115
B8		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
B9		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
B10	VCC							
B11		P61	CS1#/SDCS#					
B12		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
C1	AVSS1							
C2		P02		TMCI1	SCK6		IRQ10	AN120
C3	VREFH0							
C4		P41					IRQ9-DS	AN001
C5		P46					IRQ14-DS	AN006
C6	VSS							
C7		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
C8		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
C9		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
C10		P63	CS3#/CAS#					
C11		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
C12		P70	SDCLK					
C13	VSS							
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6		IRQ8	AN118
D2		PF5					IRQ4	
D3		P03					IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6		IRQ9	AN119
D5	VCC							
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
D8		P60	CS0#					
D9		P64	CS4#/WE#					
D10		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D11	VCC							
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
D13		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/ TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
E1	VSS							
E2	VCL							
E3		PJ5		POE8#	CTS2#/RTS2#/SS2#			
E4	EMLE							
E5		P44					IRQ12-DS	AN004
E10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
E11		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
E12		P65	CS5#/CKE					
E13		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
F1	XCIN							
F2	XCOUT							
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/ RTS6#/CTS0#/RTS0#/ SS6#/SS0#			
F4	VBATT							
F10		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
F11	VSS							
F12		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (5/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
M2		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
M3		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
M4		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
M5	VCC_USB							
M6	VSS_USB							
M7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
M8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
M10		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		
M11		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
M12		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
M13	VCC							
N1		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0	PIXD5	IRQ9	
N2		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0	PIXD4	IRQ8	
N3		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
N4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
N5					USB0_DM			
N6					USB0_DP			
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
N8	VSS							
N9	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
N11		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
N12		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
N13		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/4)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	
H9		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
H10		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
J1		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1			
J2		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0		IRQ9	
J3		P17		MTIOC3A/MTIOC3B/ MTIOC4B/GTIOC0B-B/TIOCB0/TCLKD/ TMO1/PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0		IRQ7	ADTRG1#
J4		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
J5	VSS_USB							
J6	VCC_USB							
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/SSLA0-A/ET0_TX_CLK			
J9		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
J10		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
K1		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0			
K2		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK			
K3		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0		IRQ8	
K4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
K5					USB0_DM			
K6					USB0_DP			
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2			
K9		PC3	A19	MTIOC4D/GTIOC1B-D/TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
K10		PC2	A18	MTIOC4B/GTIOC2B-D/TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (2/4)

Pin Number 100-Pin LQFP	Power Supply Clock System Contro	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
30		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
31		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1		IRQ5	
32		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
33		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
34		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
35	VCC_USB							
36					USB0_DM			
37					USB0_DP			
38	VSS_USB							
39		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
40		P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
41		P53	BCLK					
42		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
43		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
44		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
45	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL		IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2			
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK			
49		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
50		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			
51		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
54		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes
0008 0002h	SYSTEM	Mode Status Register	MDSR	16	16	3 ICLK		Operating Modes
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK		Operating Modes
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK		Operating Modes
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK		Low Power Consumption
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK		Low Power Consumption
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK		Low Power Consumption
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK		Low Power Consumption
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit
0008 0024h	SYSTEM	System Clock Control Register 2	SCKCR2	16	16	3 ICLK		Clock Generation Circuit
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK		Clock Generation Circuit
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK		Clock Generation Circuit
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK		Clock Generation Circuit
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK		Clock Generation Circuit
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK		Clock Generation Circuit
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK		Clock Generation Circuit
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK		Clock Generation Circuit
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK		Clock Generation Circuit
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK		Clock Generation Circuit
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK		Clock Generation Circuit

Table 4.1 List of I/O Registers (Address Order) (2 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK		Clock Generation Circuit
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK		Clock Generation Circuit
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK		Clock Generation Circuit
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK		Low Power Consumption
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK		Low Power Consumption
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00A3h	SYSTEM	Sub-Clock Oscillator Wait Control Register	SOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK		Resets
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LDVA
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK		LDVA
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK		LDVA
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK		LDVA
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function
0008 1200h	RAM	RAM Operating Mode Control Register	RAMMODE	8	8	2 ICLK		RAM
0008 1201h	RAM	RAM Error Status Register	RAMSTS	8	8	2 ICLK		RAM
0008 1204h	RAM	RAM Protection Register	RAMPRCR	8	8	2 ICLK		RAM
0008 1208h	RAM	RAM Error Address Capture Register	RAMECAD	32	32	2 ICLK		RAM
0008 12C0h	ECCRAM	ECCRAM Operating Mode Control Register	ECCRAMMODE	8	8	2 ICLK		RAM
0008 12C1h	ECCRAM	ECCRAM 2-Bit Error Status Register	ECCRAM2STS	8	8	2 ICLK		RAM
0008 12C2h	ECCRAM	ECCRAM 1-Bit Error Information Update Enable Register	ECCRAM1STSEN	8	8	2 ICLK		RAM
0008 12C3h	ECCRAM	ECCRAM 1-Bit Error Status Register	ECCRAM1STS	8	8	2 ICLK		RAM
0008 12C4h	ECCRAM	ECCRAM Protection Register	ECCRAMPRCR	8	8	2 ICLK		RAM
0008 12C8h	ECCRAM	ECCRAM 2-Bit Error Address Capture Register	ECCRAM2ECAD	32	32	2 ICLK		RAM
0008 12CCh	ECCRAM	ECCRAM 1-Bit Error Address Capture Register	ECCRAM1ECAD	32	32	2 ICLK		RAM
0008 12D0h	ECCRAM	ECCRAM Protection Register 2	ECCRAMPRCR2	8	8	2 ICLK		RAM
0008 12D4h	ECCRAM	ECCRAM Test Control Register	ECCRAMETST	8	8	2 ICLK		RAM
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK		Buses
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK		Buses

Table 4.1 List of I/O Registers (Address Order) (6 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 2BE8h	EXDMAC	Cluster Buffer Register 2	CLSBR2	32	32	1, 2 BCLK		EXDMACa
0008 2BECh	EXDMAC	Cluster Buffer Register 3	CLSBR3	32	32	1, 2 BCLK		EXDMACa
0008 2BF0h	EXDMAC	Cluster Buffer Register 4	CLSBR4	32	32	1, 2 BCLK		EXDMACa
0008 2BF4h	EXDMAC	Cluster Buffer Register 5	CLSBR5	32	32	1, 2 BCLK		EXDMACa
0008 2BF8h	EXDMAC	Cluster Buffer Register 6	CLSBR6	32	32	1, 2 BCLK		EXDMACa
0008 2BFCh	EXDMAC	Cluster Buffer Register 7	CLSBR7	32	32	1, 2 BCLK		EXDMACa
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1, 2 BCLK		Buses
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1, 2 BCLK		Buses
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1, 2 BCLK		Buses
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1, 2 BCLK		Buses
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1, 2 BCLK		Buses
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1, 2 BCLK		Buses
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1, 2 BCLK		Buses
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1, 2 BCLK		Buses
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1, 2 BCLK		Buses
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1, 2 BCLK		Buses
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1, 2 BCLK		Buses
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1, 2 BCLK		Buses
0008 3042h	BSC	CS4 Mode Register	CS4MOD	16	16	1, 2 BCLK		Buses
0008 3044h	BSC	CS4 Wait Control Register 1	CS4WCR1	32	32	1, 2 BCLK		Buses
0008 3048h	BSC	CS4 Wait Control Register 2	CS4WCR2	32	32	1, 2 BCLK		Buses
0008 3052h	BSC	CS5 Mode Register	CS5MOD	16	16	1, 2 BCLK		Buses
0008 3054h	BSC	CS5 Wait Control Register 1	CS5WCR1	32	32	1, 2 BCLK		Buses
0008 3058h	BSC	CS5 Wait Control Register 2	CS5WCR2	32	32	1, 2 BCLK		Buses
0008 3062h	BSC	CS6 Mode Register	CS6MOD	16	16	1, 2 BCLK		Buses
0008 3064h	BSC	CS6 Wait Control Register 1	CS6WCR1	32	32	1, 2 BCLK		Buses
0008 3068h	BSC	CS6 Wait Control Register 2	CS6WCR2	32	32	1, 2 BCLK		Buses
0008 3072h	BSC	CS7 Mode Register	CS7MOD	16	16	1, 2 BCLK		Buses
0008 3074h	BSC	CS7 Wait Control Register 1	CS7WCR1	32	32	1, 2 BCLK		Buses
0008 3078h	BSC	CS7 Wait Control Register 2	CS7WCR2	32	32	1, 2 BCLK		Buses
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1, 2 BCLK		Buses
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1, 2 BCLK		Buses
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1, 2 BCLK		Buses
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1, 2 BCLK		Buses
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK		Buses
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK		Buses
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK		Buses
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK		Buses
0008 3842h	BSC	CS4 Control Register	CS4CR	16	16	1, 2 BCLK		Buses
0008 384Ah	BSC	CS4 Recovery Cycle Register	CS4REC	16	16	1, 2 BCLK		Buses
0008 3852h	BSC	CS5 Control Register	CS5CR	16	16	1, 2 BCLK		Buses
0008 385Ah	BSC	CS5 Recovery Cycle Register	CS5REC	16	16	1, 2 BCLK		Buses
0008 3862h	BSC	CS6 Control Register	CS6CR	16	16	1, 2 BCLK		Buses
0008 386Ah	BSC	CS6 Recovery Cycle Register	CS6REC	16	16	1, 2 BCLK		Buses
0008 3872h	BSC	CS7 Control Register	CS7CR	16	16	1, 2 BCLK		Buses
0008 387Ah	BSC	CS7 Recovery Cycle Register	CS7REC	16	16	1, 2 BCLK		Buses

Table 4.1 List of I/O Registers (Address Order) (19 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9161h	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9170h	S12AD1	A/D Sampling State Register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9171h	S12AD1	A/D Sampling State Register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9176h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9177h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9178h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9179h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 917Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9184h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9186h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9190h	S12AD1	A/D Compare Control Register	ADCMPCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9192h	S12AD1	A/D Compare Channel Select Extended Register	ADCMPANSER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9193h	S12AD1	A/D Compare Level Extended Register	ADCMPLER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9194h	S12AD1	A/D Compare Channel Select Register 0	ADCMPANSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9196h	S12AD1	A/D Compare Channel Select Register 1	ADCMPANSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9198h	S12AD1	A/D Compare Level Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ah	S12AD1	A/D Compare Level Register 1	ADCMPLR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ch	S12AD1	A/D Compare Data Register 0	ADCMPDR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Eh	S12AD1	A/D Compare Data Register 1	ADCMPDR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A0h	S12AD1	A/D Compare Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A2h	S12AD1	A/D Compare Status Register 1	ADCMPSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A4h	S12AD1	A/D Compare Status Extended Register	ADCMPSER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9E00h	QSPI	QSPI Control Register	SPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E01h	QSPI	QSPI Slave Select Polarity Register	SSLP	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E02h	QSPI	QSPI Pin Control Register	SPPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E03h	QSPI	QSPI Status Register	SPSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E04h	QSPI	QSPI Data Register	SPDR	32	8, 16, 32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E08h	QSPI	QSPI Sequence Control Register	SPSCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E09h	QSPI	QSPI Sequence Status Register	SPSSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ah	QSPI	QSPI Bit Rate Register	SPBR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Bh	QSPI	QSPI Data Control Register	SPDCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ch	QSPI	QSPI Clock Delay Register	SPCKD	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Dh	QSPI	QSPI Slave Select Negation Delay Register	SSLND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Eh	QSPI	QSPI Next-Access Delay Register	SPND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E10h	QSPI	QSPI Command Register 0	SPCMD0	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E12h	QSPI	QSPI Command Register 1	SPCMD1	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E14h	QSPI	QSPI Command Register 2	SPCMD2	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E16h	QSPI	QSPI Command Register 3	SPCMD3	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E18h	QSPI	QSPI Buffer Control Register	SPBFCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ah	QSPI	QSPI Buffer Data Count Register	SPBDCR	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ch	QSPI	QSPI Transfer Data Length Multiplier Setting Register 0	SPBMUL0	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E20h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 1	SPBMUL1	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI

Table 4.1 List of I/O Registers (Address Order) (20 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9E24h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 2	SPBMUL2	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E28h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 3	SPBMUL3	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A00Eh	SCI0	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A00Fh	SCI0	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A00Eh	SCI0	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh
0008 A010h	SCI0	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A011h	SCI0	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A010h	SCI0	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh
0008 A012h	SCI0	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh

Table 4.1 List of I/O Registers (Address Order) (53 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4004h	EPTPC	MINT Interrupt Request Permission Register	MIEIPR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPCa
000C 4010h	EPTPC	ELC Output/IPLS Interrupt Request Permission Register	ELIPPR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPCa
000C 4014h	EPTPC	ELC Output/IPLS Interrupt Permission Automatic Clearing Register	ELIPACR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPCa
000C 4040h	EPTPC	STCA Status Register	STSR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4044h	EPTPC	STCA Status Notification Permission Register	STIPR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4050h	EPTPC	STCA Clock Frequency Setting Register	STCFR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4054h	EPTPC	STCA Operating Mode Register	STMR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4058h	EPTPC	Sync Message Reception Timeout Register	SYNTOR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4060h	EPTPC	IPLS Interrupt Request Timer Select Register	IPTSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4064h	EPTPC	MINT Interrupt Request Timer Select Register	MITSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4068h	EPTPC	ELC Output Timer Select Register	ELTSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 406Ch	EPTPC	Time Synchronization Channel Select Register	STCHSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4080h	EPTPC	Slave Time Synchronization Start Register	SYNSTARTR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4084h	EPTPC	Local Time Counter Initial Value Load Directive Register	LCIVLDR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4090h	EPTPC	Synchronization Loss Detection Threshold Register	SYNTDARU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4094h	EPTPC	Synchronization Loss Detection Threshold Register	SYNTDARL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4098h	EPTPC	Synchronization Detection Threshold Register	SYNTDBRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 409Ch	EPTPC	Synchronization Detection Threshold Register	SYNTDBRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 40B0h	EPTPC	Local Time Counter Initial Value Register	LCIVRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 40B4h	EPTPC	Local Time Counter Initial Value Register	LCIVRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 40B8h	EPTPC	Local Time Counter Initial Value Register	LCIVRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4124h	EPTPC	Worst 10 Acquisition Directive Register	GETW10R	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4128h	EPTPC	Positive Gradient Limit Register	PLIMITRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 412Ch	EPTPC	Positive Gradient Limit Register	PLIMITRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4130h	EPTPC	Positive Gradient Limit Register	PLIMITRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4134h	EPTPC	Negative Gradient Limit Register	MLIMITRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4138h	EPTPC	Negative Gradient Limit Register	MLIMITRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 413Ch	EPTPC	Negative Gradient Limit Register	MLIMITRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4140h	EPTPC	Statistical Information Retention Control Register	GETINFOR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4170h	EPTPC	Local Time Counter	LCCVRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4174h	EPTPC	Local Time Counter	LCCVRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4178h	EPTPC	Local Time Counter	LCCVRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4210h	EPTPC	Positive Gradient Worst 10 Value Register	PW10VRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4214h	EPTPC	Positive Gradient Worst 10 Value Register	PW10VRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4218h	EPTPC	Positive Gradient Worst 10 Value Register	PW10VRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 42D0h	EPTPC	Negative Gradient Worst 10 Value Register	MW10RU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 42D4h	EPTPC	Negative Gradient Worst 10 Value Register	MW10RM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 42D8h	EPTPC	Negative Gradient Worst 10 Value Register	MW10RL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4300h	EPTPC	Timer Start Time Setting Register	TMSTTRU0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4304h	EPTPC	Timer Start Time Setting Register	TMSTTRL0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4308h	EPTPC	Timer Cycle Setting Register 0	TMCYCR0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 430Ch	EPTPC	Timer Pulse Width Setting Register 0	TMPLSR0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4310h	EPTPC	Timer Start Time Setting Register	TMSTTRU1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4314h	EPTPC	Timer Start Time Setting Register	TMSTTRL1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4318h	EPTPC	Timer Cycle Setting Register 1	TMCYCR1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 431Ch	EPTPC	Timer Pulse Width Setting Register 1	TMPLSR1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4320h	EPTPC	Timer Start Time Setting Register	TMSTTRU2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4324h	EPTPC	Timer Start Time Setting Register	TMSTTRL2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa

Table 5.27 MTU3 Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU3	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PAcyc}	Figure 5.38
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PAcyc}	Figure 5.39
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PAcyc}: PCLKA cycle

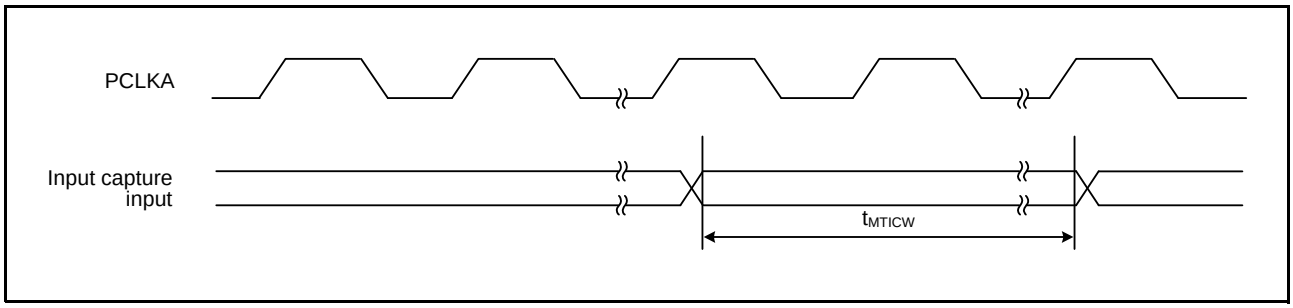


Figure 5.38 MTU3 Input Capture Input Timing

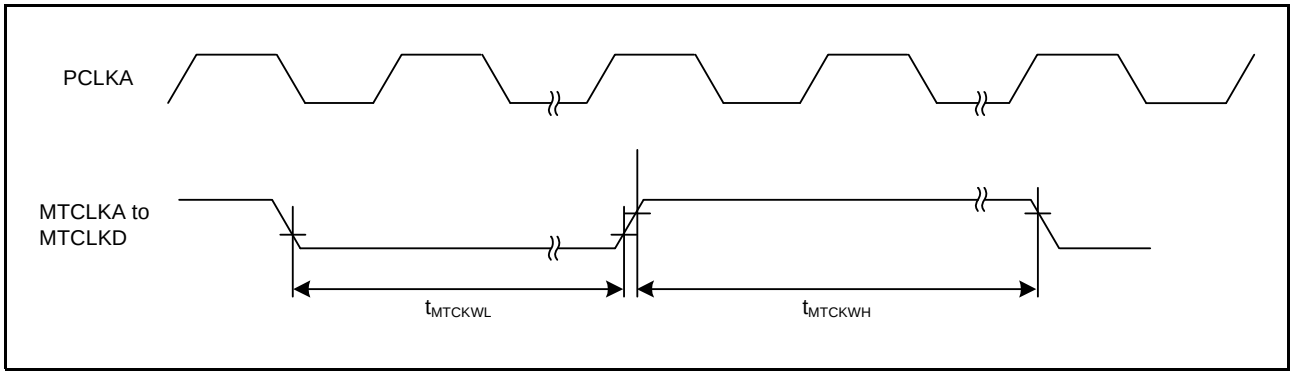


Figure 5.39 MTU3 Clock Input Timing

Table 5.28 POE3 Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
POE	POE# input pulse width	t_{POEW}	1.5	—	t_{PBcyc}	Figure 5.40

Note 1. t_{PBcyc}: PCLKB cycle

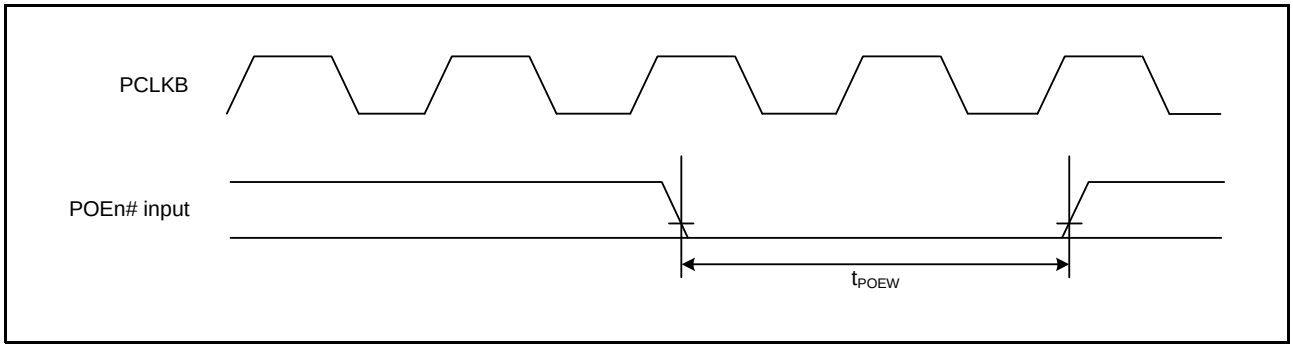


Figure 5.40 POE# Input Timing

Table 5.36 RIIC Timing (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 5.56
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage / 5.5 V)	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage / 5.5 V)	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

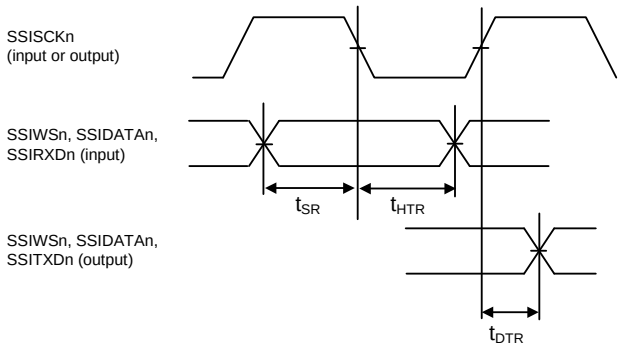
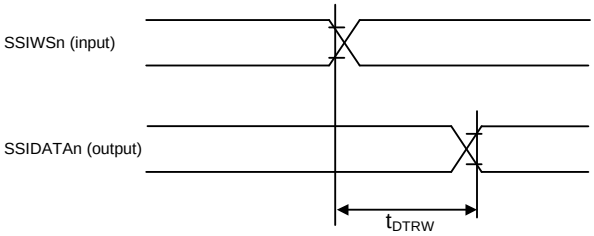


Figure 5.59 Transmit/Receive Timing (SSISCKn Falling Synchronous)



MSB bit output timing in slave transmission from SSIWSn with the settings of DEL = 1, SDTA = 0, or DEL = 1, SDTA = 1, SWL[2:0] = DWL[2:0]

Figure 5.60 SSIDATA Output Delay from SSIWSn Change Edge

5.6 D/A Conversion Characteristics

Table 5.49 D/A Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V,
2.7 ≤ VREFH0 ≤ AVCC0, VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Without AMP output	Absolute accuracy	—	—	±6.0	LSB	2-MΩ resistive load 10-bit conversion
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	2-MΩ resistive load
	RO output resistance	—	7.5	—	kΩ	
	Conversion time	—	—	3.0	µs	20-pF capacitive load
With AMP output	Resistive load	5	—	—	kΩ	
	Capacitive load	—		50	pF	
	Output voltage range	0.2	—	AVCC1 – 0.2	V	
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	
	INL integral nonlinearity error	—	±2.0	±4.0	LSB	
	Conversion time	—	—	4.0	µs	

5.7 Temperature Sensor Characteristics

Table 5.50 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage (at 25°C)	—	1.24	—	V	
Temperature sensor start time	—	—	30	µs	
Sampling time	4.15	—	—	µs	ADSSTRT.SST[7:0] = 250 states