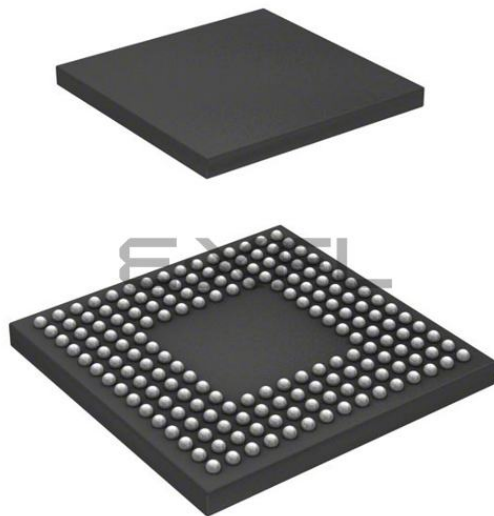




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mjhdbg-20

Table 1.1 Outline of Specifications (7/10)

Classification	Module/Function	Description
Communication function	I ² C bus interface (R1ICa)	2 channels (only channel 0 can be used in fast-mode plus) - Communication formats - I²C bus format/SMBus format - Supports the multi-master - Max. transfer rate: 1 Mbps (channel 0) - Event linking by the ELC
	CAN module (CAN)	3 channels - Compliance with the ISO11898-1 specification (standard frame and extended frame) 32 mailboxes per channel
	Serial peripheral interface (RSPIa)	2 channels - RSPI transfer facility - Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) - Capable of handling serial transfer as a master or slave - Data formats - Switching between MSB first and LSB first - The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception - Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) - Buffered structure - Double buffers for both transmission and reception - RSPCK can be stopped with the receive buffer full for master reception. - Event linking by the ELC
	Quad serial peripheral interface (QSPI)	1 channel - Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation) - Programmable bit length and selectable active sense and phase of the clock signal - Sequential execution of transfer - LSB or MSB first is selectable.
Serial sound interface (SSI)		2 channels - Full-duplex transfer is possible (only on channel 0). - Support for multiple audio formats - Support for master or slave operation - Bit clock frequency is selectable from four different types (16 fs, 32 fs, 48 fs, and 64 fs). - Support for 8-/16-/18-/20-/22-/24 bit data formats - Internal 8-stage FIFO for transmission and reception - Stopping SSIWS when data transfer is stopped is selectable.
Sampling rate converter (SRC)		1 channel - Data formats: 32-bit stereo (16 bits for the left, 16 bits for the right) and 16-bit monaural. - Input sampling rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz - Output sampling rates: 32, 44.1, 48, 8*2 or 16 kHz*2
SD host interface (SDHI)*4		1 channel - One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) - SD specifications - Part 1: Physical Layer Specification Ver.3.01 compliant (DDR not supported) - Part E1: SDIO Specification Ver. 3.00 - Error checking: CRC7 for commands and CRC16 for data - Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt - DMA transfer requests: SD_BUF write and SD_BUF read - Support for card detection and write protection
MMC host interface (MMCIF)		1 channel - Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported) - Interface for Multimedia Cards (MMCs) - Device buses: Support for 1-, 4-, and 8-bit MMC buses - Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt - DMA transfer requests: CE_DATA write and CE_DATA read - Support for card detection, boot operation, high priority interrupt (HPI)

Table 1.1 Outline of Specifications (10/10)

Classification	Module/Function	Description
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.

Note 2. Setting is only possible when the input sampling rate 44.1 kHz is selected.

Note 3. The product part number differs according to whether or not it supports encryption.

Note 4. The product part number differs according to whether or not it includes an SDHI (SD host interface).

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	RXD0 to RXD7	Input	Input pins for received data
	TXD0 to TXD7	Output	Output pins for transmitted data
	CTS0# to CTS7#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS7#	Output	Output pins for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL0 to SSCL7	I/O	Input/output pins for the I ² C clock
	SSDA0 to SSDA7	I/O	Input/output pins for the I ² C data
	• Simple SPI mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	SMISO0 to SMISO7	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI7	I/O	Input/output pins for master transmission of data
	SS0# to SS7#	Input	Chip-select input pins
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock
	SSDA12	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface with FIFO (SCIFA)	SCK8 to SCK11	I/O	Input/output pins for the clock
	RXD8 to RXD11	Input	Input pins for received data
	TXD8 to TXD11	Output	Output pins for transmitted data
	CTS8# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS8# to RTS11#	Output	Output pins for controlling the start of transmission and reception
I ² C bus interface	SCL0[FM+], SCL2	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA2	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

Table 1.4 Pin Functions (7/8)

Classifications	Pin Name	I/O	Description
MMC host interface	MMC_CLK-A/ MMC_CLK-B	Output	MMC clock pin
	MMC_CMD-A/ MMC_CMD-B	I/O	Command/response pin
	MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B	I/O	Transmit data/receive data
	MMC_CD-A/MMC_CD-B	Input	Card detection pin
	MMC_RES#-A/MMC_RES#-B	Output	MMC reset output pin
SD host interface	SDHI_CLK-A/SDHI_CLK-B	Output	SD clock output pin
	SDHI_CMD-A/SDHI_CMD-B	I/O	SD command output, response input signal pin
	SDHI_D3-A/SDHI_D3-B to SDHI_D0-A/SDHI_D0-B	I/O	SD data bus pins
	SDHI_CD-A/SDHI_CD-B	Input	SD card detection pin
	SDHI_WP-A/SDHI_WP-B	Input	SD write-protect signal
Parallel data capture unit	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
12-bit A/D converter	AN000 to AN007, AN100 to AN120	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	AVCC1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply.
	AVSS1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply.

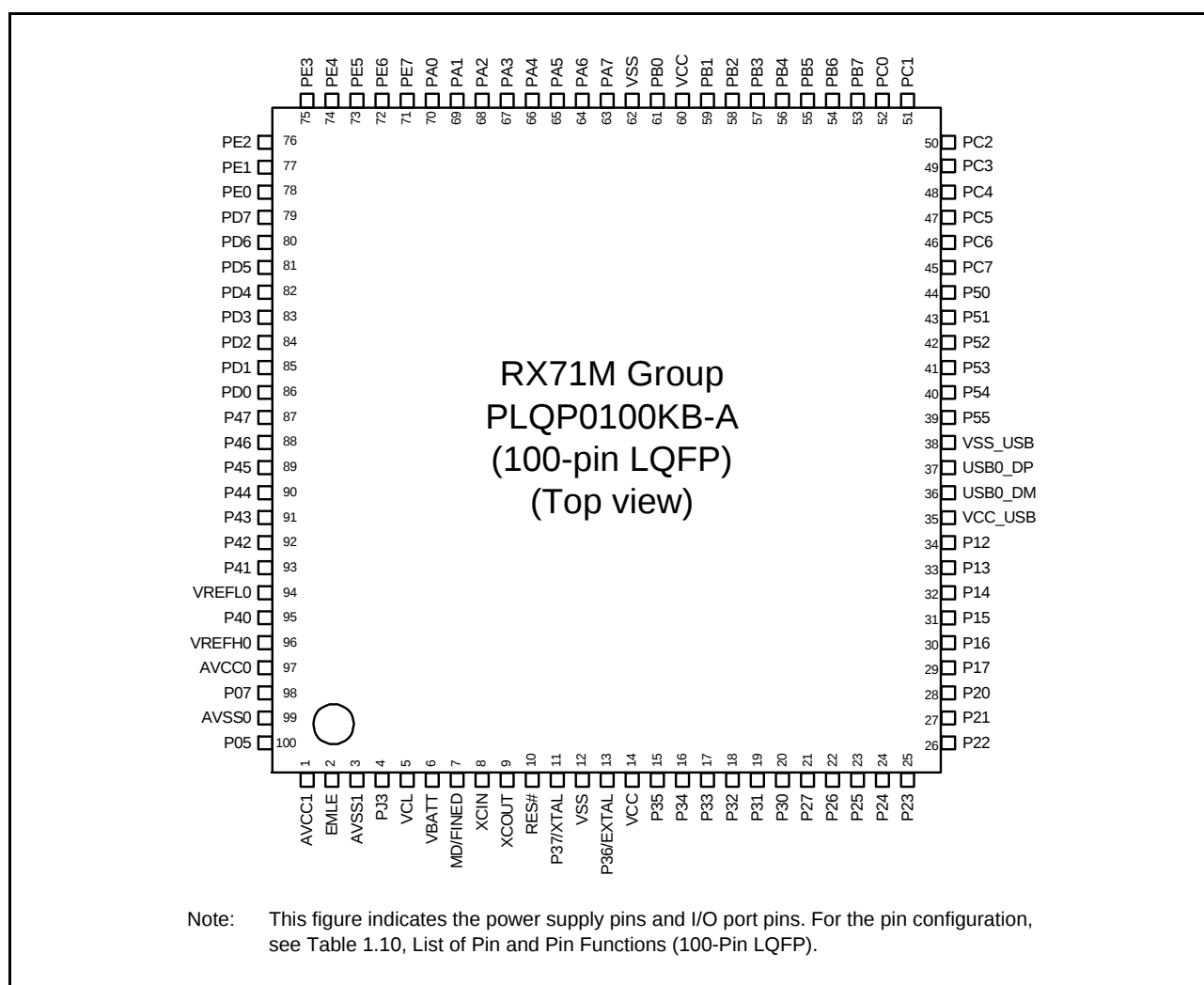


Figure 1.9 Pin Assignment (100-Pin LQFP)

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (1/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
1	AVSS0							
2		P05					IRQ13	DA1
3	AVCC1							
4		P03					IRQ11	DA0
5	AVSS1							
6		P02		TMCI1	SCK6		IRQ10	AN120
7		P01		TMCI0	RXD6/SMISO6/ SSCL6		IRQ9	AN119
8		P00		TMRI0	TXD6/SMOSI6/ SSDA6		IRQ8	AN118
9		PF5					IRQ4	
10	EMLE							
11		PJ5		POE8#	CTS2#/RTS2#/SS2#			
12	VSS							
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#			
14	VCL							
15	VBATT							
16	NC							
17	TRST#	PF4						
18	MD/FINED							
19	XCIN							
20	XCOUT							
21	RES#							
22	XTAL	P37						
23	VSS							
24	EXTAL	P36						
25	VCC							
26	UPSEL	P35					NMI	
27		P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
28		P33	EDREQ1	MTIOC0D/TIOC0D/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
29		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
30	TMS	PF3						
31	TDI	PF2			RXD1/SMISO1/ SSCL1			
32		P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/ SS1#/ET1_MDC/ SSLB0-A		IRQ1-DS	
33		P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/ET1_MDIO/ MISOB-A		IRQ0-DS	
34	TCK	PF1			SCK1			
35	TDO	PF0			TXD1/SMOSI1/SSDA1			

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5)

Pin Number				Timer	Communication	Memory Interface Camera Interface		
145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	(QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
C9		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
C10		P63	CS3#/CAS#					
C11		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
C12		P70	SDCLK					
C13	VSS							
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6		IRQ8	AN118
D2		PF5					IRQ4	
D3		P03					IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6		IRQ9	AN119
D5	VCC							
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
D8		P60	CS0#					
D9		P64	CS4#/WE#					
D10		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D11	VCC							
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
D13		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/ TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
E1	VSS							
E2	VCL							
E3		PJ5		POE8#	CTS2#/RTS2#/SS2#			
E4	EMLE							
E5		P44					IRQ12- DS	AN004
E10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
E11		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
E12		P65	CS5#/CKE					
E13		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
F1	XCIN							
F2	XCOUT							
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/ RTS6#/(CTS0#/RTS0#/ SS6#/SS0#			
F4	VBATT							
F10		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
F11	VSS							
F12		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	

Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
116	VSS							
117		P60	CS0#					
118	VCC							
119		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
120		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO- B	IRQ6	AN106
121		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
122		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
123		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
124		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
125		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
126		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
127		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
128		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
129		P91	A17		SCK7			AN115
130	VSS							
131		P90	A16		TXD7/SMOSI7/SSDA7			AN114
132	VCC							
133		P47					IRQ15- DS	AN007
134		P46					IRQ14- DS	AN006
135		P45					IRQ13- DS	AN005
136		P44					IRQ12- DS	AN004
137		P43					IRQ11-DS	AN003
138		P42					IRQ10- DS	AN002
139		P41					IRQ9-DS	AN001
140	VREFL0							
141		P40					IRQ8-DS	AN000
142	VREFH0							
143	AVCC0							
144		P07					IRQ15	ADTRG0#

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/4)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMC12/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	
H9		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
H10		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
J1		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1			
J2		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0		IRQ9	
J3		P17		MTIOC3A/MTIOC3B/ MTIOC4B/GTIOC0B- B/TIOCB0/TCLKD/ TMO1/PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0		IRQ7	ADTRG1#
J4		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
J5	VSS_USB							
J6	VCC_USB							
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRQ-D/TMC11/ PO25/POE0#	SCK5/CTS8#/SSLA0- A/ET0_TX_CLK			
J9		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
J10		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
K1		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0			
K2		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK			
K3		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0		IRQ8	
K4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
K5					USB0_DM			
K6					USB0_DP			
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2			
K9		PC3	A19	MTIOC4D/GTIOC1B- D/TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
K10		PC2	A18	MTIOC4B/GTIOC2B- D/TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			

Table 4.1 List of I/O Registers (Address Order) (2 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK		Clock Generation Circuit
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK		Clock Generation Circuit
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK		Clock Generation Circuit
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK		Low Power Consumption
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK		Low Power Consumption
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00A3h	SYSTEM	Sub-Clock Oscillator Wait Control Register	SOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK		Resets
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LDVA
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK		LDVA
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK		LDVA
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK		LDVA
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function
0008 1200h	RAM	RAM Operating Mode Control Register	RAMMODE	8	8	2 ICLK		RAM
0008 1201h	RAM	RAM Error Status Register	RAMSTS	8	8	2 ICLK		RAM
0008 1204h	RAM	RAM Protection Register	RAMPSCR	8	8	2 ICLK		RAM
0008 1208h	RAM	RAM Error Address Capture Register	RAMECAD	32	32	2 ICLK		RAM
0008 12C0h	ECCRAM	ECCRAM Operating Mode Control Register	ECCRAMMODE	8	8	2 ICLK		RAM
0008 12C1h	ECCRAM	ECCRAM 2-Bit Error Status Register	ECCRAM2STS	8	8	2 ICLK		RAM
0008 12C2h	ECCRAM	ECCRAM 1-Bit Error Information Update Enable Register	ECCRAM1STSEN	8	8	2 ICLK		RAM
0008 12C3h	ECCRAM	ECCRAM 1-Bit Error Status Register	ECCRAM1STS	8	8	2 ICLK		RAM
0008 12C4h	ECCRAM	ECCRAM Protection Register	ECCRAMPRCR	8	8	2 ICLK		RAM
0008 12C8h	ECCRAM	ECCRAM 2-Bit Error Address Capture Register	ECCRAM2ECAD	32	32	2 ICLK		RAM
0008 12CCh	ECCRAM	ECCRAM 1-Bit Error Address Capture Register	ECCRAM1ECAD	32	32	2 ICLK		RAM
0008 12D0h	ECCRAM	ECCRAM Protection Register 2	ECCRAMPRCR2	8	8	2 ICLK		RAM
0008 12D4h	ECCRAM	ECCRAM Test Control Register	ECCRAMETS	8	8	2 ICLK		RAM
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK		Buses
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK		Buses

Table 4.1 List of I/O Registers (Address Order) (19 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9161h	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9170h	S12AD1	A/D Sampling State Register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9171h	S12AD1	A/D Sampling State Register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9176h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9177h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9178h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9179h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 917Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9184h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9186h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9190h	S12AD1	A/D Compare Control Register	ADCMPCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9192h	S12AD1	A/D Compare Channel Select Extended Register	ADCMPANSE R	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9193h	S12AD1	A/D Compare Level Extended Register	ADCMPLER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9194h	S12AD1	A/D Compare Channel Select Register 0	ADCMPANSR 0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9196h	S12AD1	A/D Compare Channel Select Register 1	ADCMPANSR 1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9198h	S12AD1	A/D Compare Level Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ah	S12AD1	A/D Compare Level Register 1	ADCMPLR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ch	S12AD1	A/D Compare Data Register 0	ADCMPPDR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Eh	S12AD1	A/D Compare Data Register 1	ADCMPPDR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A0h	S12AD1	A/D Compare Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A2h	S12AD1	A/D Compare Status Register 1	ADCMPSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A4h	S12AD1	A/D Compare Status Extended Register	ADCMPSER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9E00h	QSPI	QSPI Control Register	SPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E01h	QSPI	QSPI Slave Select Polarity Register	SSLP	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E02h	QSPI	QSPI Pin Control Register	SPPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E03h	QSPI	QSPI Status Register	SPSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E04h	QSPI	QSPI Data Register	SPDR	32	8, 16, 32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E08h	QSPI	QSPI Sequence Control Register	SPSCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E09h	QSPI	QSPI Sequence Status Register	SPSSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ah	QSPI	QSPI Bit Rate Register	SPBR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Bh	QSPI	QSPI Data Control Register	SPDCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ch	QSPI	QSPI Clock Delay Register	SPCKD	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Dh	QSPI	QSPI Slave Select Negation Delay Register	SSLND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Eh	QSPI	QSPI Next-Access Delay Register	SPND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E10h	QSPI	QSPI Command Register 0	SPCMD0	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E12h	QSPI	QSPI Command Register 1	SPCMD1	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E14h	QSPI	QSPI Command Register 2	SPCMD2	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E16h	QSPI	QSPI Command Register 3	SPCMD3	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E18h	QSPI	QSPI Buffer Control Register	SPBFCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ah	QSPI	QSPI Buffer Data Count Register	SPBDCR	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ch	QSPI	QSPI Transfer Data Length Multiplier Setting Register 0	SPBMUL0	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E20h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 1	SPBMUL1	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI

Table 4.1 List of I/O Registers (Address Order) (42 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
000A 0400h	USB	Deep Standby USB Transceiver Control/Pin Monitoring Register	DPUSR0R	32	32	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*5}$	USBb
000A 0404h	USB	Deep Standby USB Suspend/Resume Interrupt Register	DPUSR1R	32	32	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*5}$	USBb
000A 0500h	PDC	PDC Control Register 0	PCCR0	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0504h	PDC	PDC Control Register 1	PCCR1	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0508h	PDC	PDC Status Register	PCSR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 050Ch	PDC	PDC Pin Monitor Register	PCMONR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0510h	PDC	PDC Receive Data Register	PCDR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0514h	PDC	Vertical Capture Register	VCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0518h	PDC	Horizontal Capture Register	HCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000C 0000h	EDMAC 0	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0008h	EDMAC 0	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0010h	EDMAC 0	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0018h	EDMAC 0	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0020h	EDMAC 0	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0028h	EDMAC 0	ETHERC/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0030h	EDMAC 0	ETHERC/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0038h	EDMAC 0	ETHERC/EDMAC Transmit/Receive Status Copy Enable Register	TRSCER	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0040h	EDMAC 0	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0048h	EDMAC 0	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0050h	EDMAC 0	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0058h	EDMAC 0	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0064h	EDMAC 0	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0068h	EDMAC 0	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 006Ch	EDMAC 0	Independent Output Signal Setting Register	IOSR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0070h	EDMAC 0	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0078h	EDMAC 0	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 007Ch	EDMAC 0	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00C8h	EDMAC 0	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00CCh	EDMAC 0	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00D4h	EDMAC 0	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 00D8h	EDMAC 0	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0100h	ETHERC0	ETHERC Mode Register	ECMR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0108h	ETHERC0	Receive Frame Length Register	RFLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC

Table 4.1 List of I/O Registers (Address Order) (43 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0110h	ETHER C0	ETHERC Status Register	ECSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0118h	ETHER C0	ETHERC Interrupt Enable Register	ECSIPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0120h	ETHER C0	PHY Interface Register	PIR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0128h	ETHER C0	PHY Status Register	PSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0140h	ETHER C0	Random Number Generation Counter Upper Limit Setting Register	RDMLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0150h	ETHER C0	IPG Register	IPGR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0154h	ETHER C0	Automatic PAUSE Frame Register	APR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0158h	ETHER C0	Manual PAUSE Frame Register	MPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0160h	ETHER C0	Received PAUSE Frame Counter	RFCF	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0164h	ETHER C0	PAUSE Frame Retransmit Count Setting Register	TPAUSER	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0168h	ETHER C0	PAUSE Frame Retransmit Counter	TPAUSECR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 016Ch	ETHER C0	Broadcast Frame Receive Count Setting Register	BCFRR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01C0h	ETHER C0	MAC Address Upper Bit Register	MAHR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01C8h	ETHER C0	MAC Address Lower Bit Register	MALR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01D0h	ETHER C0	Transmit Retry Over Counter Register	TROCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01D4h	ETHER C0	Late Collision Detect Counter Register	CDCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01D8h	ETHER C0	Lost Carrier Counter Register	LCCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01DCh	ETHER C0	Carrier Not Detect Counter Register	CNDCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01E4h	ETHER C0	CRC Error Frame Receive Counter Register	CEFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01E8h	ETHER C0	Frame Receive Error Counter Register	FRECR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01ECh	ETHER C0	Too-Short Frame Receive Counter Register	TSFRRCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01F0h	ETHER C0	Too-Long Frame Receive Counter Register	TLFRRCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01F4h	ETHER C0	Received Alignment Error Frame Counter Register	RFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01F8h	ETHER C0	Multicast Address Frame Receive Counter Register	MAFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0200h	EDMAC 1	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0208h	EDMAC 1	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0210h	EDMAC 1	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0218h	EDMAC 1	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0220h	EDMAC 1	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0228h	EDMAC 1	ETHERC/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0230h	EDMAC 1	ETHERC/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa

Table 4.1 List of I/O Registers (Address Order) (44 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0238h	EDMAC 1	ETHERC/EDMAC Transmit/Receive Status Copy Enable Register	TRSCER	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0240h	EDMAC 1	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0248h	EDMAC 1	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0250h	EDMAC 1	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0258h	EDMAC 1	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0264h	EDMAC 1	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0268h	EDMAC 1	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 026Ch	EDMAC 1	Independent Output Signal Setting Register	IOSR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0270h	EDMAC 1	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0278h	EDMAC 1	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 027Ch	EDMAC 1	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 02C8h	EDMAC 1	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 02CCh	EDMAC 1	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 02D4h	EDMAC 1	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 02D8h	EDMAC 1	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0300h	ETHER C1	ETHERC Mode Register	ECMR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0308h	ETHER C1	Receive Frame Length Register	RFLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0310h	ETHER C1	ETHERC Status Register	ECSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0318h	ETHER C1	ETHERC Interrupt Enable Register	ECSIPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0320h	ETHER C1	PHY Interface Register	PIR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0328h	ETHER C1	PHY Status Register	PSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0340h	ETHER C1	Random Number Generation Counter Upper Limit Setting Register	RDMLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0350h	ETHER C1	IPG Register	IPGR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0354h	ETHER C1	Automatic PAUSE Frame Register	APR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0358h	ETHER C1	Manual PAUSE Frame Register	MPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0360h	ETHER C1	Received PAUSE Frame Counter	RFCF	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0364h	ETHER C1	PAUSE Frame Retransmit Count Setting Register	TPAUSER	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0368h	ETHER C1	PAUSE Frame Retransmit Counter Register	TPAUSECR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 036Ch	ETHER C1	Broadcast Frame Receive Count Setting Register	BCFRR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03C0h	ETHER C1	MAC Address Upper Bit Register	MAHR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03C8h	ETHER C1	MAC Address Lower Bit Register	MALR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC

Table 4.1 List of I/O Registers (Address Order) (54 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4328h	EPTPC	Timer Cycle Setting Register 2	TMCYCR2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 432Ch	EPTPC	Timer Pulse Width Setting Register 2	TMPLSR2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4330h	EPTPC	Timer Start Time Setting Register	TMSTTRU3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4334h	EPTPC	Timer Start Time Setting Register	TMSTTRL3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4338h	EPTPC	Timer Cycle Setting Register 3	TMCYCR3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 433Ch	EPTPC	Timer Pulse Width Setting Register 3	TMPLSR3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4340h	EPTPC	Timer Start Time Setting Register	TMSTTRU4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4344h	EPTPC	Timer Start Time Setting Register	TMSTTRL4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4348h	EPTPC	Timer Cycle Setting Register 4	TMCYCR4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 434Ch	EPTPC	Timer Pulse Width Setting Register 4	TMPLSR4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4350h	EPTPC	Timer Start Time Setting Register	TMSTTRU5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4354h	EPTPC	Timer Start Time Setting Register	TMSTTRL5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4358h	EPTPC	Timer Cycle Setting Register 5	TMCYCR5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 435Ch	EPTPC	Timer Pulse Width Setting Register 5	TMPLSR5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 437Ch	EPTPC	Timer Start Register	TMSTARTR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4400h	EPTPC	PRC-TC Status Register	PRSR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4404h	EPTPC	PRC-TC Status Notification Permission Register	PRIPR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4410h	EPTPC	Channel 0 Local MAC Address Register	PRMACRU0	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4414h	EPTPC	Channel 0 Local MAC Address Register	PRMACRL0	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4418h	EPTPC	Channel 1 Local MAC Address Register	PRMACRU1	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 441Ch	EPTPC	Channel 1 Local MAC Address Register	PRMACRL1	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4420h	EPTPC	Packet Transmission Control Register	TRNDISR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4430h	EPTPC	Relay Mode Register	TRNMR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4434h	EPTPC	Cut-Through Transfer Start Threshold Register	TRNCTTDR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPCa
000C 4800h	EPTPC 0	SYNFP Status Register	YSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4804h	EPTPC 0	SYNFP Status Notification Permission Register	SYIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4810h	EPTPC 0	SYNFP MAC Address Register	SYMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4814h	EPTPC 0	SYNFP MAC Address Register	SYMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4818h	EPTPC 0	SYNFP LLC-CTL Value Register	SYLLCCTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 481Ch	EPTPC 0	SYNFP Local IP Address Register	SYIPADDRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4840h	EPTPC 0	SYNFP Specification Version Setting Register	SYSPVRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4844h	EPTPC 0	SYNFP Domain Number Setting Register	SYDOMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4850h	EPTPC 0	Announce Message Flag Field Setting Register	ANFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4854h	EPTPC 0	Sync Message Flag Field Setting Register	SYNFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4858h	EPTPC 0	Delay_Req Message Flag Field Setting Register	DYRQFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 485Ch	EPTPC 0	Delay_Resp Message Flag Field Setting Register	DYRPFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4860h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4864h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4868h	EPTPC 0	SYNFP Local Port Number Register	SYPNUMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4880h	EPTPC 0	SYNFP Register Value Load Directive Register	SYRVLDR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa

Table 4.1 List of I/O Registers (Address Order) (64 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 0470h	USBA	Pipe1 Control Register	PIPE1CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0472h	USBA	Pipe2 Control Register	PIPE2CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0474h	USBA	Pipe3 Control Register	PIPE3CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0476h	USBA	Pipe4 Control Register	PIPE4CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0478h	USBA	Pipe5 Control Register	PIPE5CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 047Ah	USBA	Pipe6 Control Register	PIPE6CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 047Ch	USBA	Pipe7 Control Register	PIPE7CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 047Eh	USBA	Pipe8 Control Register	PIPE8CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0480h	USBA	Pipe9 Control Register	PIPE9CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0490h	USBA	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0492h	USBA	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions			
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 GPT input pin*1 POE3 input pin*1 TPU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG# input pin*1 QSPI input pin*1 RES#, NMI, TCK	V _{IH}	VCC × 0.8	—	VCC + 0.3	V				
		V _{IL}	−0.3	—	VCC × 0.2					
		ΔV _T	VCC × 0.06	—	—					
		RIIC input pin (except for SMBus)	V _{IH}	VCC × 0.7	—			5.8		
			V _{IL}	−0.3	—			VCC × 0.3		
			ΔV _T	VCC × 0.05	—			—		
		Ports for 5 V tolerant*2	V _{IH}	VCC × 0.8	—			5.8		
			V _{IL}	−0.3	—			VCC × 0.2		
		Other input pins excluding ports for 5 V tolerant*3	V _{IH}	VCC × 0.8	—			VCC + 0.3		
	V _{IL}		−0.3	—	VCC × 0.2					
	Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V _{IH}	VCC × 0.9	—			VCC + 0.3	V	
		EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SSI input pin, SDHI input pin, MMC input pin, PDC input pin		VCC × 0.8	—			VCC + 0.3		
		ETHERC input pin		2.3	—			VCC + 0.3		
XCIN*3		VCC × 0.8		—	VCC + 0.3					
D0 to D31		VCC × 0.7		—	VCC + 0.3					
RIIC (SMBus)		2.1		—	VCC + 0.3					
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V _{IL}	−0.3	—	VCC × 0.1	V				
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SSI input pin, SDHI input pin, MMC input pin, PDC input pin		−0.3	—	VCC × 0.2					
	XCIN*3		−0.3	—	VCC × 0.2					
	D0 to D31		−0.3	—	VCC × 0.3					
	RIIC (SMBus)		−0.3	—	0.8					

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.

Note 2. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 3. For P32, P31, P30, and XCIN, input as follows when the V_{BATT} power supply is selected.

V_{IH} Min. = $V_{BATT} \times 0.8$, V_{IH} Max. = $V_{BATT} + 0.3$, V_{IL} Min. = -0.3 , V_{IL} Max. = $V_{BATT} \times 0.2$ ($V_{BATT} = 2.0$ to 3.6 V)

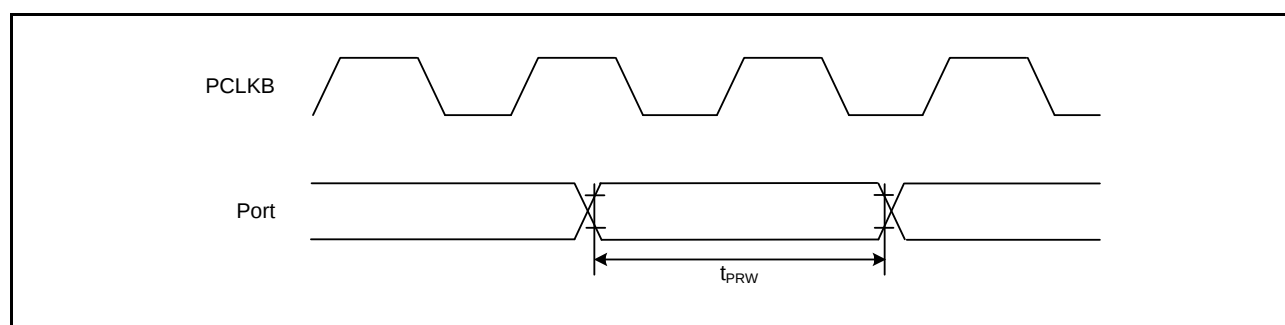
5.3.7 Timing of On-Chip Peripheral Modules

Table 5.23 I/O Port Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 5.33

Note 1. t_{PBcyc} : PCLKB cycle


Figure 5.33 I/O Port Input Timing

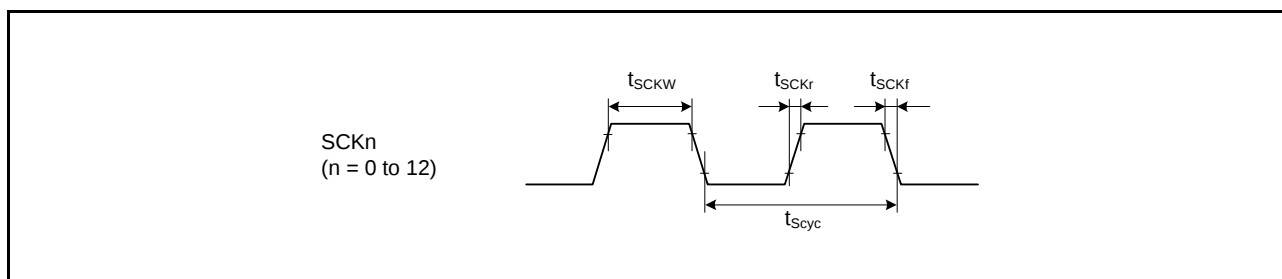


Figure 5.44 SCK Clock Input Timing

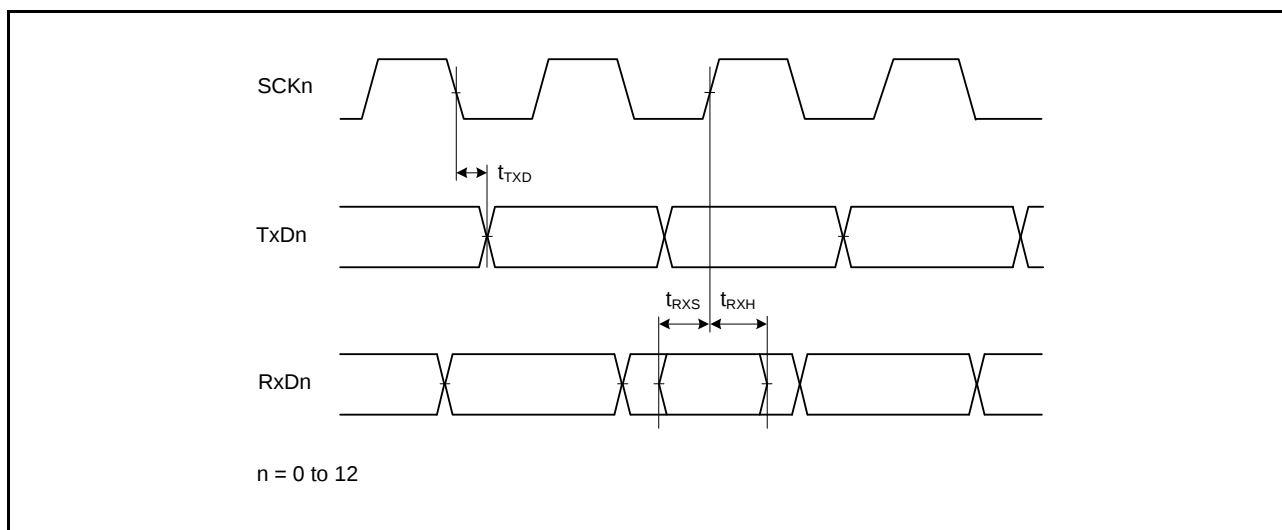


Figure 5.45 SCI Input/Output Timing: Clock Synchronous Mode

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