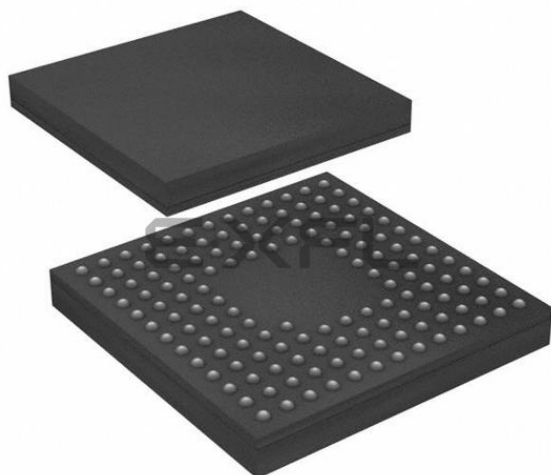




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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mlcdlk-20

Table 1.4 Pin Functions (7/8)

Classifications	Pin Name	I/O	Description
MMC host interface	MMC_CLK-A/ MMC_CLK-B	Output	MMC clock pin
	MMC_CMD-A/ MMC_CMD-B	I/O	Command/response pin
	MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B	I/O	Transmit data/receive data
	MMC_CD-A/MMC_CD-B	Input	Card detection pin
	MMC_RES#-A/MMC_RES#-B	Output	MMC reset output pin
SD host interface	SDHI_CLK-A/SDHI_CLK-B	Output	SD clock output pin
	SDHI_CMD-A/SDHI_CMD-B	I/O	SD command output, response input signal pin
	SDHI_D3-A/SDHI_D3-B to SDHI_D0-A/SDHI_D0-B	I/O	SD data bus pins
	SDHI_CD-A/SDHI_CD-B	Input	SD card detection pin
	SDHI_WP-A/SDHI_WP-B	Input	SD write-protect signal
Parallel data capture unit	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
12-bit A/D converter	AN000 to AN007, AN100 to AN120	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	AVCC1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply.
	AVSS1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply.

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer	Communication	Memory Interface Camera Interface	Interrupt	S12ADC, R12DA
C4		P43					IRQ11-DS	AN003
C5		P45					IRQ13-DS	AN005
C6		P90	A16/D16		ET1_RX_DV/ TXD7/SMOSI7/SSDA7			AN114
C7		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
C8		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2_B	IRQ2	AN110
C9		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
C10		PG0	D24		ET1_RX_CLK/ REF50CK1			
C11	VCC							
C12		P62	CS2#/RAS#					
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
C14	VSS							
C15		P70	SDCLK					
D1		P01		TMC10	RXD6/SMISO6/ SSCL6		IRQ9	AN119
D2		P02		TMC11	SCK6		IRQ10	AN120
D3		P03					IRQ11	DA0
D4		P00		TMR10	TXD6/SMOSI6/ SSDA6		IRQ8	AN118
D5		P44					IRQ12-DS	AN004
D6		P93	A19/D19	POE0#	ET1_LINKSTA/CTS7#/ RTS7#/SS7#			AN117
D7		P95	A21/D21		ET1_ERXD1/ RMII1_RXD1			
D8	VSS							
D9		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
D10		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
D11		P61	CS1#/SDCS#					
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
D13	VCC							
D14		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D15		P65	CS5#/CKE					
E1		PJ5		POE8#	CTS2#/RTS2#/SS2#			
E2	EMLE							
E3		PF5					IRQ4	
E4	VSS							
E5*1								
E12		PE6	D14[A14/D14]	MTIOC6C/ GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (5/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCiG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
M5	VCC_USB							
M6	AVCC_ USBA_							
M7	USBA_ RREF							
M8	VCC_ USBA							
M9		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
M11		P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
M12		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		
M13		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
M15		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
N1	VCC							
N2		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOC3D/ PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ SSISCK0	PIXD7		
N3		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ USBA_OVRCURB/ AUDIO_MCLK	PIXD6		
N4		P15		MTIOC0B/MTCLKB/ GTETRIG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS/ USBA_VBUSEN/ SSIWS1	PIXD0	IRQ5	
N5		P12	WR3#/BC3#	MTIC5U/TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]		IRQ2	
N6	VSS_USB							
N7	VSS2_ USBA							
N8	VSS1_ USBA							
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
N10	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
N11		P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
N12		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
N13		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (3/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
56					USB0_DP			
57	VSS_USB							
58	AVCC_USB _A							
59	USBA_RREF							
60	AVSS_USB _A							
61	PVSS_USB _A							
62	VSS2_USB _A							
63					USBA_DM			
64					USBA_DP			
65	VSS1_USB _A							
66	VCC_USB _A							
67		P11		MTIC5V/TMC13	SCK2/USBA_VBUS/ USBA_VBUS _{EN}		IRQ1	
68		P10	ALE	MTIC5W/TMR13	USBA_OVRCURA		IRQ0	
69		P53*1	BCLK					
70		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
71		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
72		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
73	VSS							
74		P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
75	VCC							
76	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
77		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMC12/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
78		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMR12/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
79		P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
80		P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
81		P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
82		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRQ-D/TMC11/ PO25/POE0#	SCK5/CTS8#//SSLA0- A/ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
83		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		

Table 4.1 List of I/O Registers (Address Order) (14 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 811Ah	TPU0	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Ch	TPU0	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Eh	TPU0	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8120h	TPU1	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8121h	TPU1	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8122h	TPU1	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8124h	TPU1	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8125h	TPU1	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8126h	TPU1	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8128h	TPU1	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 812Ah	TPU1	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8130h	TPU2	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8131h	TPU2	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8132h	TPU2	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8134h	TPU2	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8135h	TPU2	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8136h	TPU2	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8138h	TPU2	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 813Ah	TPU2	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8140h	TPU3	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81E6h	PPG0	PPG Output Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG Output Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E8h	PPG0	Next Data Enable Registers H	NDERH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E9h	PPG0	Next Data Enable Registers L	NDERL	8	8	2, 3 PCLKB	2 ICLK	PPG

Table 4.1 List of I/O Registers (Address Order) (23 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A087h	SCI4	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A088h	SCI4	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A089h	SCI4	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Ah	SCI4	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Bh	SCI4	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Ch	SCI4	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Dh	SCI4	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Eh	SCI4	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Fh	SCI4	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Eh	SCI4	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h
0008 A090h	SCI4	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A091h	SCI4	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A090h	SCI4	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h
0008 A092h	SCI4	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0A9h	SCI5	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0AAh	SCI5	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0ABh	SCI5	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h

Table 4.1 List of I/O Registers (Address Order) (41 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0080h	USB0	Pipe9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 009Ah	USB0	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 009Ch	USB0	Pipe4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 009Eh	USB0	Pipe4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00A0h	USB0	Pipe5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00A2h	USB0	Pipe5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb
000A 00F0h	USB0	PHY Cross Point Adjustment Register	PHYSLEW	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/ PCLKB) ^{*5}	USBb

Table 4.1 List of I/O Registers (Address Order) (43 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0110h	ETHER C0	ETHERC Status Register	ECSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0118h	ETHER C0	ETHERC Interrupt Enable Register	ECSIPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0120h	ETHER C0	PHY Interface Register	PIR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0128h	ETHER C0	PHY Status Register	PSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0140h	ETHER C0	Random Number Generation Counter Upper Limit Setting Register	RDMLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0150h	ETHER C0	IPG Register	IPGR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0154h	ETHER C0	Automatic PAUSE Frame Register	APR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0158h	ETHER C0	Manual PAUSE Frame Register	MPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0160h	ETHER C0	Received PAUSE Frame Counter	RFCF	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0164h	ETHER C0	PAUSE Frame Retransmit Count Setting Register	TPAUSER	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0168h	ETHER C0	PAUSE Frame Retransmit Counter	TPAUSECR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 016Ch	ETHER C0	Broadcast Frame Receive Count Setting Register	BCFRR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01C0h	ETHER C0	MAC Address Upper Bit Register	MAHR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01C8h	ETHER C0	MAC Address Lower Bit Register	MALR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01D0h	ETHER C0	Transmit Retry Over Counter Register	TROCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01D4h	ETHER C0	Late Collision Detect Counter Register	CDCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01D8h	ETHER C0	Lost Carrier Counter Register	LCCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01DCh	ETHER C0	Carrier Not Detect Counter Register	CNDCCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01E4h	ETHER C0	CRC Error Frame Receive Counter Register	CEFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01E8h	ETHER C0	Frame Receive Error Counter Register	FRECR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01ECh	ETHER C0	Too-Short Frame Receive Counter Register	TSFRCCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01F0h	ETHER C0	Too-Long Frame Receive Counter Register	TLFRCCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01F4h	ETHER C0	Received Alignment Error Frame Counter Register	RFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 01F8h	ETHER C0	Multicast Address Frame Receive Counter Register	MAFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0200h	EDMAC 1	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0208h	EDMAC 1	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0210h	EDMAC 1	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0218h	EDMAC 1	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0220h	EDMAC 1	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0228h	EDMAC 1	ETHERC/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0230h	EDMAC 1	ETHERC/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa

Table 4.1 List of I/O Registers (Address Order) (53 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4004h	EPTPC	MINT Interrupt Request Permission Register	MIEIPR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPCa
000C 4010h	EPTPC	ELC Output/IPLS Interrupt Request Permission Register	ELIPPR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPCa
000C 4014h	EPTPC	ELC Output/IPLS Interrupt Permission Automatic Clearing Register	ELIPACR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPCa
000C 4040h	EPTPC	STCA Status Register	STSR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4044h	EPTPC	STCA Status Notification Permission Register	STIPR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4050h	EPTPC	STCA Clock Frequency Setting Register	STCFR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4054h	EPTPC	STCA Operating Mode Register	STMR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4058h	EPTPC	Sync Message Reception Timeout Register	SYNTOR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4060h	EPTPC	IPLS Interrupt Request Timer Select Register	IPTSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4064h	EPTPC	MINT Interrupt Request Timer Select Register	MITSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4068h	EPTPC	ELC Output Timer Select Register	ELTSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 406Ch	EPTPC	Time Synchronization Channel Select Register	STCHSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4080h	EPTPC	Slave Time Synchronization Start Register	SYNSTARTR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4084h	EPTPC	Local Time Counter Initial Value Load Directive Register	LCIVLDR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4090h	EPTPC	Synchronization Loss Detection Threshold Register	SYNTDARU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4094h	EPTPC	Synchronization Loss Detection Threshold Register	SYNTDARL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4098h	EPTPC	Synchronization Detection Threshold Register	SYNTDBRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 409Ch	EPTPC	Synchronization Detection Threshold Register	SYNTDBRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 40B0h	EPTPC	Local Time Counter Initial Value Register	LCIVRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 40B4h	EPTPC	Local Time Counter Initial Value Register	LCIVRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 40B8h	EPTPC	Local Time Counter Initial Value Register	LCIVRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4124h	EPTPC	Worst 10 Acquisition Directive Register	GETW10R	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4128h	EPTPC	Positive Gradient Limit Register	PLIMITRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 412Ch	EPTPC	Positive Gradient Limit Register	PLIMITRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4130h	EPTPC	Positive Gradient Limit Register	PLIMITRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4134h	EPTPC	Negative Gradient Limit Register	MLIMITRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4138h	EPTPC	Negative Gradient Limit Register	MLIMITRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 413Ch	EPTPC	Negative Gradient Limit Register	MLIMITRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4140h	EPTPC	Statistical Information Retention Control Register	GETINFOR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4170h	EPTPC	Local Time Counter	LCCVRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4174h	EPTPC	Local Time Counter	LCCVRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4178h	EPTPC	Local Time Counter	LCCVRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4210h	EPTPC	Positive Gradient Worst 10 Value Register	PW10VRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4214h	EPTPC	Positive Gradient Worst 10 Value Register	PW10VRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4218h	EPTPC	Positive Gradient Worst 10 Value Register	PW10VRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 42D0h	EPTPC	Negative Gradient Worst 10 Value Register	MW10RU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 42D4h	EPTPC	Negative Gradient Worst 10 Value Register	MW10RM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 42D8h	EPTPC	Negative Gradient Worst 10 Value Register	MW10RL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4300h	EPTPC	Timer Start Time Setting Register	TMSTTRU0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4304h	EPTPC	Timer Start Time Setting Register	TMSTTRL0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4308h	EPTPC	Timer Cycle Setting Register 0	TMCYCR0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 430Ch	EPTPC	Timer Pulse Width Setting Register 0	TMPLSR0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4310h	EPTPC	Timer Start Time Setting Register	TMSTTRU1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4314h	EPTPC	Timer Start Time Setting Register	TMSTTRL1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4318h	EPTPC	Timer Cycle Setting Register 1	TMCYCR1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 431Ch	EPTPC	Timer Pulse Width Setting Register 1	TMPLSR1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4320h	EPTPC	Timer Start Time Setting Register	TMSTTRU2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa
000C 4324h	EPTPC	Timer Start Time Setting Register	TMSTTRL2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPCa

Table 4.1 List of I/O Registers (Address Order) (55 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4890h	EPTPC 0	SYNFP Reception Filter Register 1	SYRFL1R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4894h	EPTPC 0	SYNFP Reception Filter Register 2	SYRFL2R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4898h	EPTPC 0	SYNFP Transmission Enable Register	SYTRENr	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A0h	EPTPC 0	Master Clock ID Register	MTCIDU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A4h	EPTPC 0	Master Clock ID Register	MTCIDL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A8h	EPTPC 0	Master Clock Port Number Register	MTPID	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C0h	EPTPC 0	SYNFP Transmission Interval Setting Register	SYTLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C4h	EPTPC 0	SYNFP Received logMessageInterval Value Indication Register	SYRLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C8h	EPTPC 0	offsetFromMaster Value Register	OFMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48CCh	EPTPC 0	offsetFromMaster Value Register	OFMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48D0h	EPTPC 0	meanPathDelay Value Register	MPDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48D4h	EPTPC 0	meanPathDelay Value Register	MPDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E0h	EPTPC 0	grandmasterPriority Field Setting Register	GMPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E4h	EPTPC 0	grandmasterClockQuality Field Setting Register	GMCQR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E8h	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48ECh	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48F0h	EPTPC 0	currentUtcOffset/timeSource Field Setting Register	CUOTSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48F4h	EPTPC 0	stepsRemoved Field Setting Register	SRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4900h	EPTPC 0	PTP-primary Message Destination MAC Address Setting Registers	PPMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4904h	EPTPC 0	PTP-primary Message Destination MAC Address Setting Registers	PPMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4908h	EPTPC 0	PTP-pdelay Message MAC Address Setting Registers	PDMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 490Ch	EPTPC 0	PTP-pdelay Message MAC Address Setting Registers	PDMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4910h	EPTPC 0	PTP Message EtherType Setting Register	PETYPER	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4920h	EPTPC 0	PTP-primary Message Destination IP Address Setting Register	PPIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4924h	EPTPC 0	PTP-pdelay Message Destination IP Address Setting Register	PDIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4928h	EPTPC 0	PTP event Message TOS Setting Register	PETOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 492Ch	EPTPC 0	PTP general Message TOS Setting Register	PGTOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4930h	EPTPC 0	PTP-primary Message TTL Setting Register	PPTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4934h	EPTPC 0	PTP-pdelay Message TTL Setting Register	PDTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4938h	EPTPC 0	PTP event Message UDP Destination Port Number Setting Register	PEUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 493Ch	EPTPC 0	PTP general Message UDP Destination Port Number Setting Register	PGUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa

Table 4.1 List of I/O Registers (Address Order) (61 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 0420h	USBA	CFIFO Port Select Register	CFIFOSEL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0422h	USBA	CFIFO Port Control Register	CFIFOCTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0428h	USBA	D0FIFO Port Select Register	D0FIFOSEL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 042Ah	USBA	D0FIFO Port Control Register	D0FIFOCTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 042Ch	USBA	D1FIFO Port Select Register	D1FIFOSEL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 042Eh	USBA	D1FIFO Port Control Register	D1FIFOCTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0430h	USBA	Interrupt Enable Register 0	INTENB0	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0432h	USBA	Interrupt Enable Register 1	INTENB1	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0436h	USBA	BRDY Interrupt Enable Register	BRDYENB	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 0438h	USBA	NRDY Interrupt Enable Register	NRDYENB	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa
000D 043Ah	USBA	BEMP Interrupt Enable Register	BEMPENB	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB) ^{*5}	USBAa

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Rating

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V

Item	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB	−0.3 to +4.6	V
V _{BATT} power supply voltage	V _{BATT}	−0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1)	V _{in}	−0.3 to VCC + 0.3	V
Input voltage (ports for 5 V tolerant*1)	V _{in}	−0.3 to +5.8	V
Reference power supply voltage	VREFH0	−0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0, AVCC1*2	−0.3 to +4.6	V
USBA power supply voltage	VCC_USBA*2	−0.3 to +4.6	V
USBA analog power supply voltage	AVCC_USBA*2	−0.3 to +4.6	V
Analog input voltage	V _{AN}	−0.3 to AVCC + 0.3	V
Operating temperature	T _{opr}	−40 to +85	°C
Operating temperature (high-temperature products)	T _{opr}	−40 to +105 (Under planning)	°C
Storage temperature	T _{stg}	−55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS.

When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open.

When the USBA is not to be used, connect the VCC_USBA and AVCC_USBA pins to VCC and the VSS1_USBA, VSS2_USBA, PVSS_USBA, and AVSS_USBA pins to VSS, respectively. Do not leave these pins open.

Table 5.9 Operating Frequency (Low-Speed Operating Mode 2)

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

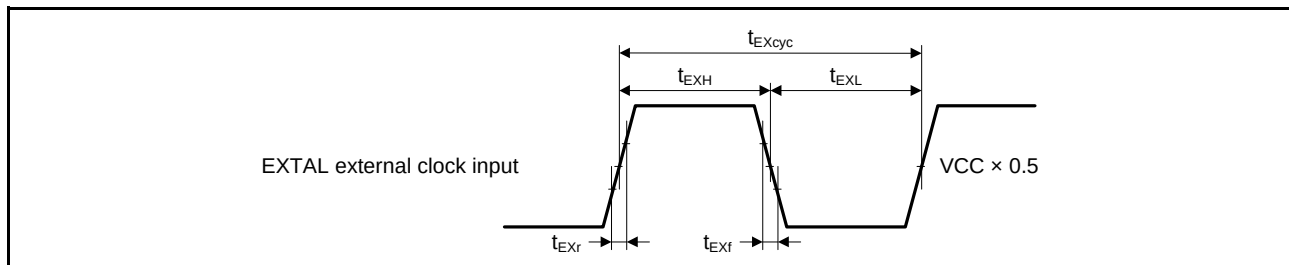
Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	32	—	264	kHz
	Peripheral module clock (PCLKA)			—	—	264	
	Peripheral module clock (PCLKB)			—	—	264	
	Peripheral module clock (PCLKC)* ¹			—	—	264	
	Peripheral module clock (PCLKD)* ¹			—	—	264	
	Flash-IF clock (FCLK)			32	—	264	
	External bus clock (BCLK)	Packages with 177 to 144 pins only		—	—	264	
		Package with 100 pins only		—	—	264	
	BCLK pin output	Packages with 177 to 144 pins only		—	—	264	
		Package with 100 pins only		—	—	264	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	264	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	264	

Note 1. The 12-bit A/D converter cannot be used.

Table 5.12 EXTAL Clock Timing

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 5.4
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

**Figure 5.4 EXTAL External Clock Input Timing****Table 5.13 Main Clock Timing**

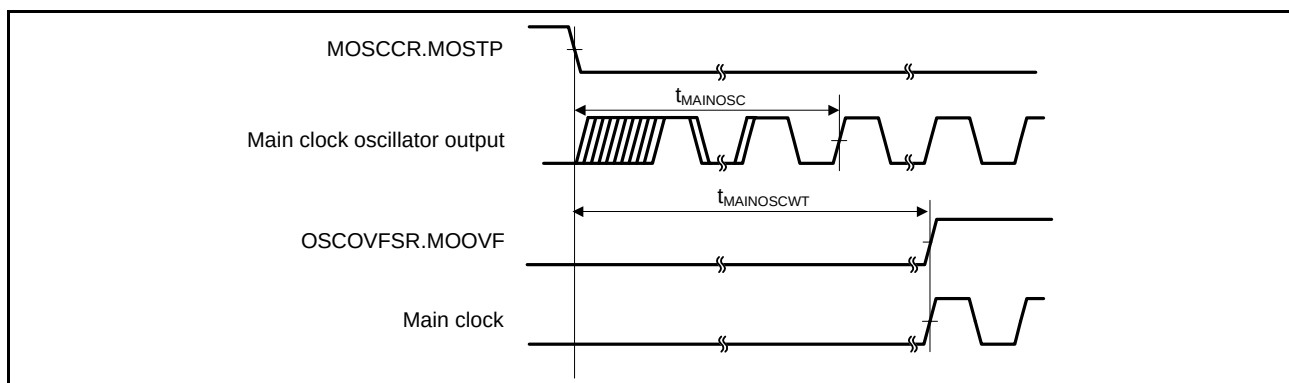
Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 5.5
Main clock oscillator stabilization wait time (crystal)	$t_{MAINSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main-clock oscillation stabilization wait time in accord with the formula below.

$$t_{MAINSCWT} = [(MSTS[7:0] \text{ bits} \times 32) + 10] / f_{LOCO}$$

**Figure 5.5 Main Clock Oscillation Start Timing**

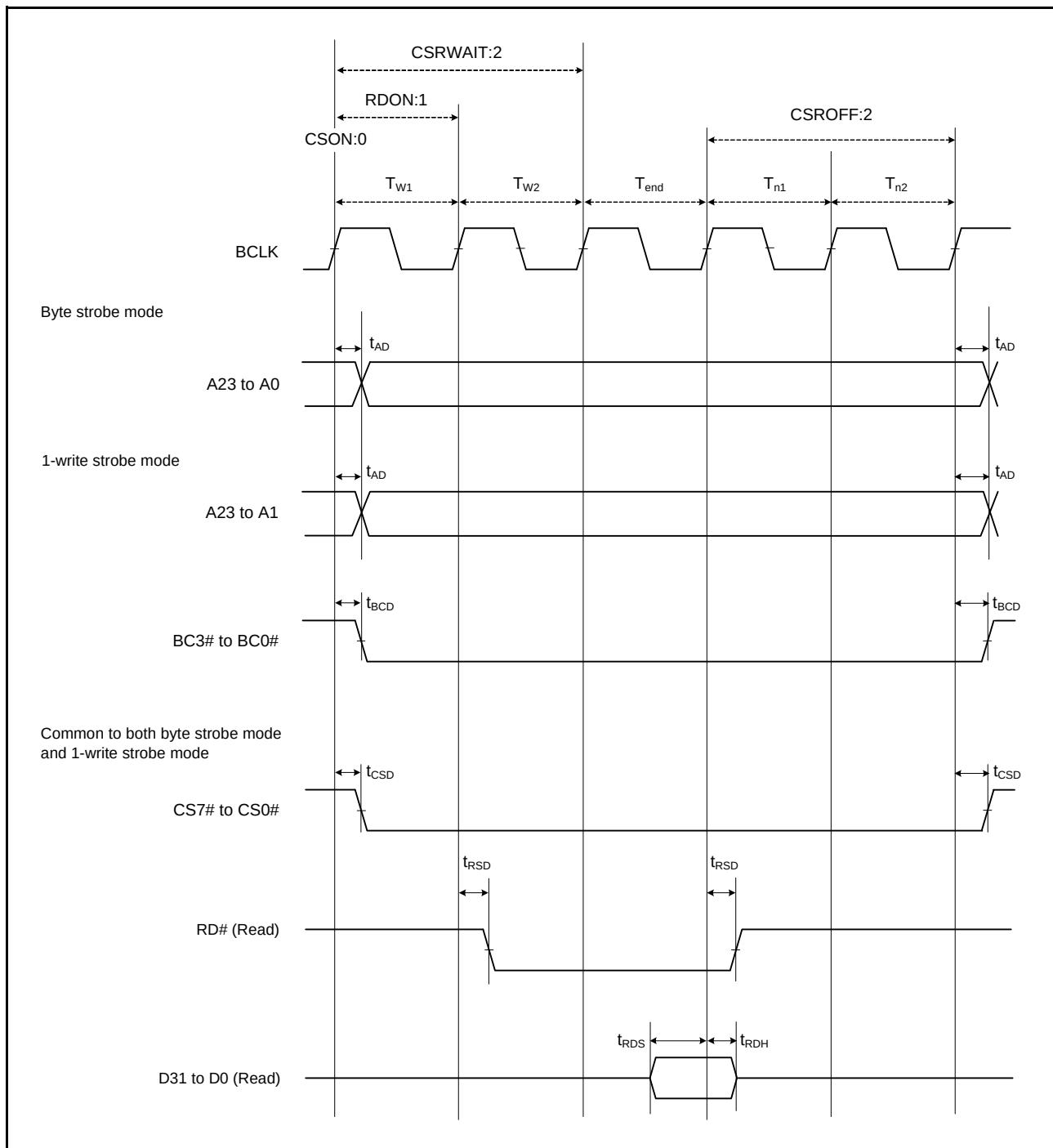


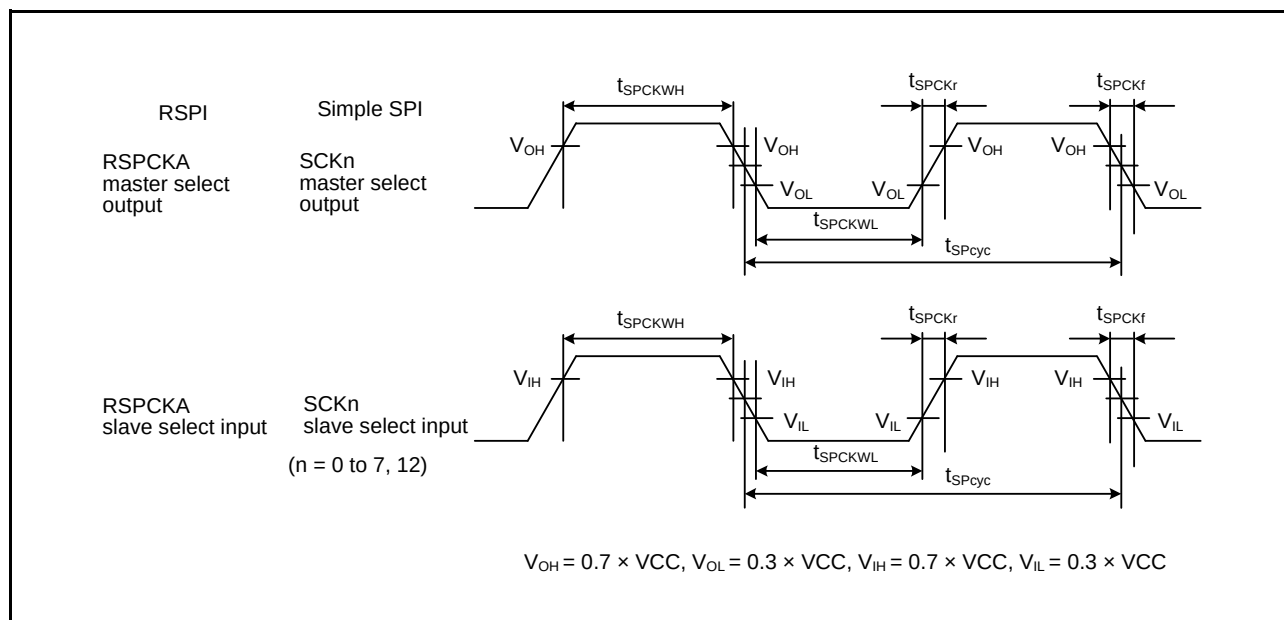
Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

Table 5.34 Simple SPI Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPCyc}	4	65536	t_{PBcyc}	Figure 5.46
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPCyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPCyc}	
	SCK clock rise/fall time	t_{SPCKr} , t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 5.47 to Figure 5.52
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPCyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPCyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	-10	—	ns	
	Data rise/fall time	t_{Dr} , t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr} , t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{PAcyc}	Figure 5.51, Figure 5.52
	Slave output release time	t_{REL}	—	5	t_{PAcyc}	

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.46 RSPI Clock Timing and Simple SPI Clock Timing**

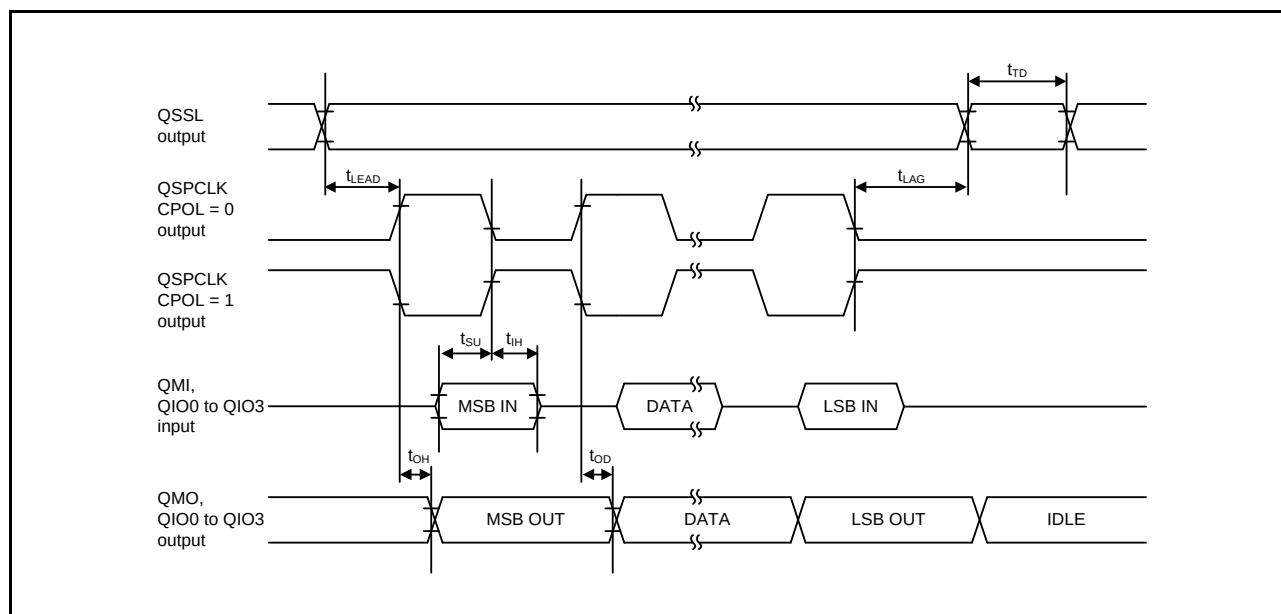


Figure 5.55 Transmit/Receive Timing (CPHA = 1)

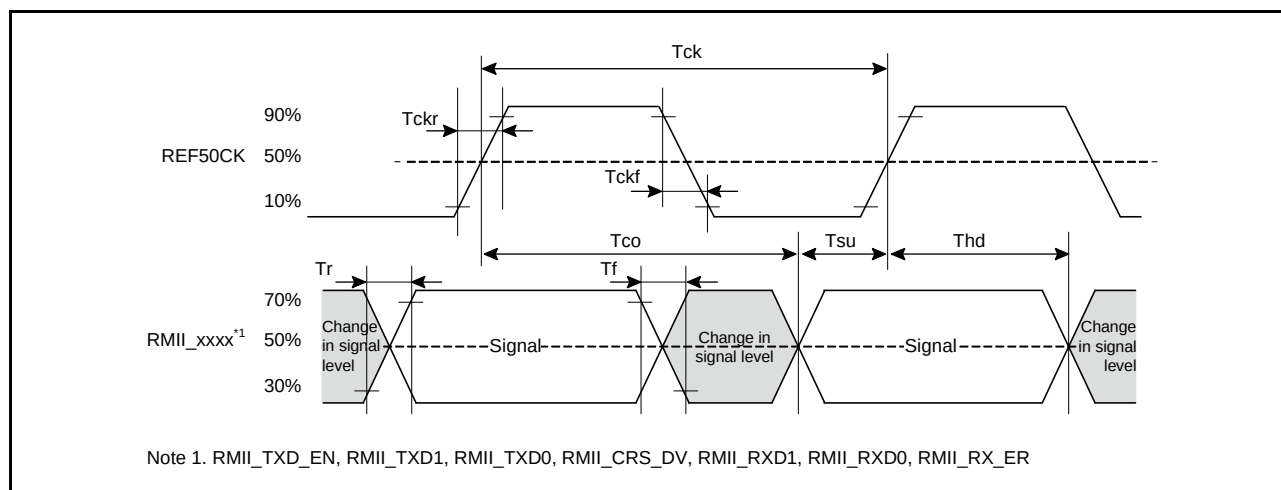


Figure 5.62 Timing with the REF50CK and RMII Signals

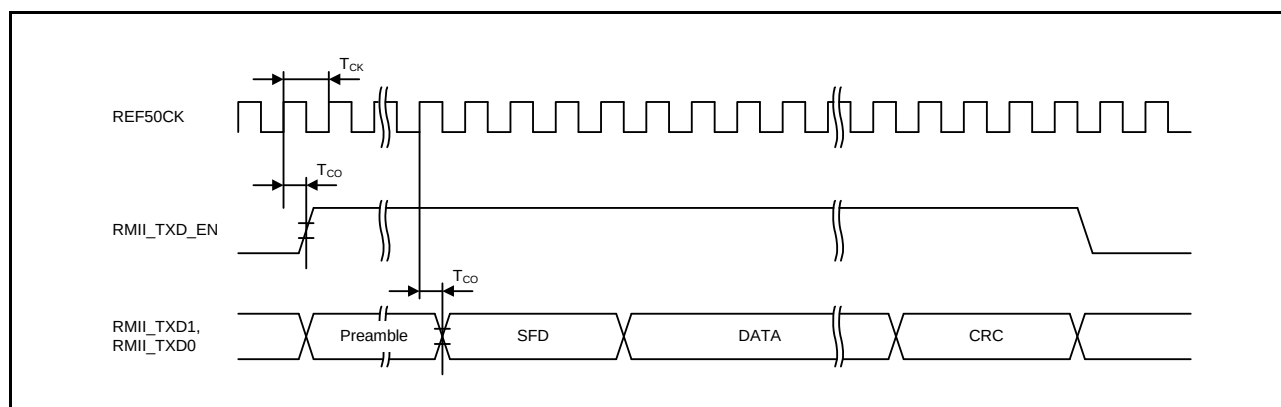


Figure 5.63 RMII Transmission Timing

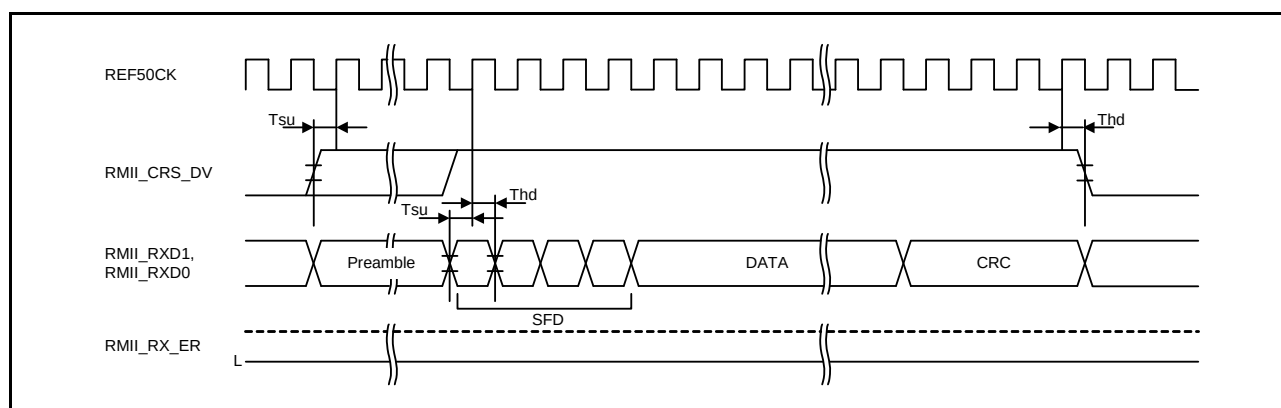


Figure 5.64 RMII Reception Timing (Normal Operation)

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

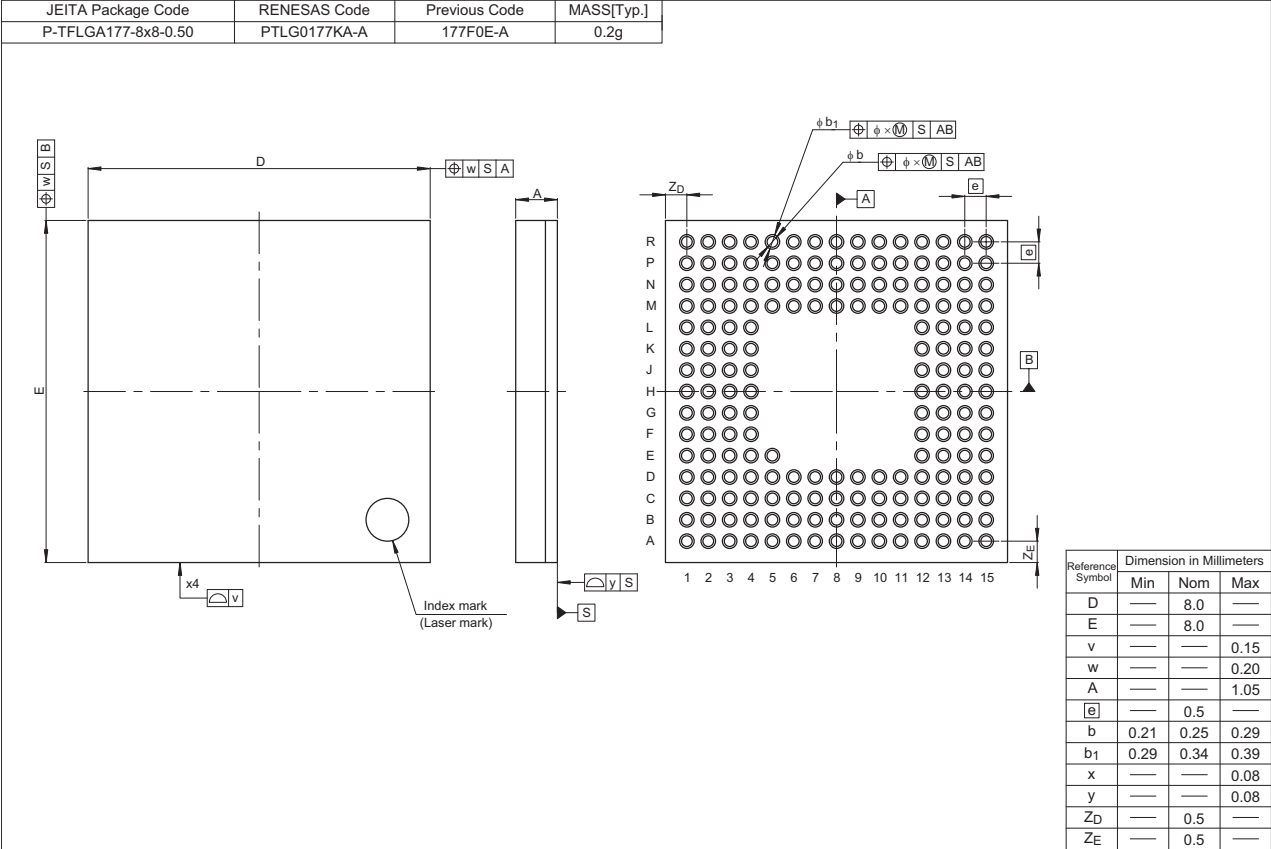


Figure A 177-Pin TFLGA (PTLG0177KA-A)

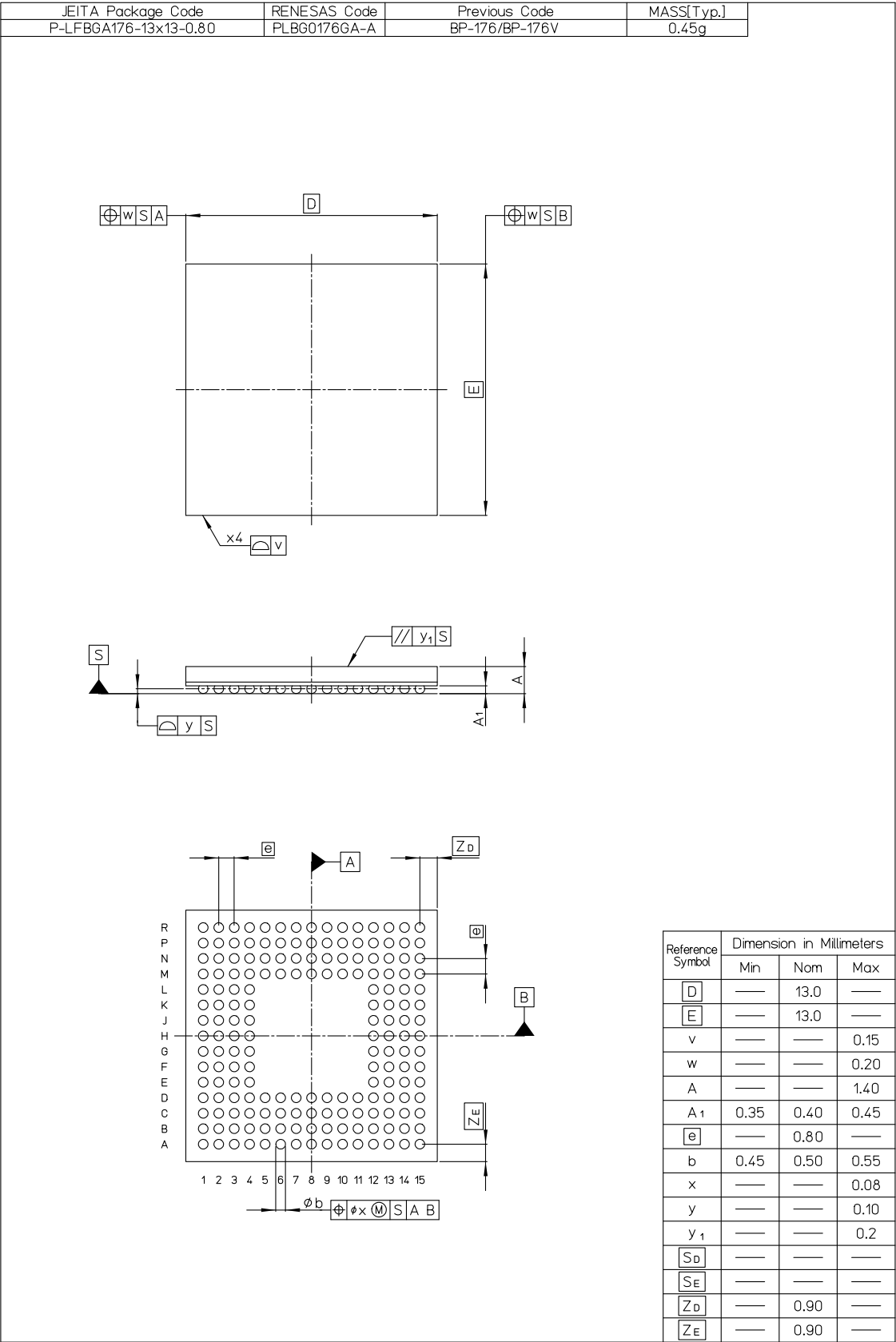


Figure B 176-Pin LFBGA (PLBG0176GA-A)