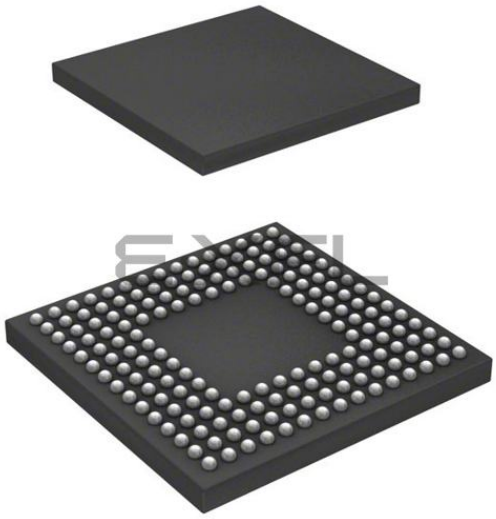

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mlddbg-20

Table 1.1 Outline of Specifications (5/10)

Classification	Module/Function	Description
Timers	General PWM timer (GPTa)	• 16 bits × 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Four clock sources independently selectable for all channels (PCLKA/1, PCLKA/4, PCLKA/8, PCLKA/16) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • Digital filter function for signals on the input capture and external trigger pins • Event linking by the ELC
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units • Pulse output with the MTU or TPU output as a trigger • Maximum of 32 pulse-output possible
	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCd)	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/8)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.22-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	XCOUT	Output	Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
	UB	Input	USB boot mode or user boot mode enable pin
	UPSEL	Input	Selects the power supply method in USB boot mode. The low level selects self-power mode and the high level selects bus power mode.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

Table 4.1 List of I/O Registers (Address Order) (9 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7783h	ICU	Software Configurable Interrupt B Select Register 131	SLIBXR131	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7784h	ICU	Software Configurable Interrupt B Select Register 132	SLIBXR132	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7785h	ICU	Software Configurable Interrupt B Select Register 133	SLIBXR133	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7786h	ICU	Software Configurable Interrupt B Select Register 134	SLIBXR134	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7787h	ICU	Software Configurable Interrupt B Select Register 135	SLIBXR135	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7788h	ICU	Software Configurable Interrupt B Select Register 136	SLIBXR136	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7789h	ICU	Software Configurable Interrupt B Select Register 137	SLIBXR137	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Ah	ICU	Software Configurable Interrupt B Select Register 138	SLIBXR138	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Bh	ICU	Software Configurable Interrupt B Select Register 139	SLIBXR139	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Ch	ICU	Software Configurable Interrupt B Select Register 140	SLIBXR140	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Dh	ICU	Software Configurable Interrupt B Select Register 141	SLIBXR141	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Eh	ICU	Software Configurable Interrupt B Select Register 142	SLIBXR142	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Fh	ICU	Software Configurable Interrupt B Select Register 143	SLIBXR143	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7790h	ICU	Software Configurable Interrupt B Select Register 144	SLIBR144	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7791h	ICU	Software Configurable Interrupt B Select Register 145	SLIBR145	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7792h	ICU	Software Configurable Interrupt B Select Register 146	SLIBR146	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7793h	ICU	Software Configurable Interrupt B Select Register 147	SLIBR147	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7794h	ICU	Software Configurable Interrupt B Select Register 148	SLIBR148	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7795h	ICU	Software Configurable Interrupt B Select Register 149	SLIBR149	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7796h	ICU	Software Configurable Interrupt B Select Register 150	SLIBR150	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7797h	ICU	Software Configurable Interrupt B Select Register 151	SLIBR151	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7798h	ICU	Software Configurable Interrupt B Select Register 152	SLIBR152	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7799h	ICU	Software Configurable Interrupt B Select Register 153	SLIBR153	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Ah	ICU	Software Configurable Interrupt B Select Register 154	SLIBR154	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Bh	ICU	Software Configurable Interrupt B Select Register 155	SLIBR155	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Ch	ICU	Software Configurable Interrupt B Select Register 156	SLIBR156	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Dh	ICU	Software Configurable Interrupt B Select Register 157	SLIBR157	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Eh	ICU	Software Configurable Interrupt B Select Register 158	SLIBR158	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Fh	ICU	Software Configurable Interrupt B Select Register 159	SLIBR159	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77A0h	ICU	Software Configurable Interrupt B Select Register 160	SLIBR160	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77A1h	ICU	Software Configurable Interrupt B Select Register 161	SLIBR161	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77A2h	ICU	Software Configurable Interrupt B Select Register 162	SLIBR162	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77A3h	ICU	Software Configurable Interrupt B Select Register 163	SLIBR163	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77A4h	ICU	Software Configurable Interrupt B Select Register 164	SLIBR164	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 77A5h	ICU	Software Configurable Interrupt B Select Register 165	SLIBR165	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (14 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 811Ah	TPU0	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Ch	TPU0	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Eh	TPU0	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8120h	TPU1	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8121h	TPU1	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8122h	TPU1	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8124h	TPU1	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8125h	TPU1	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8126h	TPU1	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8128h	TPU1	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 812Ah	TPU1	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8130h	TPU2	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8131h	TPU2	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8132h	TPU2	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8134h	TPU2	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8135h	TPU2	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8136h	TPU2	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8138h	TPU2	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 813Ah	TPU2	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8140h	TPU3	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81E6h	PPG0	PPG Output Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG Output Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E8h	PPG0	Next Data Enable Registers H	NDERH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E9h	PPG0	Next Data Enable Registers L	NDERL	8	8	2, 3 PCLKB	2 ICLK	PPG

Table 4.1 List of I/O Registers (Address Order) (19 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9161h	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9170h	S12AD1	A/D Sampling State Register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9171h	S12AD1	A/D Sampling State Register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9176h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9177h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9178h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9179h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 917Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9184h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9186h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9190h	S12AD1	A/D Compare Control Register	ADCMPCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9192h	S12AD1	A/D Compare Channel Select Extended Register	ADCMPANSER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9193h	S12AD1	A/D Compare Level Extended Register	ADCMPLER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9194h	S12AD1	A/D Compare Channel Select Register 0	ADCMPANSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9196h	S12AD1	A/D Compare Channel Select Register 1	ADCMPANSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9198h	S12AD1	A/D Compare Level Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ah	S12AD1	A/D Compare Level Register 1	ADCMPLR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ch	S12AD1	A/D Compare Data Register 0	ADCMPDR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Eh	S12AD1	A/D Compare Data Register 1	ADCMPDR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A0h	S12AD1	A/D Compare Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A2h	S12AD1	A/D Compare Status Register 1	ADCMPSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A4h	S12AD1	A/D Compare Status Extended Register	ADCMPSER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9E00h	QSPI	QSPI Control Register	SPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E01h	QSPI	QSPI Slave Select Polarity Register	SSLP	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E02h	QSPI	QSPI Pin Control Register	SPPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E03h	QSPI	QSPI Status Register	SPSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E04h	QSPI	QSPI Data Register	SPDR	32	8, 16, 32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E08h	QSPI	QSPI Sequence Control Register	SPSCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E09h	QSPI	QSPI Sequence Status Register	SPSSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ah	QSPI	QSPI Bit Rate Register	SPBR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Bh	QSPI	QSPI Data Control Register	SPDCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ch	QSPI	QSPI Clock Delay Register	SPCKD	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Dh	QSPI	QSPI Slave Select Negation Delay Register	SSLND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Eh	QSPI	QSPI Next-Access Delay Register	SPND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E10h	QSPI	QSPI Command Register 0	SPCMD0	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E12h	QSPI	QSPI Command Register 1	SPCMD1	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E14h	QSPI	QSPI Command Register 2	SPCMD2	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E16h	QSPI	QSPI Command Register 3	SPCMD3	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E18h	QSPI	QSPI Buffer Control Register	SPBFCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ah	QSPI	QSPI Buffer Data Count Register	SPBDCR	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ch	QSPI	QSPI Transfer Data Length Multiplier Setting Register 0	SPBMUL0	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E20h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 1	SPBMUL1	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI

Table 4.1 List of I/O Registers (Address Order) (58 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4D6Ch	EPTPC1	Frame Reception Filter MAC Address 1 Setting Registers	FMAC1RL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4DC0h	EPTPC1	Asymmetric Delay Setting Register	DASYMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4DC4h	EPTPC1	Asymmetric Delay Setting Register	DASYMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4DC8h	EPTPC1	Timestamp Latency Setting Register	TSLATR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4DCCh	EPTPC1	SYNFP Operation Setting Register	SYCONFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4DD0h	EPTPC1	SYNFP Frame Format Setting Register	SYFORMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4DD4h	EPTPC1	Response Message Reception Timeout Register	RSTOUTR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000D 0000h	SCIFA8	Serial Mode Register	SMR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0002h	SCIFA8	Bit Rate Register	BRR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0002h	SCIFA8	Modulation Duty Register	MDDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0004h	SCIFA8	Serial Control Register	SCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0006h	SCIFA8	Transmit FIFO Data Register	FTDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0008h	SCIFA8	Serial Status Register	FSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 000Ah	SCIFA8	Receive FIFO Data Register	FRDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 000Ch	SCIFA8	FIFO Control Register	FCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 000Eh	SCIFA8	FIFO Data Count Register	FDR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0010h	SCIFA8	Serial Port Register	SPTR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0012h	SCIFA8	Line Status Register	LSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0014h	SCIFA8	Serial Extended Mode Register	SEMR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0016h	SCIFA8	FIFO Trigger Control Register	FTCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0020h	SCIFA9	Serial Mode Register	SMR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0022h	SCIFA9	Bit Rate Register	BRR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0022h	SCIFA9	Modulation Duty Register	MDDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0024h	SCIFA9	Serial Control Register	SCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0026h	SCIFA9	Transmit FIFO Data Register	FTDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0028h	SCIFA9	Serial Status Register	FSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 002Ah	SCIFA9	Receive FIFO Data Register	FRDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 002Ch	SCIFA9	FIFO Control Register	FCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 002Eh	SCIFA9	FIFO Data Count Register	FDR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0030h	SCIFA9	Serial Port Register	SPTR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0032h	SCIFA9	Line Status Register	LSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0034h	SCIFA9	Serial Extended Mode Register	SEMR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0036h	SCIFA9	FIFO Trigger Control Register	FTCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0040h	SCIFA10	Serial Mode Register	SMR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0042h	SCIFA10	Bit Rate Register	BRR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0042h	SCIFA10	Modulation Duty Register	MDDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0044h	SCIFA10	Serial Control Register	SCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0046h	SCIFA10	Transmit FIFO Data Register	FTDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0048h	SCIFA10	Serial Status Register	FSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 004Ah	SCIFA10	Receive FIFO Data Register	FRDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 004Ch	SCIFA10	FIFO Control Register	FCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 GPT input pin*1 POE3 input pin*1 TPU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG# input pin*1 QSPI input pin*1 RES#, NMI, TCK	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Ports for 5 V tolerant*2	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
	Other input pins excluding ports for 5 V tolerant*3	V_{IH}	VCC × 0.8	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SSI input pin, SDHI input pin, MMC input pin, PDC input pin		VCC × 0.8	—	VCC + 0.3		
	ETHERC input pin		2.3	—	VCC + 0.3		
	XCIN*3		VCC × 0.8	—	VCC + 0.3		
	D0 to D31		VCC × 0.7	—	VCC + 0.3		
	RIIC (SMBus)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1	V	
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SSI input pin, SDHI input pin, MMC input pin, PDC input pin		–0.3	—	VCC × 0.2		
	XCIN*3		–0.3	—	VCC × 0.2		
	D0 to D31		–0.3	—	VCC × 0.3		
	RIIC (SMBus)		–0.3	—	0.8		

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.
Note 3. For P32, P31, P30, and XCIN, input as follows when the V_{BATT} power supply is selected.
VIH Min. = V_{BATT} × 0.8, VIH Max. = V_{BATT} + 0.3, VIL Min. = –0.3, VIL Max. = V_{BATT} × 0.2 (V_{BATT} = 2.0 to 3.6 V)

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Max.*2		I_{CC}*3	—	—	220	mA	ICLK = 240 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 60 MHz FCLK = 60 MHz BCLK = 120 MHz BCLK pin = 60 MHz
		Normal	Peripheral function clock signal supplied*4		—	52	—		
			Peripheral function clock signal stopped*4		—	28	—		
		Coremark	Peripheral function clock signal stopped*4		—	41	—		
		Sleep mode: The clock signal to peripheral modules is supplied*4				37	108		
		All-module-clock-stop mode (reference value)			—	15	80		
		Increased by BGO operation *5	Reading from the code flash memory while the data flash memory is being programmed		—	7	—		
			Reading from the code flash memory while the code flash memory is being programmed		—	10	—		
	Low-speed operating mode 1: Supply of the clock signal to peripheral modules is stopped*4				—	4.4	—		All clocks 1 MHz
	Low-speed operating mode 2: Supply of the clock signal to peripheral modules is stopped*4				—	3	—		All clocks 32.768 kHz
	Software standby mode				—	1.9	59		
	Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USBb only)			—	25	75	μA	
		Power not supplied to standby RAM and USB resume detecting unit (USBb only)	Power-on reset circuit and low-power consumption function disabled*6		—	12.5	26		
			Power-on reset circuit and low-power consumption function enabled*7		—	3.1	13.5		
		Increased by RTC operation	When a crystal oscillator for low clock loads is in use		—	0.6	—		
			When a crystal oscillator for standard clock loads is in use		—	2.0	—		
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use		—	0.9	—		V_{BATT} = 2.0 V, VCC = 0 V
					—	1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		—	1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
					—	3.3	—		V_{BATT} = 3.3 V, VCC = 0 V

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripheral modules is stopped in this state. This does not include operations as BGO (background operations).
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:2.5:5:2.5 when EXTAL = 24 MHz)
I_{CC} Max. = 0.47 × f + 107 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.09 × f + 7 (normal operation in high-speed operating mode)
I_{CC} Typ. = 0.14 × f + 74 (low-speed operating mode 1)
I_{CC} Max. = 0.50 × f + 4 (sleep mode)
Note 4. This does not include operations as BGO (background operations). Whether supply of the clock signal to peripheral modules continues or is stopped only depends on the state determined by the settings of the bits in module stop control registers A to D. The setting for the peripheral module clock stopped state is FCLK = BCLK = PCLKA = PCLKB = PCLKC = PCLKD = BCLK pin = 3.75 MHz (division by 64).
Note 5. This is the increase for programming or erasure of the code flash memory (limitations apply to the combinations of ranges in

Table 5.14 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	3.78	4.16	4.63	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	44	µs	Figure 5.6
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	7.57	8.33	9.26	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108	120	132	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 5.7

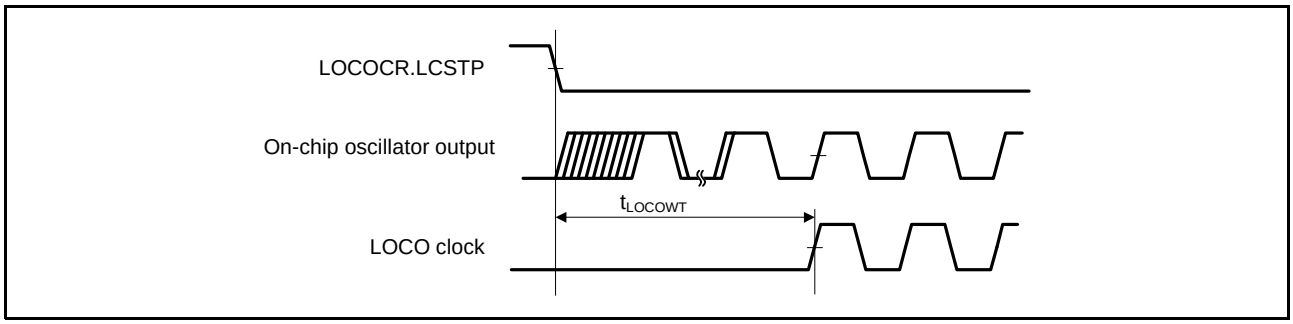


Figure 5.6 LOCO Clock Oscillation Start Timing

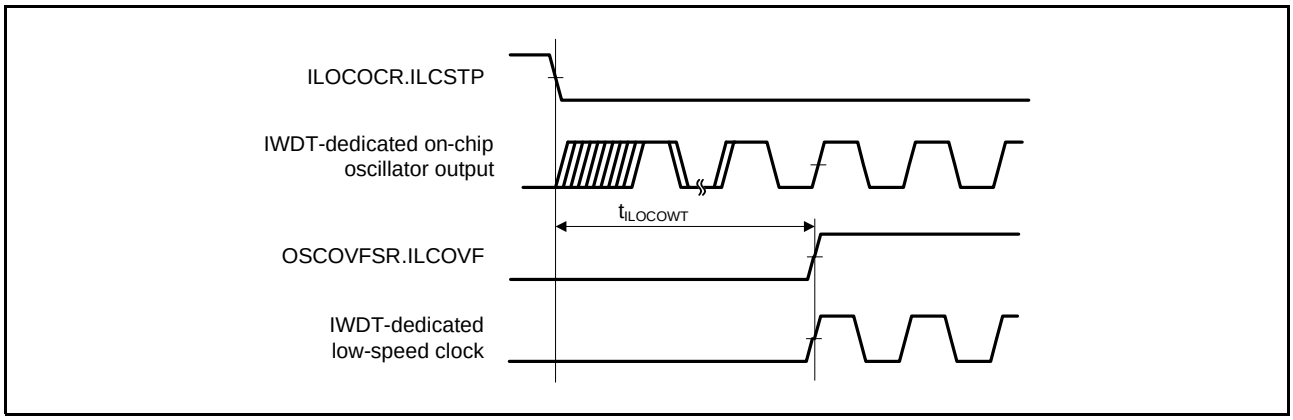


Figure 5.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 5.15 HOCO Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.61	16	16.39	MHz	–20°C ≤ T_a ≤ 85°C
		17.56	18	18.44	MHz	
		19.52	20	20.48	MHz	
		15.52	16	16.48	MHz	–40°C ≤ T_a < –20°C
		17.46	18	18.54	MHz	
		19.40	20	20.60	MHz	
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	µs	Figure 5.8
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150	µs	Figure 5.9

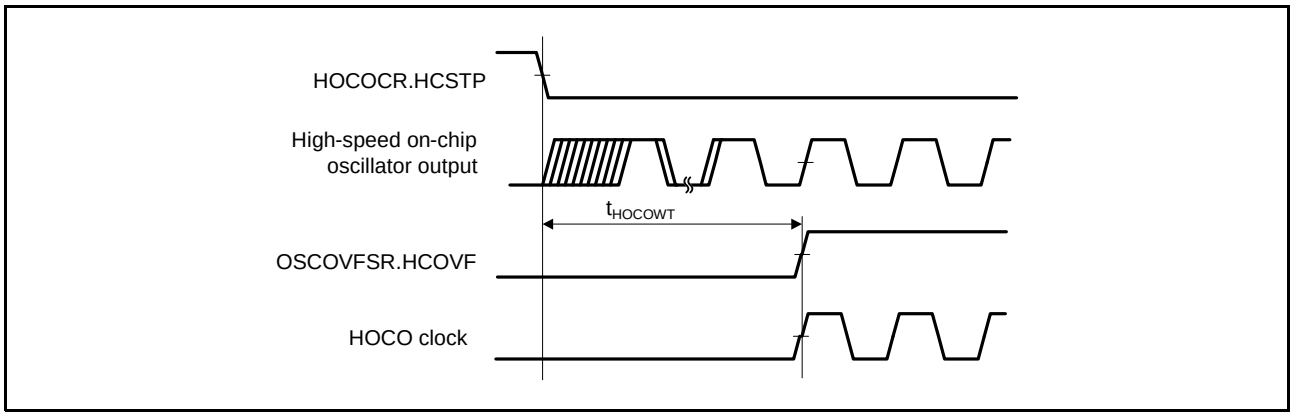


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

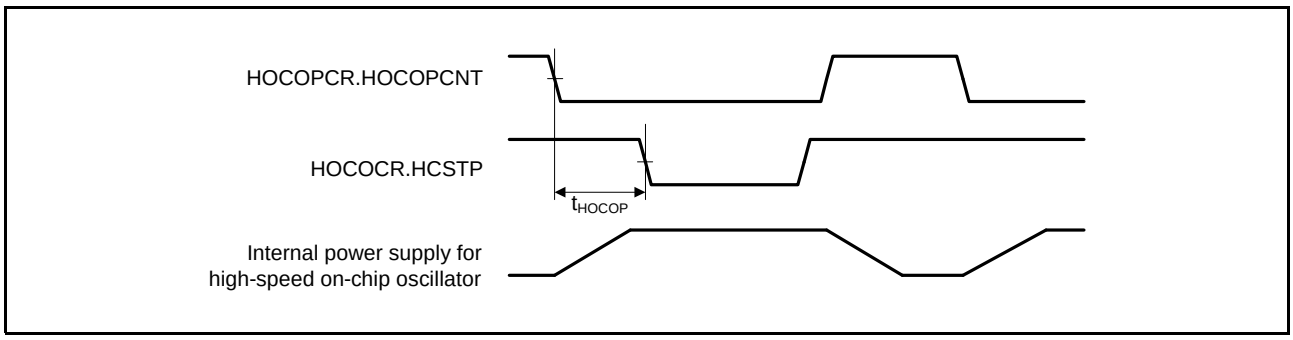


Figure 5.9 High-Speed On-Chip Oscillator Power Supply Control Timing

Table 5.19 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	min	typ	max	Unit	Test Conditions
Recovery time after cancellation of deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 5.13
Wait time after cancellation of deep software standby mode	t_{DSBYWT}	31	—	32	t_{Lcyc}	

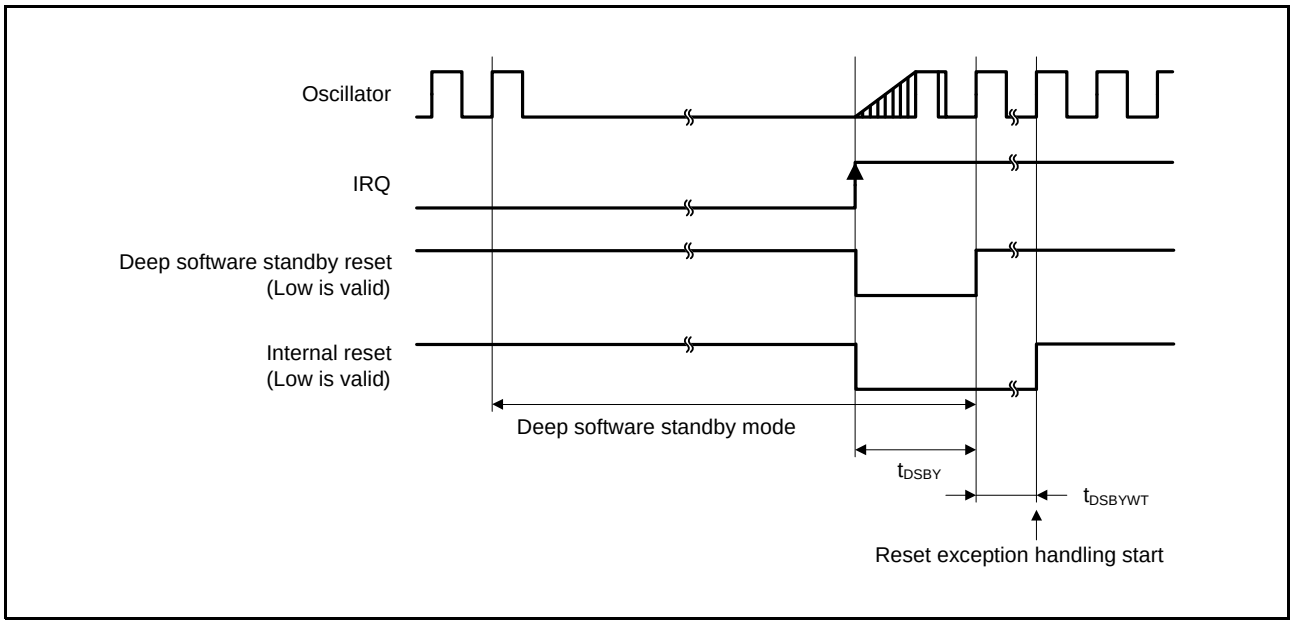


Figure 5.13 Deep Software Standby Mode Cancellation Timing

5.3.5 Bus Timing

Table 5.21 Bus Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
ICLK = 8 to 240 MHz, PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	12.5	ns	Figure 5.16 to Figure 5.21
Byte control delay time	t_{BCD}	—	12.5	ns	
CS# delay time	t_{CSD}	—	12.5	ns	
ALE delay time	t_{ALED}	—	12.5	ns	
RD# delay time	t_{RSD}	—	12.5	ns	
Read data setup time	t_{RDS}	12.5	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	12.5	ns	
Write data delay time	t_{WDD}	—	12.5	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	12.5	—	ns	Figure 5.22
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	12.5	ns	Figure 5.23
CS# delay time 2 (SDRAM)	t_{CSD2}	1	12.5	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	12.5	ns	
CKE delay time (SDRAM)	t_{CKED}	1	12.5	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	10	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	12.5	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	12.5	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	12.5	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	12.5	ns	

Table 5.33 RSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item				Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{PAcyc}	Figure 5.46
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input			—	1	µs	
	Data input setup time	Master		t_{SU}	6	—	ns	Figure 5.47 to Figure 5.52
		Slave			$8.3 - t_{PAcyc}$	—		
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—	ns	
			PCLKA division ratio set to a value other than 1/2	t_H	t_{PAcyc}	—		
		Slave			$8.3 + 2 \times t_{PAcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{PAcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{PAcyc}	
	Data output delay time	Master		t_{OD}	—	6.3	ns	
		Slave			—	$3 \times t_{PAcyc} + 20$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns	
		Slave			$4 \times t_{PAcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	5	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{PAcyc}	Figure 5.51, Figure 5.52
	Slave output release time			t_{REL}	—	3	t_{PAcyc}	

Note 1. t_{PAcyc}: PCLKA cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the RSPI interface, the AC portion of the electrical characteristics is measured for each group.

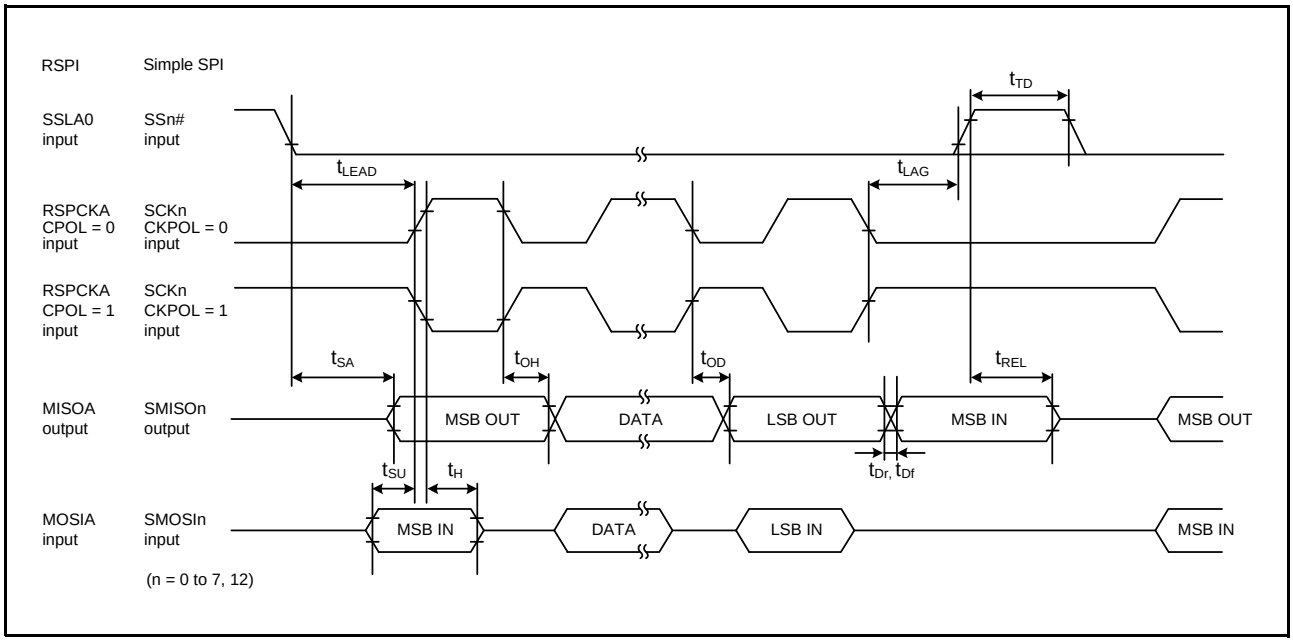


Figure 5.51 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

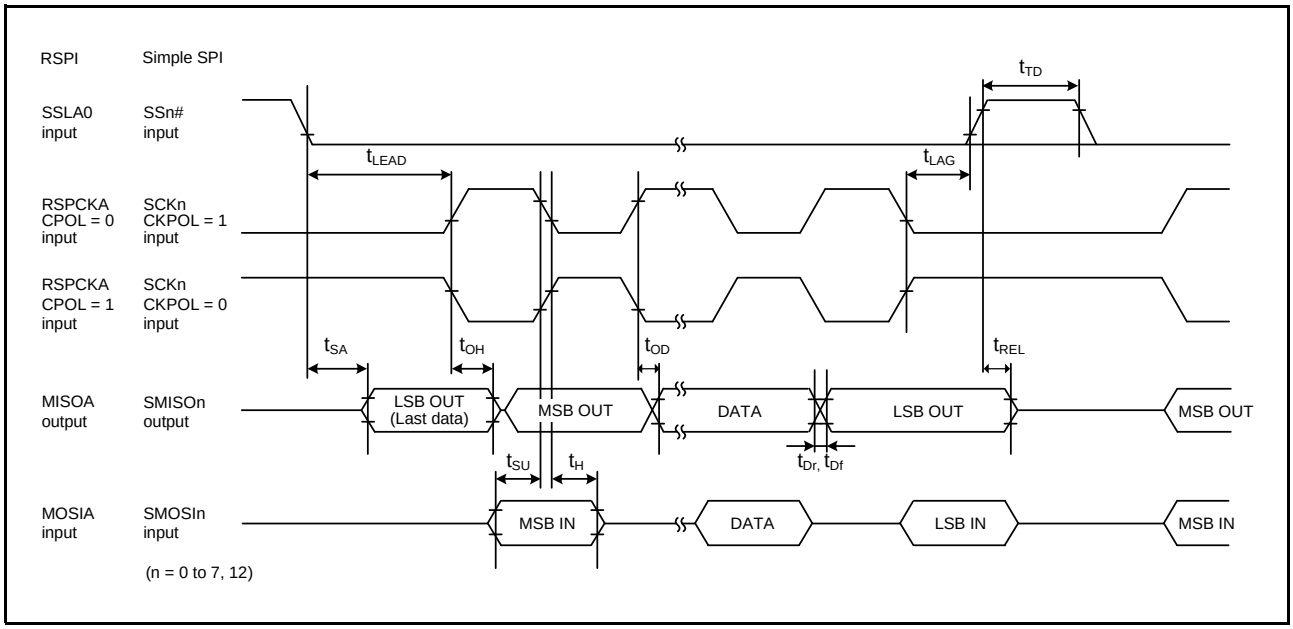


Figure 5.52 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

Table 5.41 PDC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	—	ns	Figure 5.72
	PIXCLK input high pulse width	t_{PIXH}	10	—	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	—	ns	
	PIXCLK rising time	t_{PIXr}	—	5	ns	
	PIXCLK falling time	t_{PIXf}	—	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	—	ns	Figure 5.73
	PCKO output high pulse width	t_{PCKH}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO output low pulse width	t_{PCKL}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO rising time	t_{PCKr}	—	5	ns	
	PCKO falling time	t_{PCKf}	—	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	—	ns	Figure 5.74
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	—	ns	
	PIXD input setup time	t_{PIXDS}	10	—	ns	
	PIXD input hold time	t_{PIXDH}	5	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle

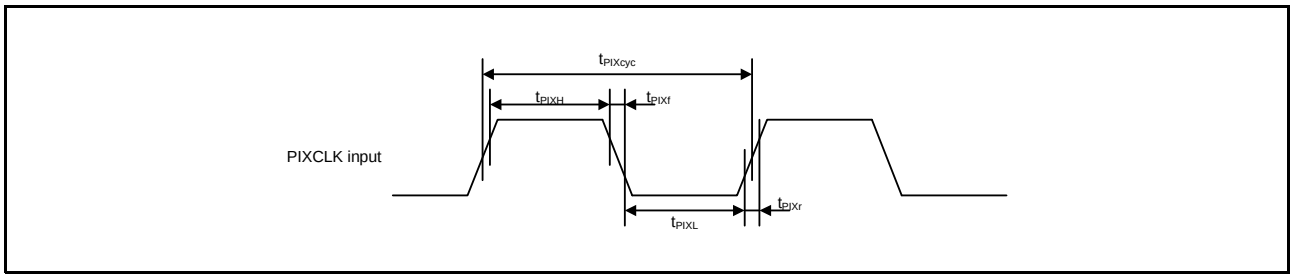


Figure 5.72 PDC Input Clock Timing

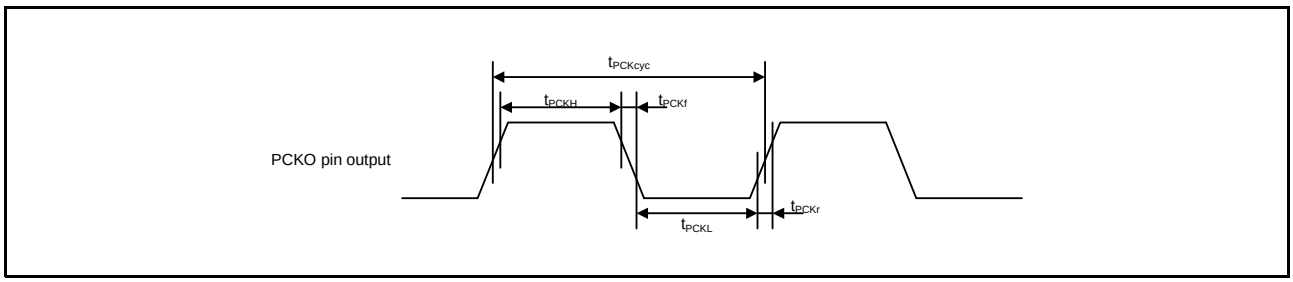


Figure 5.73 PDC Output Clock Timing

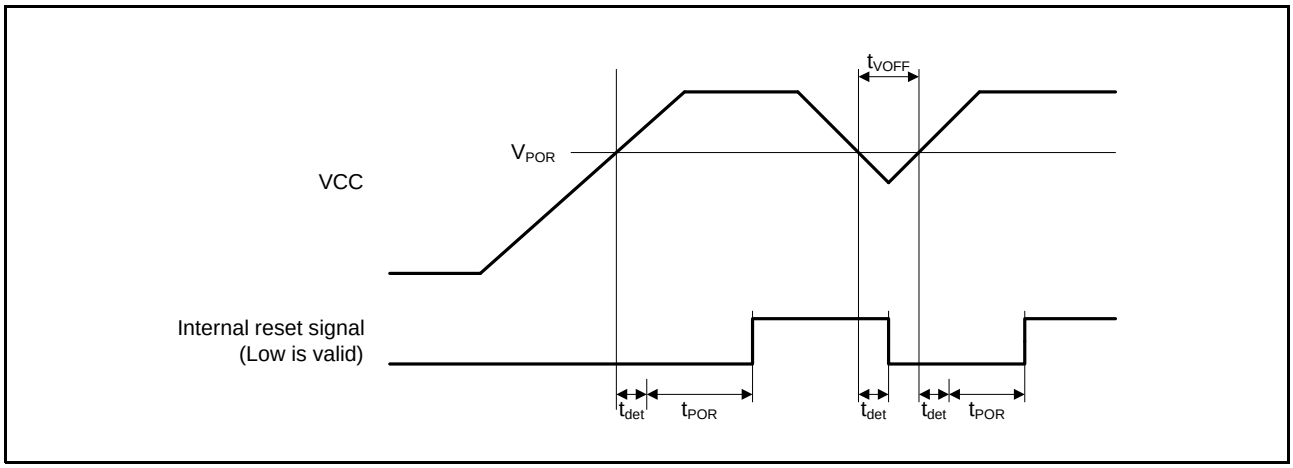


Figure 5.83 Power-on Reset Timing

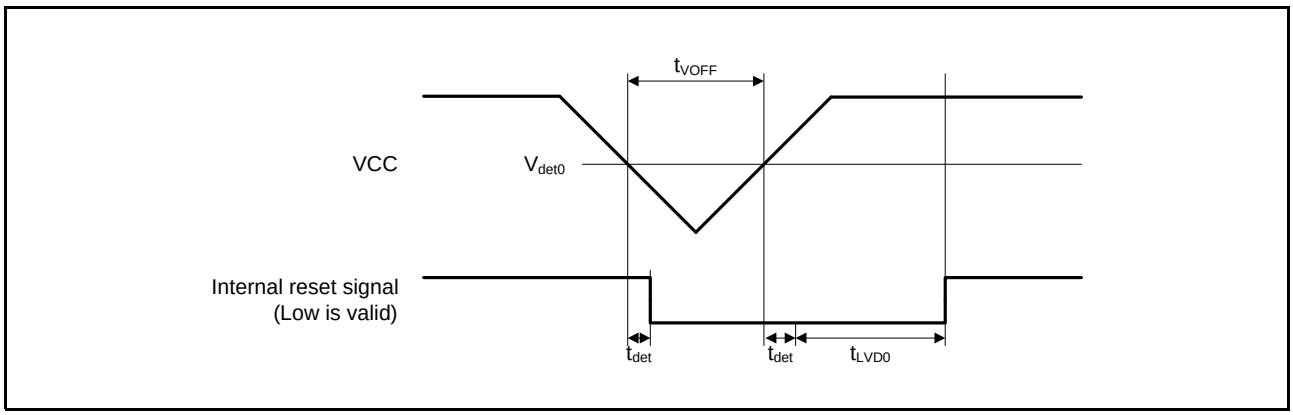


Figure 5.84 Voltage Detection Circuit Timing (V_{det0})

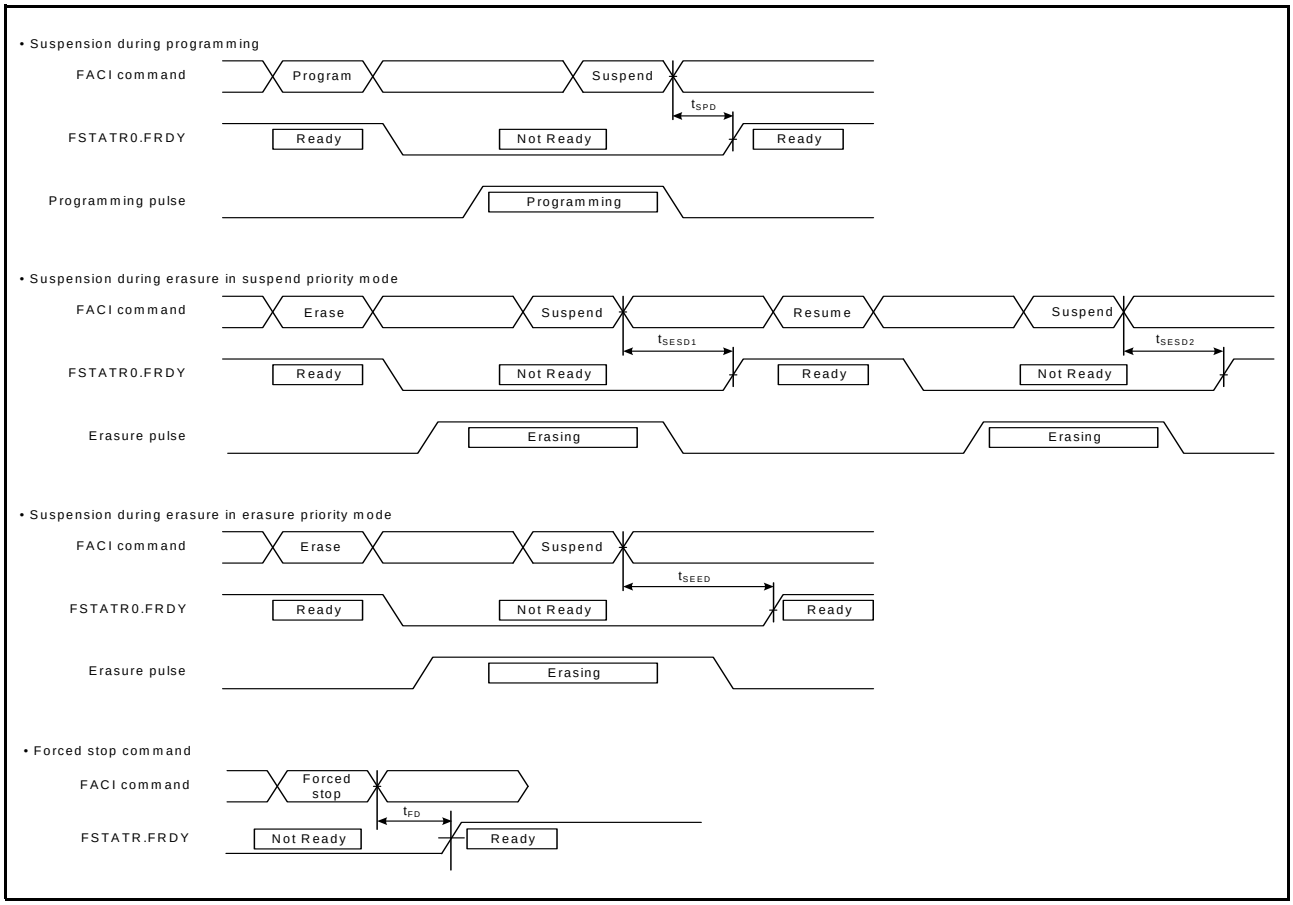


Figure 5.89 Flash Memory Programming/Erasure Suspension Timing

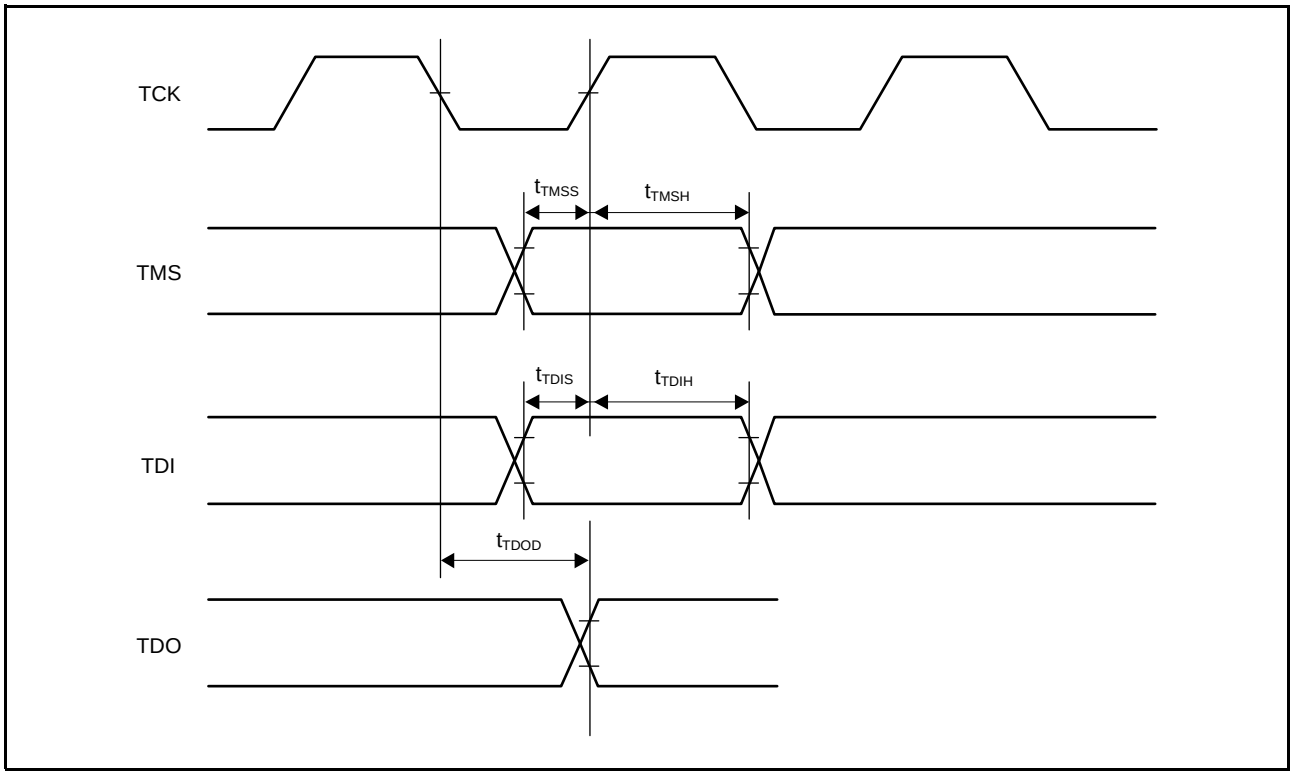
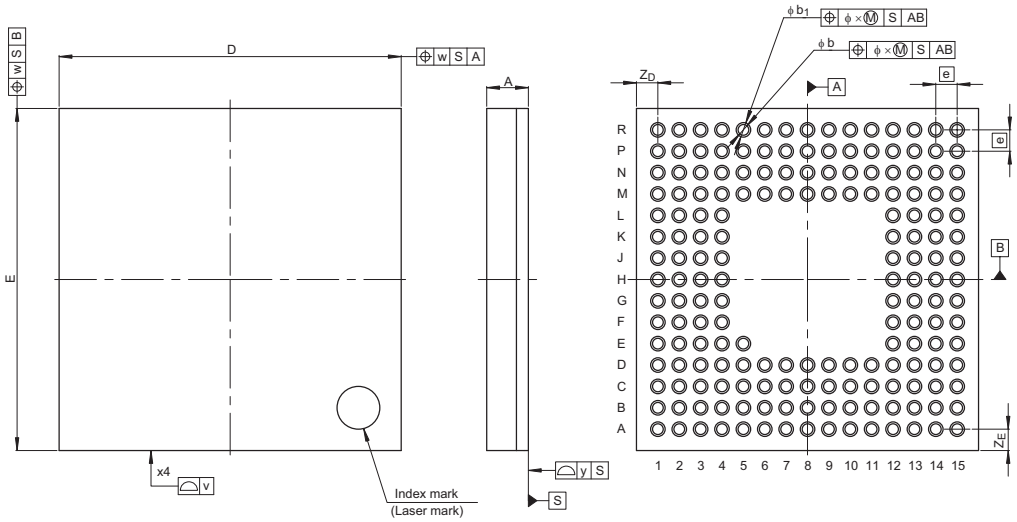


Figure 5.92 Boundary Scan Input/Output Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA177-8x8-0.50	PTLG0177KA-A	177F0E-A	0.2g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	8.0	—
E	—	8.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure A 177-Pin TFLGA (PTLG0177KA-A)

REVISION HISTORY	RX71M Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Jan 15, 2015	—	First edition, issued