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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD, QSPI, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b, 21x12b; D/A 2x12
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f571mlhdbg-20

Table 1.1 Outline of Specifications (9/10)

Classification	Module/Function	Description
Safety	Memory protection unit (MPU)	- Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. - Minimum protection unit: 16 bytes - Reading from, writing to, and enabling the execution access can be specified for each area. - An address exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	- Protects against the reading of programs from blocks 8 and 9 of the code flash memory - Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRC)	- CRC code generation for arbitrary amounts of data in 8-bit units - Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ - Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop function	Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDG-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Encryption function	AESa*3	- Key lengths: 128, 196, and 256 bits - Support for CBC, ECB, CFB, OFB, CTR, and CMAC operating modes - Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles - Compliant with FIPS PUB 197
	DES*3	- Key lengths: 56 bits (DES)/3 × 56 bits (T-DES) - Support for DES and triple DES - Support for ECB and CBC operating modes - Speed of calculations: 6 clock cycles in single DES mode 14 clock cycles in triple DES mode - Compliant with FIPS PUB 46-3 - Compliant with FIPS PUB 81
	SHAa*3	- Support for SHA-1 (128), SHA-2 (224 or 256), and HMAC (160, 224, or 256) - Speed of calculations: 50 clock cycles in SHA-1 mode 42 clock cycles in SHA-224 mode 42 clock cycles in SHA-256 mode - Compliant with SHA as defined in FIPS PUB 180-1 and -2 - Compliant with HMAC as defined in FIPS PUB 198
	True random number generator (RNG)*3	- Length of random numbers: 16 bits - Generation of random-number-generated interrupts after a number is generated - Random number generation time: 3.6 ms (typ)
Operating frequency		Up to 240 MHz
Power supply voltage		$V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = 2.7 \text{ to } 3.6 \text{ V}$, $2.7 \leq V_{REFH0} \leq AVCC0$, $V_{CC_USBA} = AVCC_USBA = 2.7 \text{ to } 3.6 \text{ V}$, $V_{BATT} = 2.0 \text{ to } 3.6 \text{ V}$
Operating temperature		D-version: -40 to +85°C G-version: -40 to +105°C (in planning)
Package		177-pin TFLGA (PTLG0177KA-A) (in planning) 176-pin LFBGA (PLBG0176GA-A) (in planning) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) (in planning) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) (in planning) 100-pin LQFP (PLQP0100KB-A)

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R								
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15							
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14							
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13							
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12							
11	PD6	PG1	VCC	P61	RX71M Group PTLG0177KA-A (177-Pin TFLGA) (Upper Perspective View)							P81	P82	PC6	VCC	11							
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10							
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9							
8	P94	PD1	PD2	VSS								VCC_ USBA	VSS1_ USBA	P10	P11	8							
7	VSS	P92	PD0	P95								USBA_ RREF	VSS2_ USBA	USBA_ DM	USBA_ DP	7							
6	VCC	P91	P90	P93								AVCC_ USBA	VSS_ USB	AVSS_ USBA	PVSS_ USBA	6							
5	P46	P47	P45	P44	NC	RX71M Group PTLG0177KA-A (177-Pin TFLGA) (Upper Perspective View)							VCC_ USB	P12	USB0_ DP	USB0_ DM	5						
4	P42	P41	P43	P00	VSS								BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5								PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE								VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5								VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E								F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	VSS	PE6	P67	PA2	PA4	PA7	PB1	PB5	VSS	VCC	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	VCC	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	VSS	VCC	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64	RX71M Group PTLG0145KA-A (145-Pin TFLGA) (Upper Perspective View)					P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	VSS_ USB	USB0_ DP	6
5	P45	P43	P46	VCC	P44					P54	P13	VCC_ USB	USB0_ DM	5
4	P42	VREFL0	P41	P01	EMLE	VBATT	BSCANP	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD/ FINED	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	AVCC1	AVSS1	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCiG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
C4		P43					IRQ11-DS	AN003
C5		P45					IRQ13-DS	AN005
C6		P90	A16/D16		ET1_RX_DV/ TXD7/SMOSI7/SSDA7			AN114
C7		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
C8		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2_B	IRQ2	AN110
C9		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
C10		PG0	D24		ET1_RX_CLK/ REF50CK1			
C11	VCC							
C12		P62	CS2#/RAS#					
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
C14	VSS							
C15		P70	SDCLK					
D1		P01		TMCIO	RXD6/SMISO6/ SSCL6		IRQ9	AN119
D2		P02		TMC11	SCK6		IRQ10	AN120
D3		P03					IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/ SSDA6		IRQ8	AN118
D5		P44					IRQ12-DS	AN004
D6		P93	A19/D19	POE0#	ET1_LINKSTA/CTS7#/ RTS7#/SS7#			AN117
D7		P95	A21/D21		ET1_ERXD1/ RMII1_RXD1			
D8	VSS							
D9		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
D10		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
D11		P61	CS1#/SDCS#					
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
D13	VCC							
D14		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D15		P65	CS5#/CKE					
E1		PJ5		POE8#	CTS2#/RTS2#/SS2#			
E2	EMLE							
E3		PF5					IRQ4	
E4	VSS							
E5*1								
E12		PE6	D14[A14/D14]	MTIOC6C/ GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCiG, SCiH, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
J14		PA7	A7	TIOCB2/PO23	MISOA-B/ ET0_WOL			
J15		PA6	A6	MTIC5V/MTCLKB/ GTETR-G-C/TIOCA2/ TMC13/PO22/POE10#	CTS5#/(RTS5#/(SS5#/ MOSIA-B/ ET0_EXOUT			
K1		P33	EDREQ1	MTIOC0D/TIOC0D/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOU/RTICIC2/ POE0#/(POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/ SSCL1			
K4	TCK	PF1			SCK1			
K12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/(RTS4#/(CTS6#/ RTS6#/(SS4#/(SS6#/ ET0_RX_CLK/ REF50CK0			
K13		P71	A18/CS1#		ET0_MDIO			
K14	VCC							
K15		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
L1		P31		MTIOC4D/TMC12/ PO9/RTIC1	CTS1#/(RTS1#/ SS1#/(ET1_MDC/ SSLB0-A		IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/ PO8/RTIC0/POE8#	RXD1/SMISO1/ SSCL1/ET1_MDIO/ MISOB-A		IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/ SSDA1			
L4		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ SSIDATA1	HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
L15		P72	A19/CS2#		ET0_MDC			
M1		P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/ET1_WOL/ RSPCKB-A			
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/ RTS3#/(SMOSI1/ SS3#/(SSDA1/ ET1_EXOUT/ MOSIB-A			
M3		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
M4		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (7/7)

Pin Number				Timer	Communication	Memory Interface Camera Interface		
176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	(QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
171		P41					IRQ9-DS	AN001
172	VREFL0							
173		P40					IRQ8-DS	AN000
174	VREFH0							
175	AVCC0							
176		P07					IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (4/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
87		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
88		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
89		PA6	A6	MTIC5V/MTCLKB/ GTETRIG-C/TIOCA2/ TMC13/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
90		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
91	VCC							
92		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
93	VSS							
94		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
95		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
96		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
97		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
98		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
99		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
100		P65	CS5#/CKE					
101		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
102		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/ TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
103	VCC							
104		P70	SDCLK					
105	VSS							
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
108		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3/ SS12#/ET0_ERXD3/	MMC_D7-B		AN101
109		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXD12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
110		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
111		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
112		P64	CS4#/WE#					
113		P63	CS3#/CAS#					
114		P62	CS2#/RAS#					
115		P61	CS1#/SDCS#					

Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
116	VSS							
117		P60	CS0#					
118	VCC							
119		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
120		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO- B	IRQ6	AN106
121		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
122		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
123		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
124		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
125		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
126		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
127		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
128		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
129		P91	A17		SCK7			AN115
130	VSS							
131		P90	A16		TXD7/SMOSI7/SSDA7			AN114
132	VCC							
133		P47					IRQ15- DS	AN007
134		P46					IRQ14- DS	AN006
135		P45					IRQ13- DS	AN005
136		P44					IRQ12- DS	AN004
137		P43					IRQ11-DS	AN003
138		P42					IRQ10- DS	AN002
139		P41					IRQ9-DS	AN001
140	VREFL0							
141		P40					IRQ8-DS	AN000
142	VREFH0							
143	AVCC0							
144		P07					IRQ15	ADTRG0#

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (2/4)

Pin Number	Power Supply Clock System Contro	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SClg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
30		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
31		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMC12/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1		IRQ5	
32		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMR12/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
33		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
34		P12		TMC11	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
35	VCC_USB							
36					USB0_DM			
37					USB0_DP			
38	VSS_USB							
39		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
40		P54	ALE/EDACK0	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
41		P53	BCLK					
42		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
43		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
44		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
45	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL		IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMC12/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMR12/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2			
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMC11/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK			
49		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
50		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			
51		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
54		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP).

The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

This CPU has the following ten control registers.

(1) Interrupt stack pointer (ISP) / User stack pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

(2) Exception table register (EXTB)

The exception table register (EXTB) specifies the address where the exception vector table starts.

(3) Interrupt table register (INTB)

The interrupt table register (INTB) specifies the address where the interrupt vector table starts.

(4) Program counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(5) Processor status word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(6) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(7) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(8) Fast interrupt vector register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to section Table 4.1, List of I/O Registers (Address Order).

The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
 Number of divided clock synchronization cycles +
 Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

(5) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

Table 4.1 List of I/O Registers (Address Order) (45 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 03D0h	ETHER C1	Transmit Retry Over Counter Register	TROCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03D4h	ETHER C1	Late Collision Detect Counter Register	CDCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03D8h	ETHER C1	Lost Carrier Counter Register	LCCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03DCh	ETHER C1	Carrier Not Detect Counter Register	CNDCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03E4h	ETHER C1	CRC Error Frame Receive Counter Register	CEFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03E8h	ETHER C1	Frame Receive Error Counter Register	FRECR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03ECh	ETHER C1	Too-Short Frame Receive Counter Register	TSFRCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03F0h	ETHER C1	Too-Long Frame Receive Counter Register	TLFRCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03F4h	ETHER C1	Received Alignment Error Frame Counter Register	RFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03F8h	ETHER C1	Multicast Address Frame Receive Counter Register	MAFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0400h	PTPED MAC	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0408h	PTPED MAC	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0410h	PTPED MAC	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0418h	PTPED MAC	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0420h	PTPED MAC	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0428h	PTPED MAC	PTP/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0430h	PTPED MAC	PTP/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0440h	PTPED MAC	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0448h	PTPED MAC	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0450h	PTPED MAC	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0458h	PTPED MAC	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0464h	PTPED MAC	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0468h	PTPED MAC	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0470h	PTPED MAC	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0478h	PTPED MAC	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 047Ch	PTPED MAC	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04C8h	PTPED MAC	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04CCh	PTPED MAC	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04D4h	PTPED MAC	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04D8h	PTPED MAC	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0500h	EPTPC	PTP Reset Register	PTRSTR	32	32	3, 4 PCLKA	2, 3 ICLK	EPTPCa
000C 0504h	EPTPC	STCA Clock Select Register	STCSELR	32	32	3, 4 PCLKA	2, 3 ICLK	EPTPCa
000C 1200h	MTU3	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (55 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4890h	EPTPC 0	SYNFP Reception Filter Register 1	SYRFL1R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4894h	EPTPC 0	SYNFP Reception Filter Register 2	SYRFL2R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4898h	EPTPC 0	SYNFP Transmission Enable Register	SYTRENr	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A0h	EPTPC 0	Master Clock ID Register	MTCIDU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A4h	EPTPC 0	Master Clock ID Register	MTCIDL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48A8h	EPTPC 0	Master Clock Port Number Register	MTPID	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C0h	EPTPC 0	SYNFP Transmission Interval Setting Register	SYTLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C4h	EPTPC 0	SYNFP Received logMessageInterval Value Indication Register	SYRLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48C8h	EPTPC 0	offsetFromMaster Value Register	OFMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48CCh	EPTPC 0	offsetFromMaster Value Register	OFMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48D0h	EPTPC 0	meanPathDelay Value Register	MPDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48D4h	EPTPC 0	meanPathDelay Value Register	MPDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E0h	EPTPC 0	grandmasterPriority Field Setting Register	GMPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E4h	EPTPC 0	grandmasterClockQuality Field Setting Register	GMCQR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48E8h	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48ECh	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48F0h	EPTPC 0	currentUtcOffset/timeSource Field Setting Register	CUOTSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 48F4h	EPTPC 0	stepsRemoved Field Setting Register	SRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4900h	EPTPC 0	PTP-primary Message Destination MAC Address Setting Registers	PPMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4904h	EPTPC 0	PTP-primary Message Destination MAC Address Setting Registers	PPMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4908h	EPTPC 0	PTP-pdelay Message MAC Address Setting Registers	PDMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 490Ch	EPTPC 0	PTP-pdelay Message MAC Address Setting Registers	PDMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4910h	EPTPC 0	PTP Message EtherType Setting Register	PETYPER	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4920h	EPTPC 0	PTP-primary Message Destination IP Address Setting Register	PPIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4924h	EPTPC 0	PTP-pdelay Message Destination IP Address Setting Register	PDIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4928h	EPTPC 0	PTP event Message TOS Setting Register	PETOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 492Ch	EPTPC 0	PTP general Message TOS Setting Register	PGTOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4930h	EPTPC 0	PTP-primary Message TTL Setting Register	PPTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4934h	EPTPC 0	PTP-pdelay Message TTL Setting Register	PDTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 4938h	EPTPC 0	PTP event Message UDP Destination Port Number Setting Register	PEUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa
000C 493Ch	EPTPC 0	PTP general Message UDP Destination Port Number Setting Register	PGUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPCa

5.3 AC Characteristics

Table 5.7 Operating Frequency (High-Speed Operating Mode)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	240	MHz
	Peripheral module clock (PCLKA)			—	—	120	
	Peripheral module clock (PCLKB)			—	—	60	
	Peripheral module clock (PCLKC)			—	—	60	
	Peripheral module clock (PCLKD)			—	—	60	
	Flash-IF clock (FCLK)			—*1	—	60	
	External bus clock (BCLK)	Packages with 177 to 144 pins only		—	—	120	
		Package with 100 pins only		—	—	60	
	BCLK pin output	Packages with 177 to 144 pins only		—	—	60	
		Package with 100 pins only		—	—	30	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	60	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	60	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

Table 5.8 Operating Frequency (Low-Speed Operating Mode 1)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	1	MHz
	Peripheral module clock (PCLKA)			—	—	1	
	Peripheral module clock (PCLKB)			—	—	1	
	Peripheral module clock (PCLKC)*1			—	—	1	
	Peripheral module clock (PCLKD)*1			—	—	1	
	Flash-IF clock (FCLK)			—	—	1	
	External bus clock (BCLK)	Packages with 177 to 144 pins only		—	—	1	
		Package with 100 pins only		—	—	1	
	BCLK pin output	Packages with 177 to 144 pins only		—	—	1	
		Package with 100 pins only		—	—	1	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	1	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	1	

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

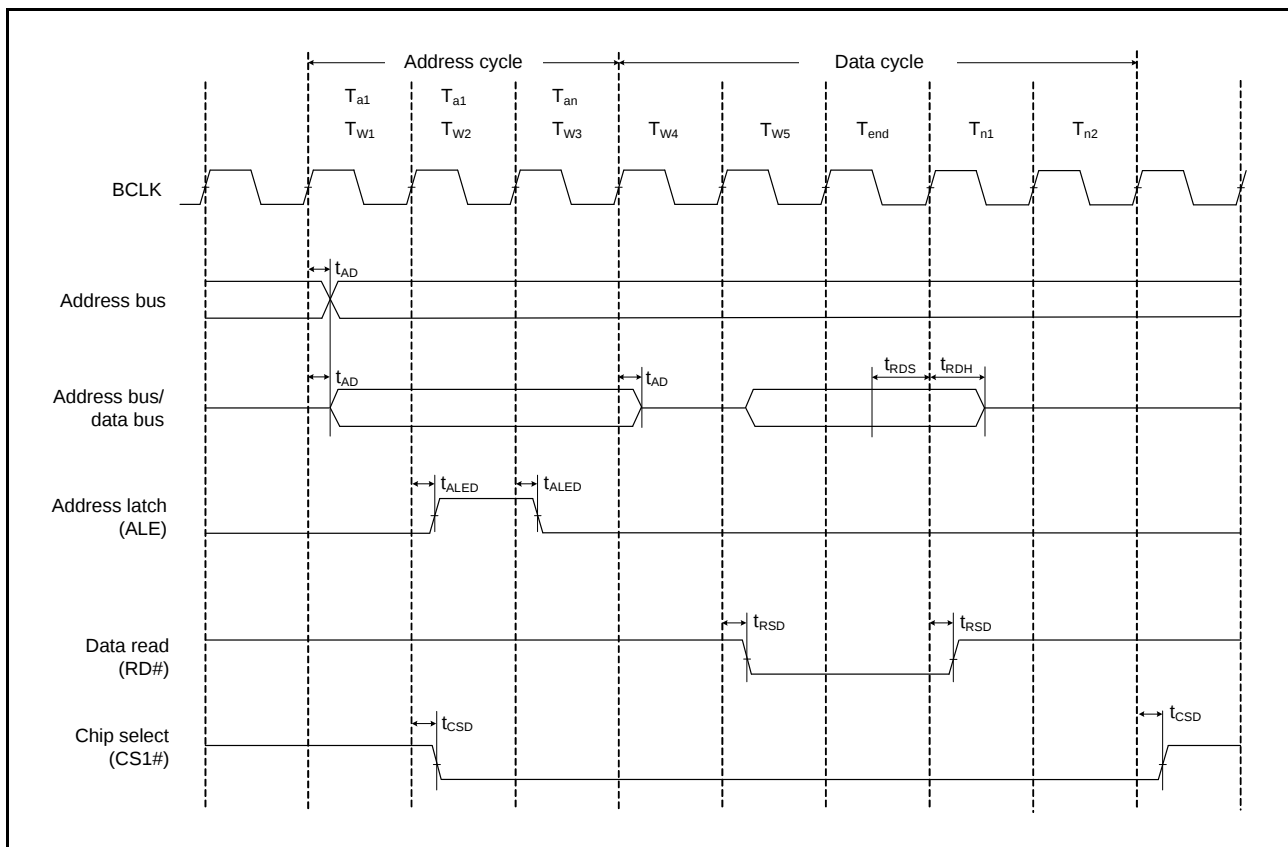


Figure 5.16 Address/Data Multiplexed Bus Read Access Timing

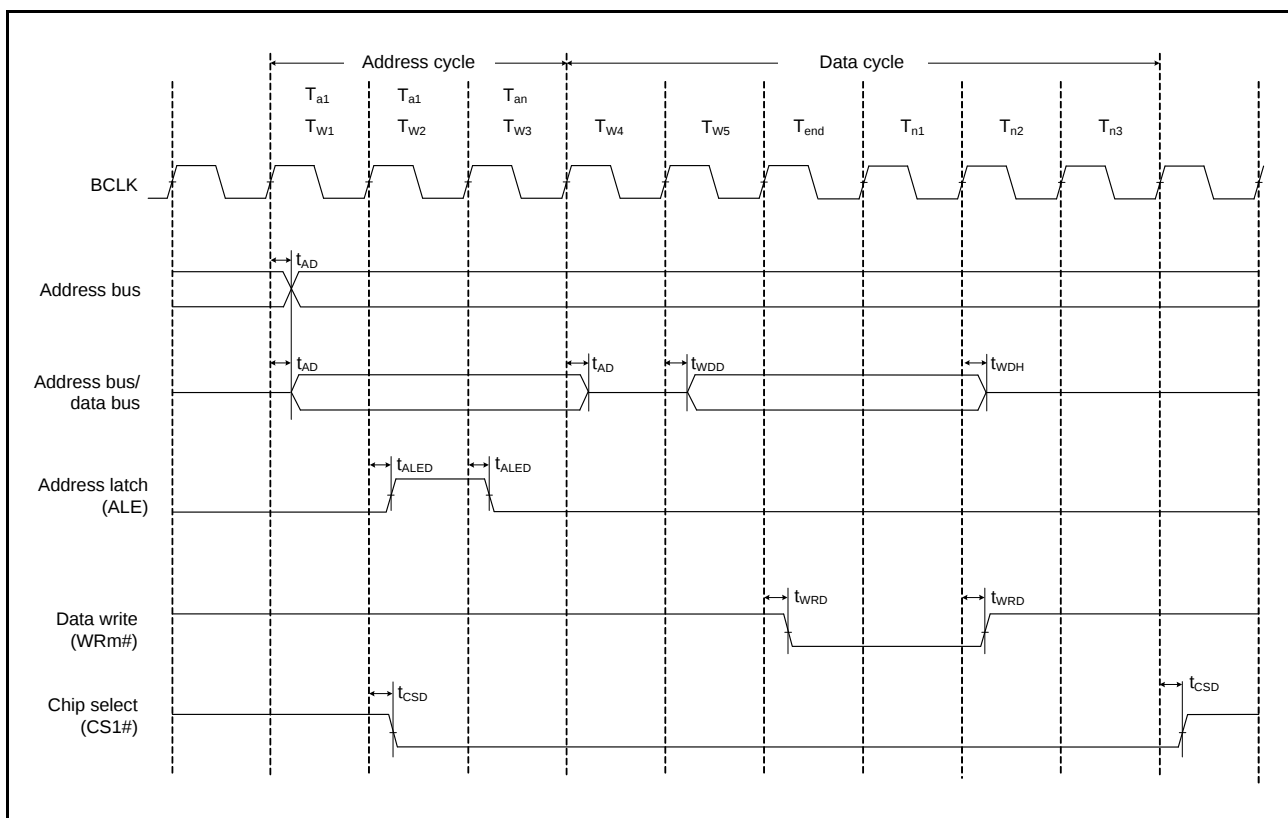
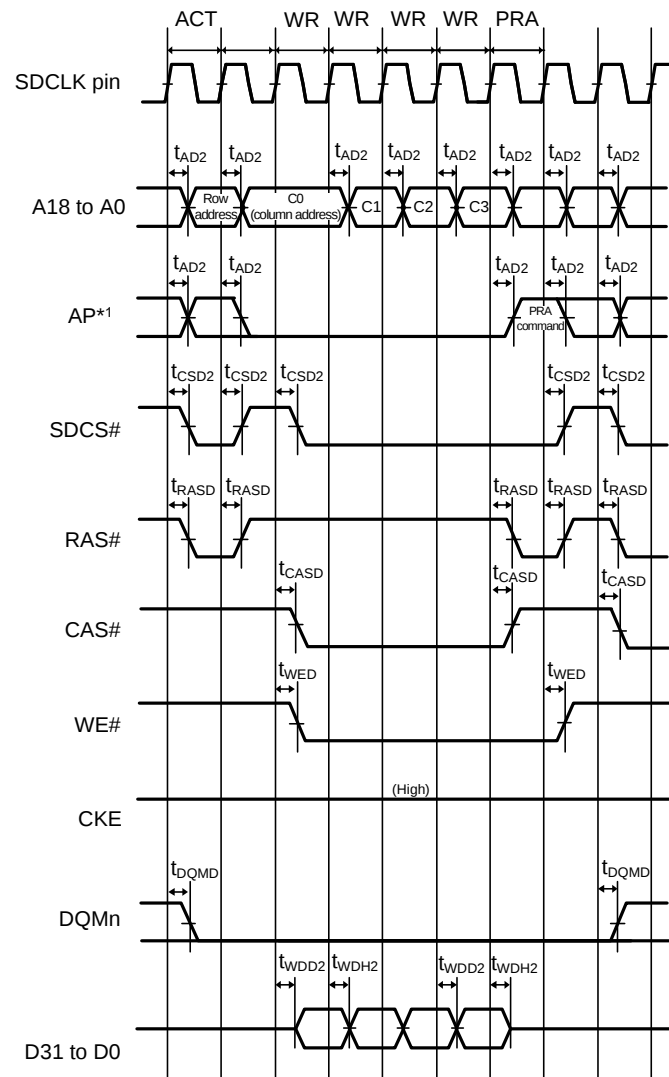


Figure 5.17 Address/Data Multiplexed Bus Write Access Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.26 SDRAM Space Multiple Write Bus Timing

Table 5.37 RIIC Timing (2)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 High-drive output is selected by the driving ability control register.

	Item	Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 5.56
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 20$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PBcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PBcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle, t_{PBcyc} : PCLKB cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

Table 5.40 ETHERC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
High-drive output is selected by the driving ability control register.

	Item	Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 5.62 to Figure 5.64
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_XXXX*1 output delay time	T_{co}	2.5	15.0	ns	
	RMII_XXXX*2 setup time	T_{su}	3	—	ns	
	RMII_XXXX*2 hold time	T_{hd}	1	—	ns	
	RMII_XXXX*1, *2 rise/fall time	T_r/T_f	0.5	5	ns	
	ET_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.66
ETHERC (MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t_{TEND}	1	20	ns	Figure 5.67
	ET_ETXD0 to ET_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET_CRs setup time	t_{CRSs}	10	—	ns	
	ET_CRs hold time	t_{CRSh}	10	—	ns	
	ET_COL setup time	t_{COLs}	10	—	ns	Figure 5.68
	ET_COL hold time	t_{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 5.69
	ET_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.70
	ET_RX_ER hold time	t_{RESh}	10	—	ns	
	ET_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.71

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0

Note 2. RMII_CRs_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

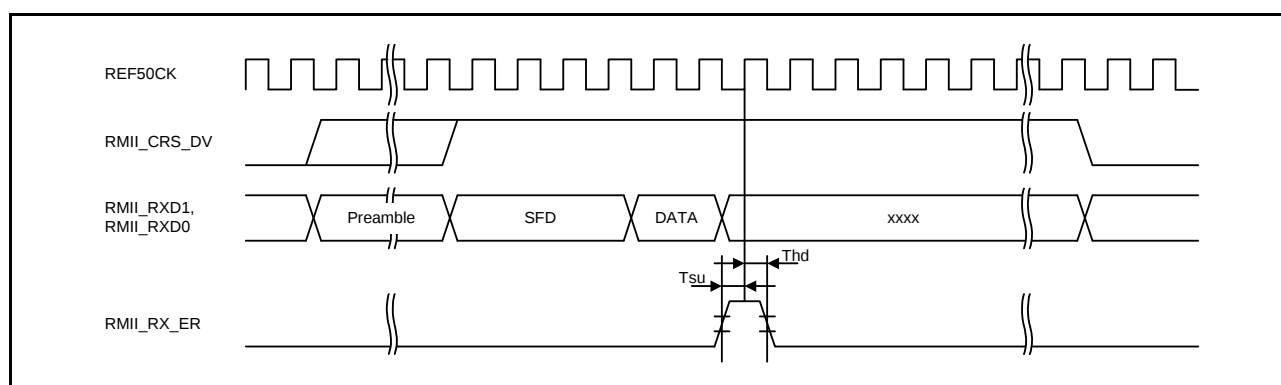


Figure 5.65 RMII Reception Timing (Error Occurrence)

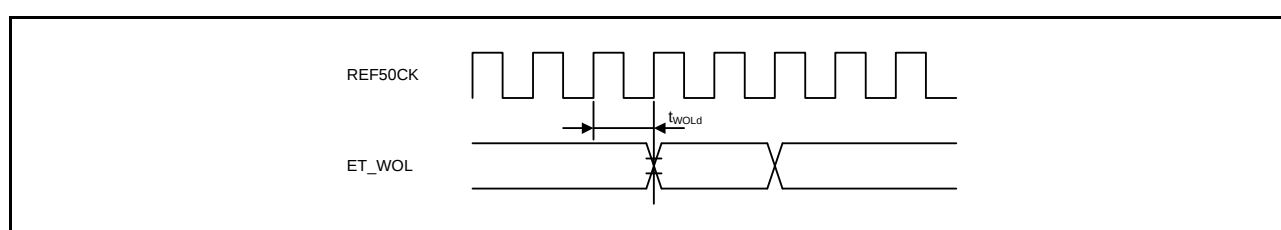


Figure 5.66 WOL Output Timing (RMII)

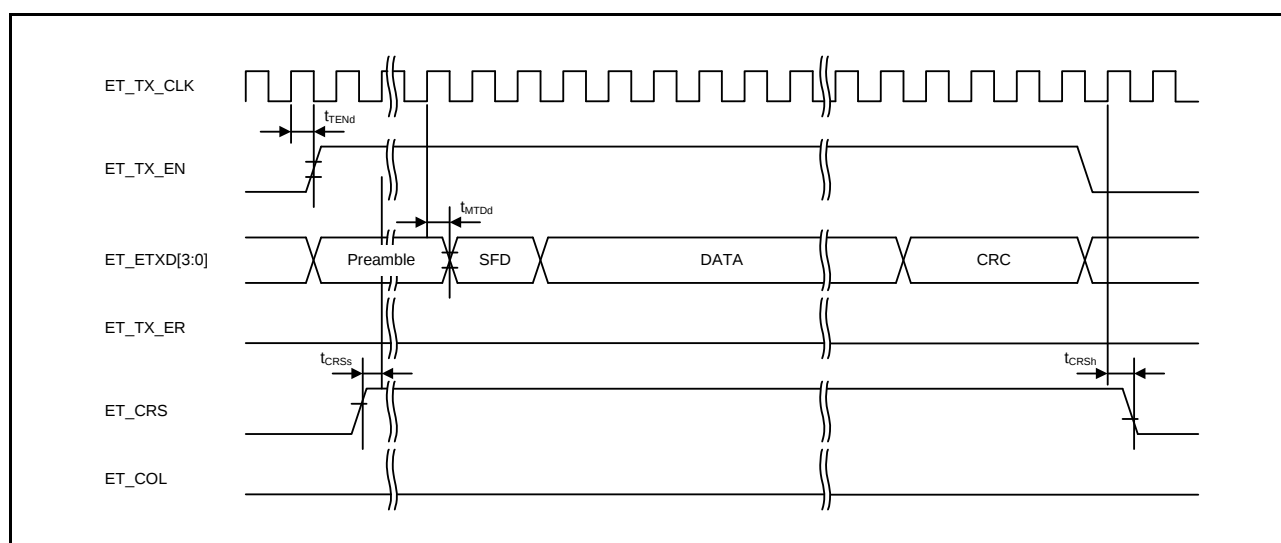


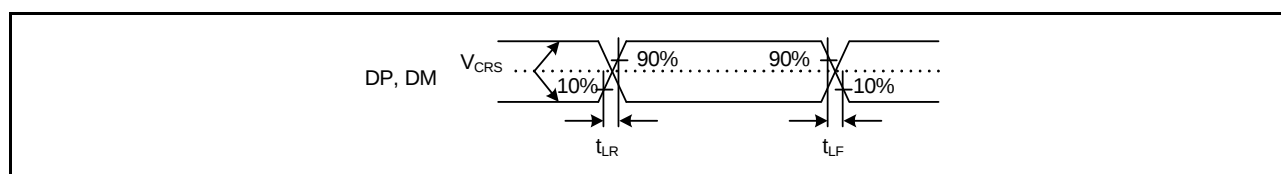
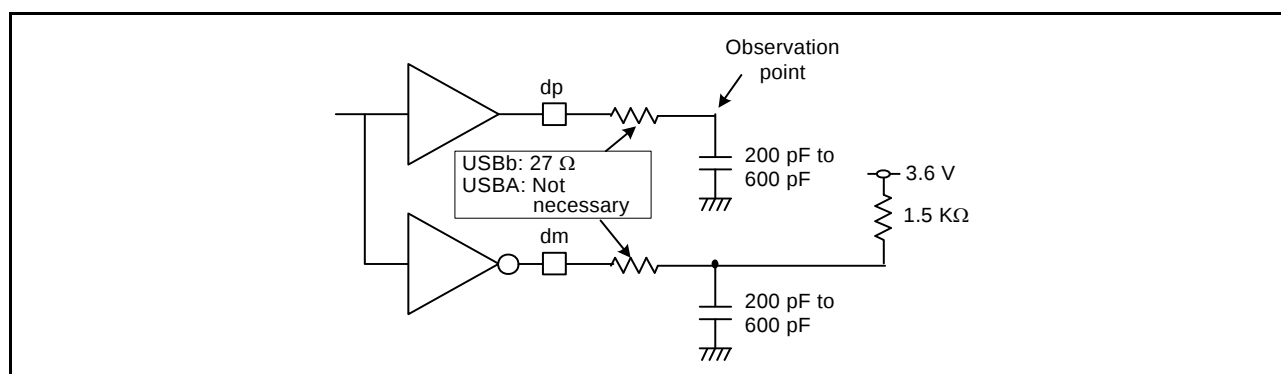
Figure 5.67 MII Transmission Timing (Normal Operation)

5.4 USB Characteristics

Table 5.42 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 3.0$ to 3.6 V, $3.0 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{CC_USBA} = AV_{CC_USBA} = 3.0$ to 3.6 V,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $USBA_RREF = 2.2$ k $\Omega \pm 1\%$, $USBMCLK = 20/24$ MHz, $UCLK = 48$ MHz,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V
	Input low level voltage	V_{IL}	—	—	0.8	V
	Differential input sensitivity	V_{DI}	0.2	—	—	V DP – DM
	Differential common mode range	V_{CM}	0.8	—	2.5	V
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V $I_{OH} = -200$ μ A
	Output low level voltage	V_{OL}	0.0	—	0.3	V $I_{OL} = 2$ mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V Figure 5.75
	Rise time	t_{LR}	75	—	300	ns
	Fall time	t_{LF}	75	—	300	ns
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	% t_{LR} / t_{LF}
Pull-up and pull-down characteristics	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	k Ω

**Figure 5.75 DP and DM Output Timing (Low Speed)****Figure 5.76 Test Circuit (Low Speed)**