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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l35ccd-fp-31

Table 1.5 Specifications (2)

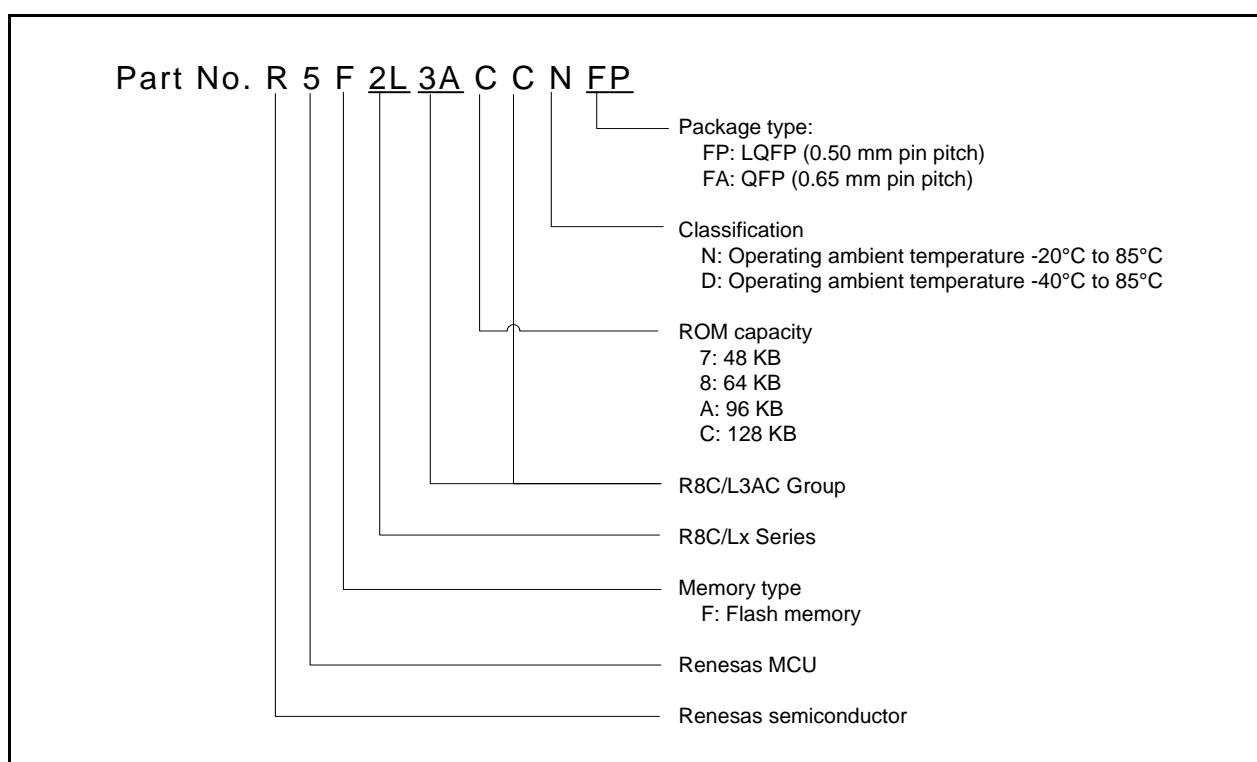
Item	Function	Specification	
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode	
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode	
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)	
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output: 6 pins, sawtooth wave modulation), complementary PWM mode (three-phase waveform output: 6 pins, triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)	
	Timer RE	8 bits × 1 Real-time clock mode (counting of seconds, minutes, hours, days of week), output compare mode	
	Timer RG	16 bits × 1 Phase-counting mode, timer mode (output compare function, input capture function), PWM mode (output: 1 pin)	
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART × 2 channels	
	UART2	Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), multiprocessor communication function	
Synchronous Serial Communication Unit (SSU)		1 (shared with I ² C-bus)	
I ² C bus		1 (shared with SSU)	
LIN Module		Hardware LIN: 1 channel (timer RA, UART0 used)	
A/D Converter	R8C/L35C Group	10-bit resolution × 10 channels, including sample and hold function, with sweep mode	
	R8C/L36C Group	10-bit resolution × 10 channels, including sample and hold function, with sweep mode	
	R8C/L38C Group	10-bit resolution × 16 channels, including sample and hold function, with sweep mode	
	R8C/L3AC Group	10-bit resolution × 20 channels, including sample and hold function, with sweep mode	
D/A Converter		8-bit resolution × 2 circuits	
Comparator B		2 circuits	
LCD Drive Control Circuit	R8C/L35C Group	Common output: Max. 4 pins Segment output: Max. 24 pins	Bias: 1/2, 1/3 Duty: static, 1/2, 1/3, 1/4
	R8C/L36C Group	Common output: Max. 8 pins Segment output: Max. 32 pins ⁽¹⁾	Bias: 1/2, 1/3, 1/4 Duty: static, 1/2, 1/3, 1/4, 1/8
	R8C/L38C Group	Common output: Max. 8 pins Segment output: Max. 48 pins ⁽¹⁾	
	R8C/L3AC Group	Common output: Max. 8 pins Segment output: Max. 56 pins ⁽¹⁾	
	Voltage multiplier and dedicated regulator integrated		

Note:

1. This applies when four pins are selected for common output.

Table 1.10 Product List for R8C/L3AC Group**Current of Apr 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L3A7CNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7CNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8CNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8CNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AACNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AACNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3A7CDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7CDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8CDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8CDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AACDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AACDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	

**Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/L3AC Group**

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/L35C Group. Figure 1.6 shows a Block Diagram of R8C/L36C Group. Figure 1.7 shows a Block Diagram of R8C/L38C Group. Figure 1.8 shows a Block Diagram of R8C/L3AC Group.

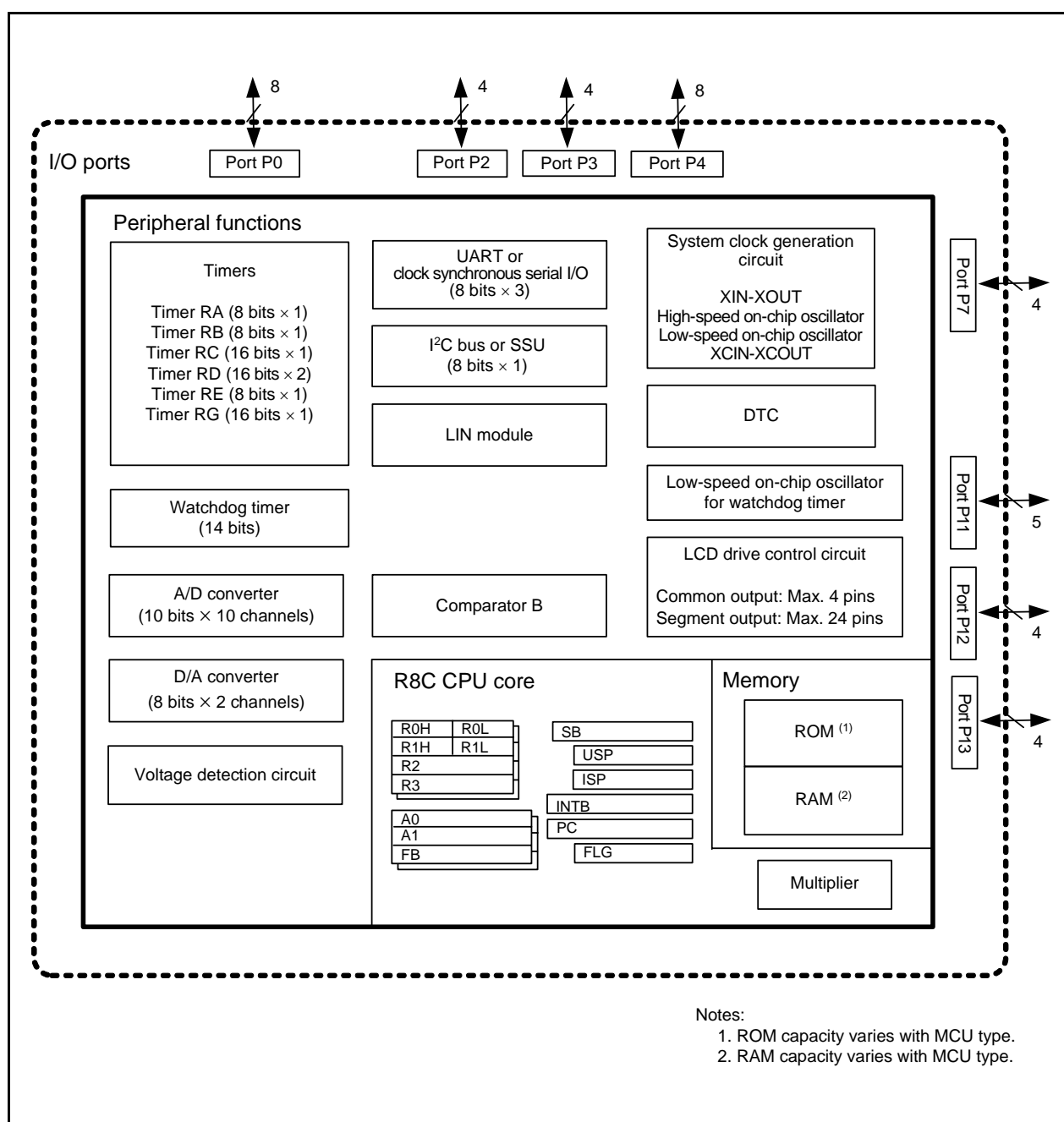


Figure 1.5 Block Diagram of R8C/L35C Group

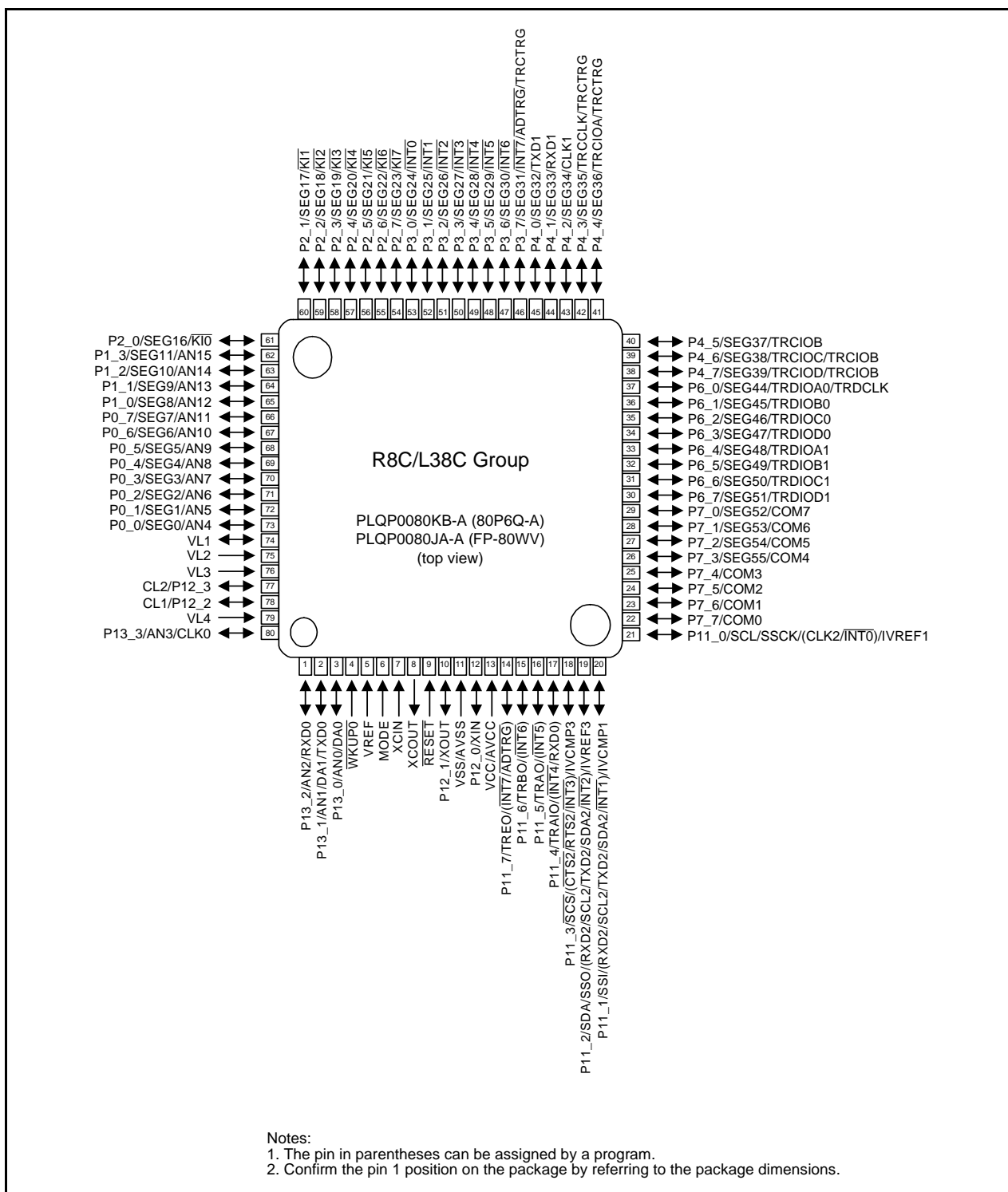


Figure 1.11 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages

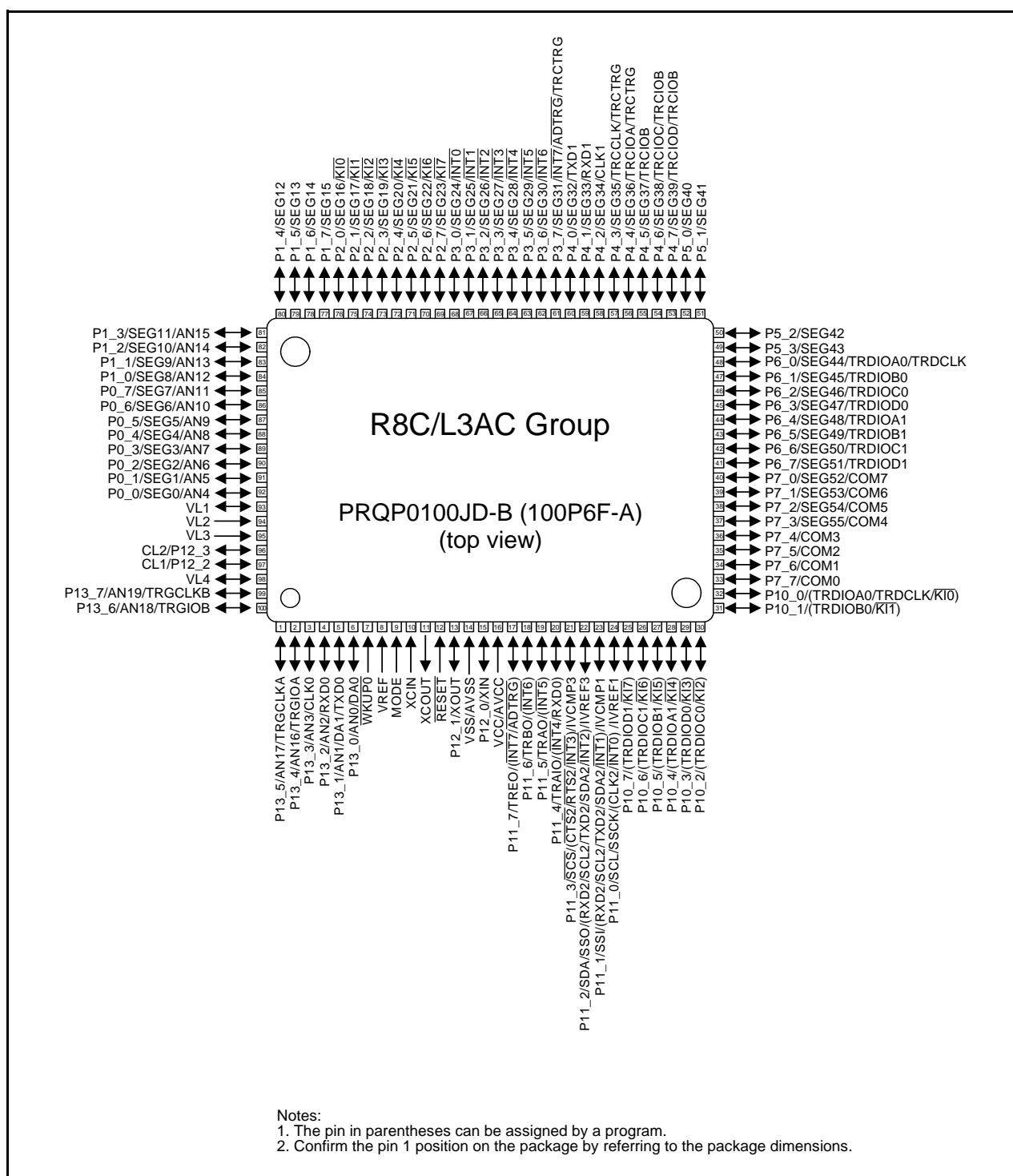


Figure 1.13 Pin Assignment (Top View) of PRQP0100JD-B Package

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	00h
01E1h	Port P1 Pull-Up Control Register	P1PUR	00h
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h	Port P3 Pull-Up Control Register	P3PUR	00h
01E4h	Port P4 Pull-Up Control Register	P4PUR	00h
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h	Port P6 Pull-Up Control Register	P6PUR	00h
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h			
01E9h			
01EAh	Port P10 Pull-Up Control Register	P10PUR	00h
01EBh	Port P11 Pull-Up Control Register	P11PUR	00h
01ECh	Port P12 Pull-Up Control Register	P12PUR	00h
01EDh	Port P13 Pull-Up Control Register	P13PUR	00h
01EEh			
01EFh			
01F0h	Port P10 Drive Capacity Control Register	P10DRR	00h
01F1h	Port P11 Drive Capacity Control Register	P11DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
0280h	LCD Display Control Data Register	LRA16H	XXh
0281h		LRA17H	XXh
0282h		LRA18H	XXh
0283h		LRA19H	XXh
0284h		LRA20H	XXh
0285h		LRA21H	XXh
0286h		LRA22H	XXh
0287h		LRA23H	XXh
0288h		LRA24H	XXh
0289h		LRA25H	XXh
028Ah		LRA26H	XXh
028Bh		LRA27H	XXh
028Ch		LRA28H	XXh
028Dh		LRA29H	XXh
028Eh		LRA30H	XXh
028Fh		LRA31H	XXh
0290h		LRA32H	XXh
0291h		LRA33H	XXh
0292h		LRA34H	XXh
0293h		LRA35H	XXh
0294h		LRA36H	XXh
0295h		LRA37H	XXh
0296h		LRA38H	XXh
0297h		LRA39H	XXh
0298h		LRA40H	XXh
0299h		LRA41H	XXh
029Ah		LRA42H	XXh
029Bh		LRA43H	XXh
029Ch		LRA44H	XXh
029Dh		LRA45H	XXh
029Eh		LRA46H	XXh
029Fh		LRA47H	XXh
02A0h		LRA48H	XXh
02A1h		LRA49H	XXh
02A2h		LRA50H	XXh
02A3h		LRA51H	XXh
02A4h		LRA52H	XXh
02A5h		LRA53H	XXh
02A6h		LRA54H	XXh
02A7h		LRA55H	XXh
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
02C0h			
02C1h			
02C2h			
02C3h			
02C4h			
02C5h			
02C6h			
02C7h			
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h			
02E1h			
02E2h			
02E3h			
02E4h			
02E5h			
02E6h			
02E7h			
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh			
02FFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions
(VCC = 1.8 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter			Conditions	Standard			Unit	
					Min.	Typ.	Max.		
Vcc/AVcc	Supply voltage				1.8	—	5.5	V	
Vss/AVss	Supply voltage				—	0	—	V	
VIH	Input “H” voltage	Other than CMOS input		4.0 V ≤ Vcc ≤ 5.5 V	0.8 Vcc	—	Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0.8 Vcc	—	Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0.9 Vcc	—	Vcc	V	
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
VIL	Input “L” voltage	Other than CMOS input		4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0	—	0.05 Vcc	V	
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)			—	—	−160	mA	
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(avg)			—	—	−80	mA	
IOH(peak)	Peak output “H” current	Port P10, P11 (2)			—	—	−40	mA	
		Other pins			—	—	−10	mA	
IOH(avg)	Average output “H” current (1)	Port P10, P11 (2)			—	—	−20	mA	
		Other pins			—	—	−5	mA	
IoL(sum)	Peak sum output “L” current	Sum of all pins IoL(peak)			—	—	160	mA	
IoL(sum)	Average sum output “L” current	Sum of all pins IoL(avg)			—	—	80	mA	
IoL(peak)	Peak output “L” current	Port P10, P11 (2)			—	—	40	mA	
		Other pins			—	—	10	mA	
IoL(avg)	Average output “L” current (1)	Port P10, P11 (2)			—	—	20	mA	
		Other pins			—	—	5	mA	
f(XIN)	XIN clock input oscillation frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
f(XCIN)	XCIN clock input oscillation frequency			1.8 V ≤ Vcc ≤ 5.5 V	—	32.768	50	kHz	
fOCO40M	When used as the count source for timer RC, timer RD, or timer RG (3)			2.7 V ≤ Vcc ≤ 5.5 V	32	—	40	MHz	
fOCO-F	fOCO-F frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
—	System clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
f(BCLK)	CPU clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	

Notes:

1. The average output current indicates the average value of current measured during 100 ms.
2. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.
3. fOCO40M can be used as the count source for timer RC, timer RD, or timer RG in the range of VCC = 2.7 V to 5.5V.

Table 5.6 Flash Memory (Program ROM) Characteristics
(VCC = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽¹⁾		1,000 ⁽²⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	ms
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁶⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. Definition of programming/erasure endurance
 The programming and erasure endurance is defined on a per-block basis.
 If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7 Flash Memory (Data flash Block A to Block D) Characteristics
(V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽¹⁾		10,000 ⁽²⁾	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	ms
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20 ⁽⁶⁾	—	85	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

- Definition of programming/erasure endurance
 The programming and erasure endurance is defined on a per-block basis.
 If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 40°C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.

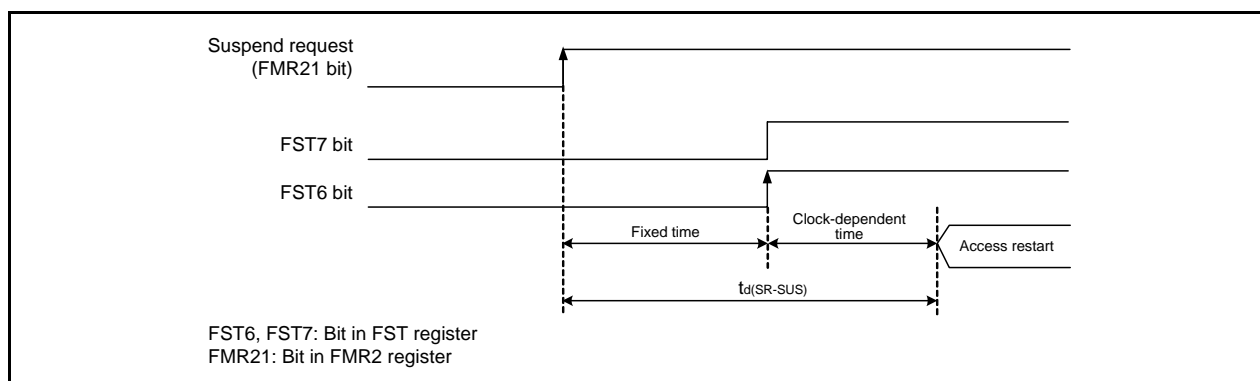


Figure 5.2 Time delay until Suspend

Table 5.12 High-speed On-Chip Oscillator Circuit Characteristics
(VCC = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	VCC = 1.8 V to 5.5 V –20°C ≤ T _{opr} ≤ 85°C	38.4	40	41.6	MHz
		VCC = 1.8 V to 5.5 V –40°C ≤ T _{opr} ≤ 85°C	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽¹⁾	VCC = 1.8 V to 5.5 V –20°C ≤ T _{opr} ≤ 85°C	35.389	36.864	38.338	MHz
		VCC = 1.8 V to 5.5 V –40°C ≤ T _{opr} ≤ 85°C	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	VCC = 1.8 V to 5.5 V –20°C ≤ T _{opr} ≤ 85°C	30.72	32	33.28	MHz
		VCC = 1.8 V to 5.5 V –40°C ≤ T _{opr} ≤ 85°C	30.40	32	33.60	MHz
—	Oscillation stability time	VCC = 5.0 V, T _{opr} = 25°C	—	0.5	3	ms
—	Self power consumption at oscillation	VCC = 5.0 V, T _{opr} = 25°C	—	400	—	μA

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.13 Low-speed On-Chip Oscillator Circuit Characteristics
(VCC = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		112.5	125	137.5	kHz
—	Oscillation stability time	VCC = 5.0 V, T _{opr} = 25°C	—	30	100	μs
—	Self power consumption at oscillation	VCC = 5.0 V, T _{opr} = 25°C	—	3	—	μA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
—	Oscillation stability time	VCC = 5.0 V, T _{opr} = 25°C	—	30	100	μs
—	Self power consumption at oscillation	VCC = 5.0 V, T _{opr} = 25°C	—	2	—	μA

Table 5.14 Power Supply Circuit Characteristics
(VCC = 1.8 to 5.5 V, VSS = 0 V, and T_{opr} = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽¹⁾		—	—	2000	μs

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.15 LCD Drive Control Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C
(D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL4	2.2	—	5.5	V
VL3	VL3 voltage		VL2	—	VL4	V
VL2	VL2 voltage	R8C/L35C	VL1	—	VL4	V
		R8C/L36C, R8C/L38C, R8C/L3AC	VL1	—	VL3	V
VL1	VL1 voltage		1	—	VL2 (3)	V
—	VL1 internally-generated voltage accuracy (1)		Setting voltage –0.2	Setting voltage	Setting voltage +0.2	V
f(FR)	Frame frequency		50	—	180	Hz
ILCD	LCD drive control circuit current		—	(Note 2)	—	μA

Notes:

1. The voltage is selected with bits LVLS0 to LVLS3 in the LCR1 register.
2. Refer to **Table 5.18 DC Characteristics (2)**, **Table 5.20 DC Characteristics (4)**, and **Table 5.22 DC Characteristics (6)**.
3. The VL1 voltage should be VCC or below.

Table 5.16 Power-Off Mode Characteristics
(V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C
(D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Power-off mode operating supply voltage		2.2	—	5.5	V

Table 5.20 DC Characteristics (4) [2.7 V ≤ V_{CC} < 4.0 V]
(T_{OP} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition							Standard			Unit	
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.		
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed								
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—			—	7.0	14.5	mA
			10 MHz	Off	Off	125 kHz	No division	—			—	3.6	10	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—			—	3.0	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—			—	1.5	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—			—	7.0	14.5	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	—			—	3.0	—	mA
			Off	Off	10 MHz	125 kHz	No division	—			—	4.0	—	mA
			Off	Off	10 MHz	125 kHz	Divide-by-8	—			—	1.7	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	85	390	μA
			Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	90	400
		Off		32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM			—	50	—
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	15	90	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	5	80	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	5	—	μA
									LCD drive control circuit (5) When the internal voltage multiplier is used					
		Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	μA	
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	T _{opr} = 25°C Peripheral clock off		—	2	5.0	μA
		Power-off mode	Off	Off	Off	Off	—	—	T _{opr} = 25°C		—	0.02	0.2	μA
							T _{opr} = 85°C							

Notes:

- V_{CC} = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are V_{SS}.
- XIN is set to square wave input.
- V_{CC} = 3.0 V
- VLCD = V_{CC}, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
- The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

Table 5.22 DC Characteristics (6) [1.8 V ≤ V_{CC} < 2.7 V]
(T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed								
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	Off	125 kHz	No division	—			—	2.2	—	mA
			5 MHz	Off	Off	125 kHz	Divide-by-8	—			—	0.8	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	—			—	2.5	10	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	—			—	1.7	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	90	300	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	90	400	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM		—	45	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	15	90	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	4	80	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	4	—	μA
										LCD drive control circuit (5) When the internal voltage multiplier is used	—	11	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	μA
			Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	T _{opr} = 25°C Peripheral clock off		—	2.0	5.0
		Off		Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	T _{opr} = 85°C Peripheral clock off		—	13	—	μA
		Power-off mode	Off	Off	Off	Off	—	—	T _{opr} = 25°C		—	0.02	0.2	μA
			Off	Off	Off	Off	—	—	T _{opr} = 85°C		—	0.3	—	μA

Notes:

- V_{CC} = 1.8 V to 2.7 V, single chip mode, output pins are open, and other pins are V_{SS}.
- XIN is set to square wave input.
- V_{CC} = 2.2 V
- VLCD = V_{CC}, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
- The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

5.5 AC Characteristics

Table 5.23 Timing Requirements of Synchronous Serial Communication Unit (SSU)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	—	—	tcyc (1)
tHI	SSCK clock "H" width			0.4	—	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	—	0.6	tsucyc
trISE	SSCK clock rising time	Master		—	—	1	tcyc (1)
		Slave		—	—	1	μs
tFALL	SSCK clock falling time	Master		—	—	1	tcyc (1)
		Slave		—	—	1	μs
tsu	SSO, SSI data input setup time			100	—	—	ns
tH	SSO, SSI data input hold time			1	—	—	tcyc (1)
tLEAD	SCS setup time	Slave		1tcyc + 50	—	—	ns
tLAG	SCS hold time	Slave		1tcyc + 50	—	—	ns
tOD	SSO, SSI data output delay time			—	—	1	tcyc (1)
tsA	SSI slave access time		2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ V _{CC} < 2.7 V	—	—	1.5tcyc + 200	ns
toR	SSI slave out open time		2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ V _{CC} < 2.7 V	—	—	1.5tcyc + 200	ns

Note:

1. 1tcyc = 1/f₁(s)

Table 5.27 Timing Requirements of Serial Interface
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (CK)	CLKi input cycle time	800	—	300	—	200	—	ns
t _w (CKH)	CLKi input "H" width	400	—	150	—	100	—	ns
t _w (CKL)	CLKi input "L" width	400	—	150	—	100	—	ns
t _d (C-Q)	TXDi output delay time	—	200	—	80	—	50	ns
t _h (C-Q)	TXDi hold time	0	—	0	—	0	—	ns
t _{su} (D-C)	RXDi input setup time	150	—	70	—	50	—	ns
t _h (C-D)	RXDi input hold time	90	—	90	—	90	—	ns

$i = 0$ to 2

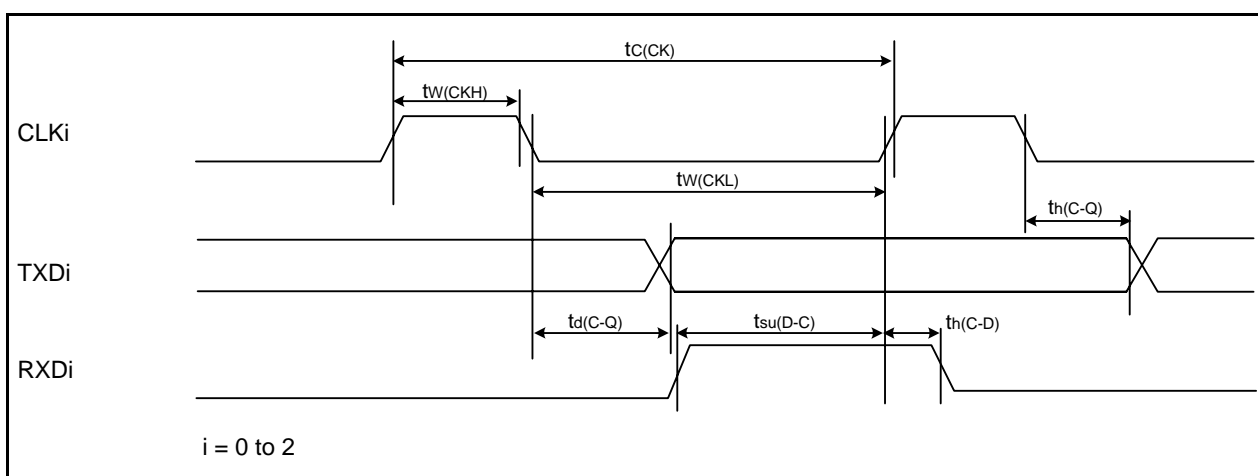


Figure 5.10 Input and Output Timing of Serial Interface

Table 5.28 Timing Requirements of External Interrupt $\overline{\text{INTi}}$ ($i = 0$ to 7) and Key Input Interrupt $\overline{\text{Kli}}$ ($i = 0$ to 7)
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tw(INH)	$\overline{\text{INTi}}$ input “H” width, $\overline{\text{Kli}}$ input “H” width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
tw(INL)	$\overline{\text{INTi}}$ input “L” width, $\overline{\text{Kli}}$ input “L” width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

Notes:

- When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

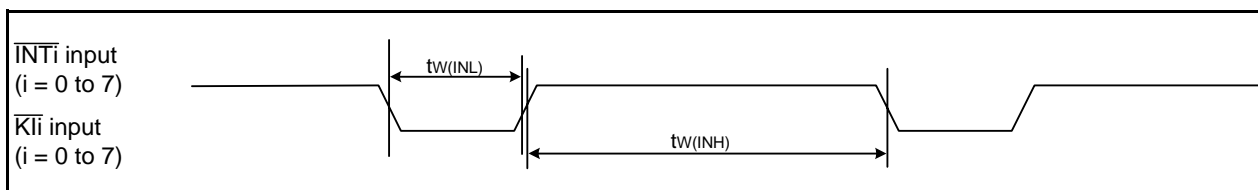


Figure 5.11 Input Timing of External Interrupt $\overline{\text{INTi}}$ and Key Input Interrupt $\overline{\text{Kli}}$

REVISION HISTORY	R8C/L35C Group, R8C/L36C Group, R8C/L38C Group, R8C/L3AC Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Oct 30, 2009	—	First Edition issued
0.20	Apr 15, 2011	6 7 7 to 10 24 29 45 to 68	Table 1.6 Function deleted, Current consumption revised 1.2 “of R8C/Lx Series” → “for Each Group” Tables 1.7 to 1.10 revised Table 1.15 “Voltage detection circuit” deleted 4. Special Function Registers (SFRs) “The description offered in this chapter is based on the R8C/L3AC Group.” added 5. Electrical Characteristics added
1.00	Jun 25, 2010	— 1 7 to 10 45 55 69 to 72	“Preliminary” and “Under development” deleted 1.1 revised Tables 1.7 to 1.10 revised Tables 5.1 Note 2 added Table 5.15 Note 3 added Package Dimensions revised
1.01	Apr 15, 2011	2 3 6 11 to 14 20 to 22 23, 24 28 38 to 40 48 57, 59, 61	Table 1.1 revised Table 1.2 Note 2, Table 1.3 Note 1 revised Table 1.6 “Flash Memory” revised Figure 1.5 to Figure 1.8 revised Table 1.11 to Table 1.13 “Voltage Detection Circuit” deleted Table 1.14 and Table 1.15 title “for R8C/L3AC Group” added 3. “The internal ROM ... with address 0FFFFh.” deleted Table 4.10 to Table 4.12 “0248h to 026Fh”, “02A8h to 02BFh”, “02C0h to 02CFh” revised Table 5.3 “tCONV”, “tSAMP” revised Table 5.18, Table 5.20, Table 5.22 “High-Speed” → “High-Speed (fOCO-F)”

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