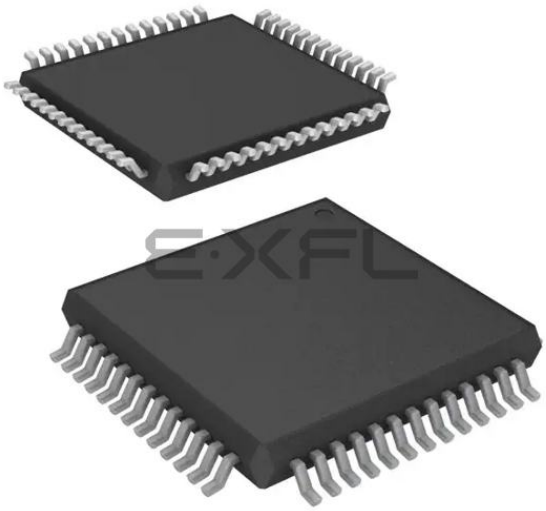
Renesas Electronics America Inc - R5F2L35CCNFP#30 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l35ccnfp-30

Table 1.10 Product List for R8C/L3AC Group **Current of Apr 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L3A7CNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7CNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8CNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8CNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AACNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AACNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3A7CDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7CDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8CDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8CDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AACDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AACDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	

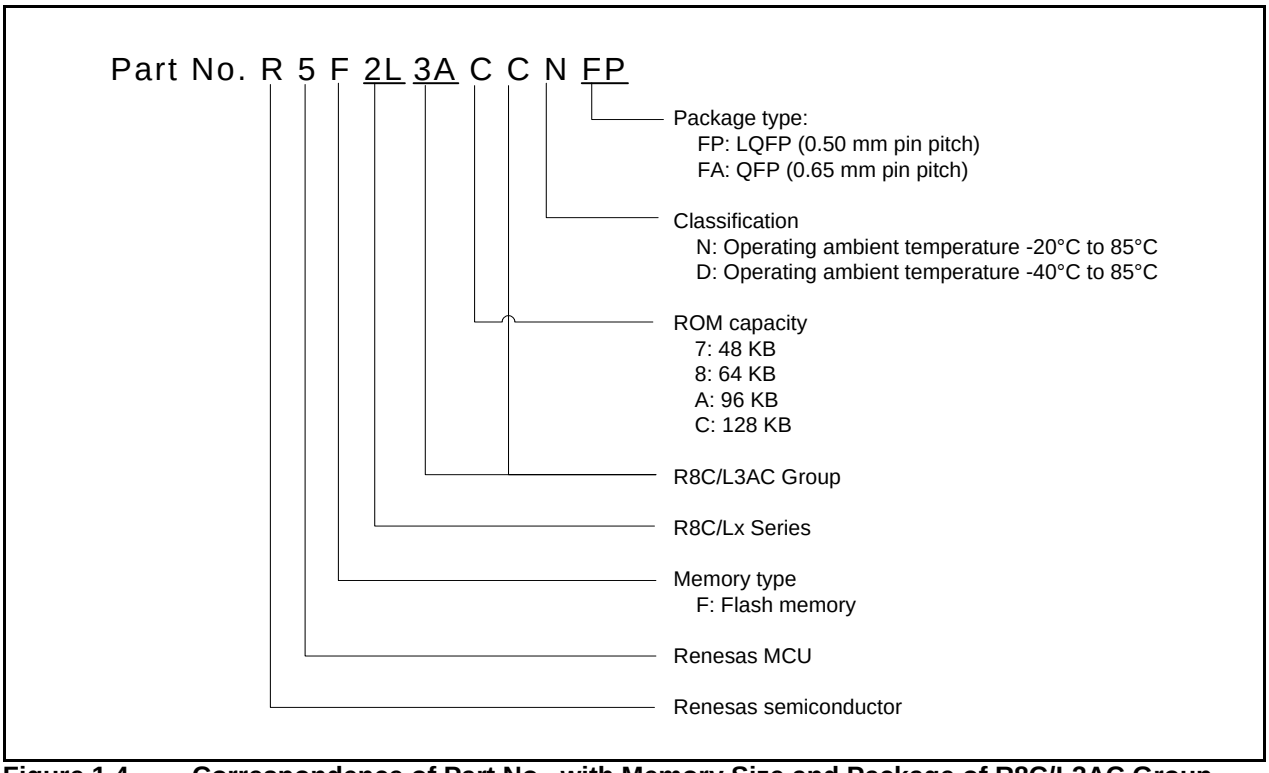
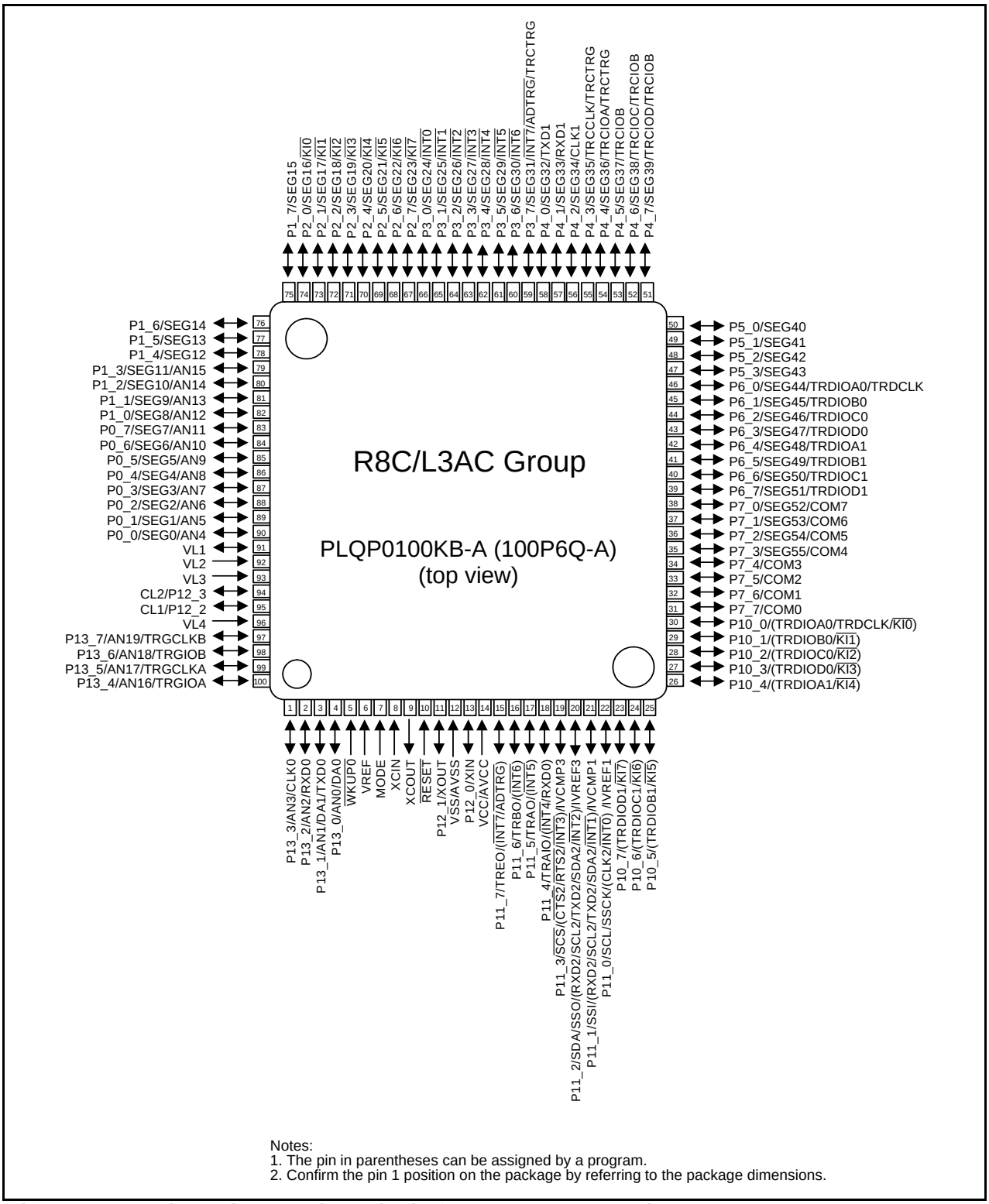
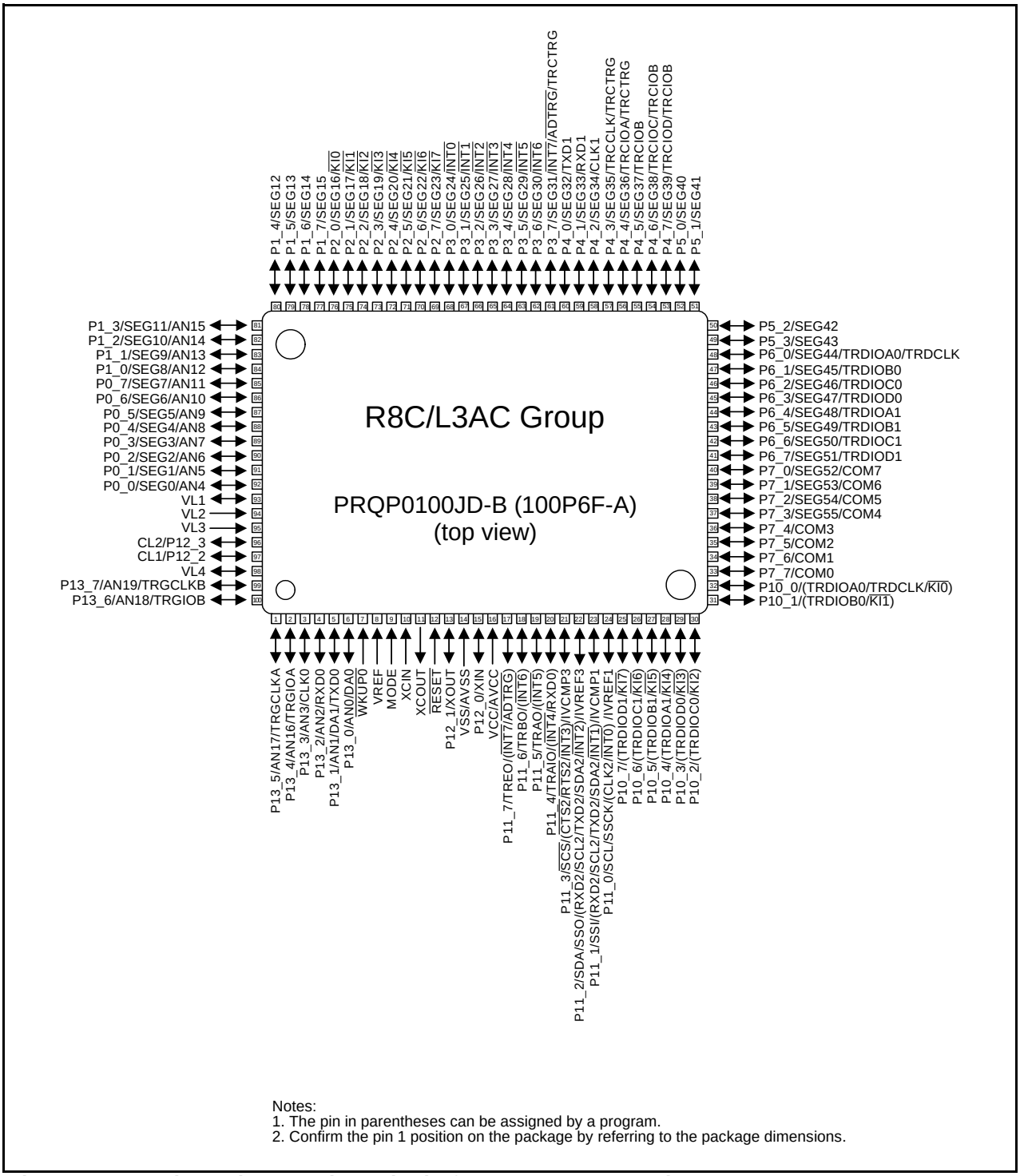


Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/L3AC Group



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.12 Pin Assignment (Top View) of PLQP0100KB-A Package



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.13 Pin Assignment (Top View) of PRQP0100JD-B Package

Table 1.13 Pin Name Information by Pin Number (3)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
85 [87]	68	49	40		P0_5						AN9	SEG5
86 [88]	69	50	41		P0_4						AN8	SEG4
87 [89]	70	51	42		P0_3						AN7	SEG3
88 [90]	71	52	43		P0_2						AN6	SEG2
89 [91]	72	53	44		P0_1						AN5	SEG1
90 [92]	73	54	45		P0_0						AN4	SEG0
91 [93]	74	55	46									VL1
92 [94]	75	56	47									VL2
93 [95]	76	57										VL3
94 [96]	77	58	48		P12_3							CL2
95 [97]	78	59	49		P12_2							CL1
96 [98]	79	60	50									VL4
97 [99]					P13_7		TRGCLKB				AN19	
98 [100]					P13_6		TRGIOB				AN18	
99 [1]					P13_5		TRGCLKA				AN17	
100 [2]					P13_4		TRGIOA				AN16	

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.16 list SFR Informations and Table 4.17 lists the ID Code Areas and Option Function Select Area. The description offered in this chapter is based on the R8C/L3AC Group.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXh (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	X0000000b
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:
1. Blank spaces are reserved. No access is allowed.
2. The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.17 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

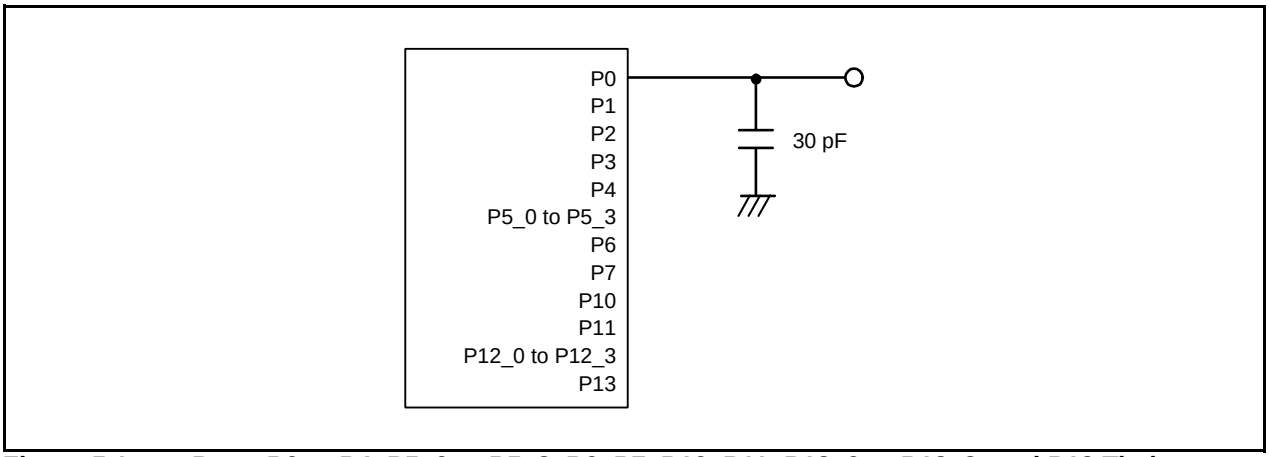


Figure 5.1 Ports P0 to P4, P5_0 to P5_3, P6, P7, P10, P11, P12_0 to P12_3, and P13 Timing Measurement Circuit

Table 5.4 D/A Converter Characteristics
(V_{CC}/AV$_{CC}$ = Vref = 2.7 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
t_{su}	Setup time		—	—	3	µs
R_O	Output resistor		—	6	—	kΩ
I_{Vref}	Reference power input current	(Note 1)	—	—	1.5	mA

Note:
1. This applies when one D/A converter is used and the value of the DAi register (i = 0 or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator B Characteristics
(V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	—	V_{CC} – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	—	V_{CC} + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (1)	V_I = Vref ± 100 mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	—	17.5	—	µA

Note:
1. When the digital filter is disabled.

Table 5.8 Voltage Detection 0 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	µs

Notes:
1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.9 Voltage Detection 1 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (1)	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (1)	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (1)	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (1)	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (1)	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (1)	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	At the falling of Vcc	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.15 LCD Drive Control Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL4	2.2	—	5.5	V
VL3	VL3 voltage		VL2	—	VL4	V
VL2	VL2 voltage	R8C/L35C	VL1	—	VL4	V
		R8C/L36C, R8C/L38C, R8C/L3AC	VL1	—	VL3	V
VL1	VL1 voltage		1	—	VL2 (3)	V
—	VL1 internally-generated voltage accuracy (1)		Setting voltage –0.2	Setting voltage	Setting voltage +0.2	V
f(FR)	Frame frequency		50	—	180	Hz
ILCD	LCD drive control circuit current		—	(Note 2)	—	µA

Notes:
1. The voltage is selected with bits LVLS0 to LVLS3 in the LCR1 register.
2. Refer to **Table 5.18 DC Characteristics (2)**, **Table 5.20 DC Characteristics (4)**, and **Table 5.22 DC Characteristics (6)**.
3. The VL1 voltage should be VCC or below.

Table 5.16 Power-Off Mode Characteristics (VCC = 2.2 to 5.5 V, VSS = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Power-off mode operating supply voltage		2.2	—	5.5	V

5.4 DC Characteristics

Table 5.17 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Port P10, P11 (1)	V_{CC} = 5V	I_{OH} = –20 mA	V_{CC} – 2.0	—	V_{CC}	V
		Other pins	V_{CC} = 5V	I_{OH} = –5 mA	V_{CC} – 2.0	—	V_{CC}	V
		XOUT	V_{CC} = 5V	I_{OH} = –200 μA	1.0	—	—	V
V_{OL}	Output “L” voltage	Port P10, P11 (1)	V_{CC} = 5V	I_{OL} = 20 mA	—	—	2.0	V
		Other pins	V_{CC} = 5V	I_{OL} = 5 mA	—	—	2.0	V
		XOUT	V_{CC} = 5V	I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{INT5}$, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, KI4, KI5, KI6, KI7, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRGCLKA, TRGCLKB, TRGIOA, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.5	—	V
		$\overline{RESET}$, $\overline{WKUP0}$			0.1	1.0	—	V
I_{IH}	Input “H” current		VI = 5.0 V, V_{CC} = 5.0 V		—	—	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5.0 V		—	—	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	14	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.22 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed								
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	Off	125 kHz	No division	—			—	2.2	—	mA
			5 MHz	Off	Off	125 kHz	Divide-by-8	—			—	0.8	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	—			—	2.5	10	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	—			—	1.7	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	90	300	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	90	400	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM		—	45	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	4	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	4	—	µA
										LCD drive control circuit (5) When the internal voltage multiplier is used	—	11	—	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2.0	5.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off		—	13	—	µA
		Power-off mode	Off	Off	Off	Off	—	—	Topr = 25°C		—	0.02	0.2	µA
			Off	Off	Off	Off	—	—	Topr = 85°C		—	0.3	—	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 2.2 V
4. VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.The standard value does not include the current that flows through external division resistors.
5. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

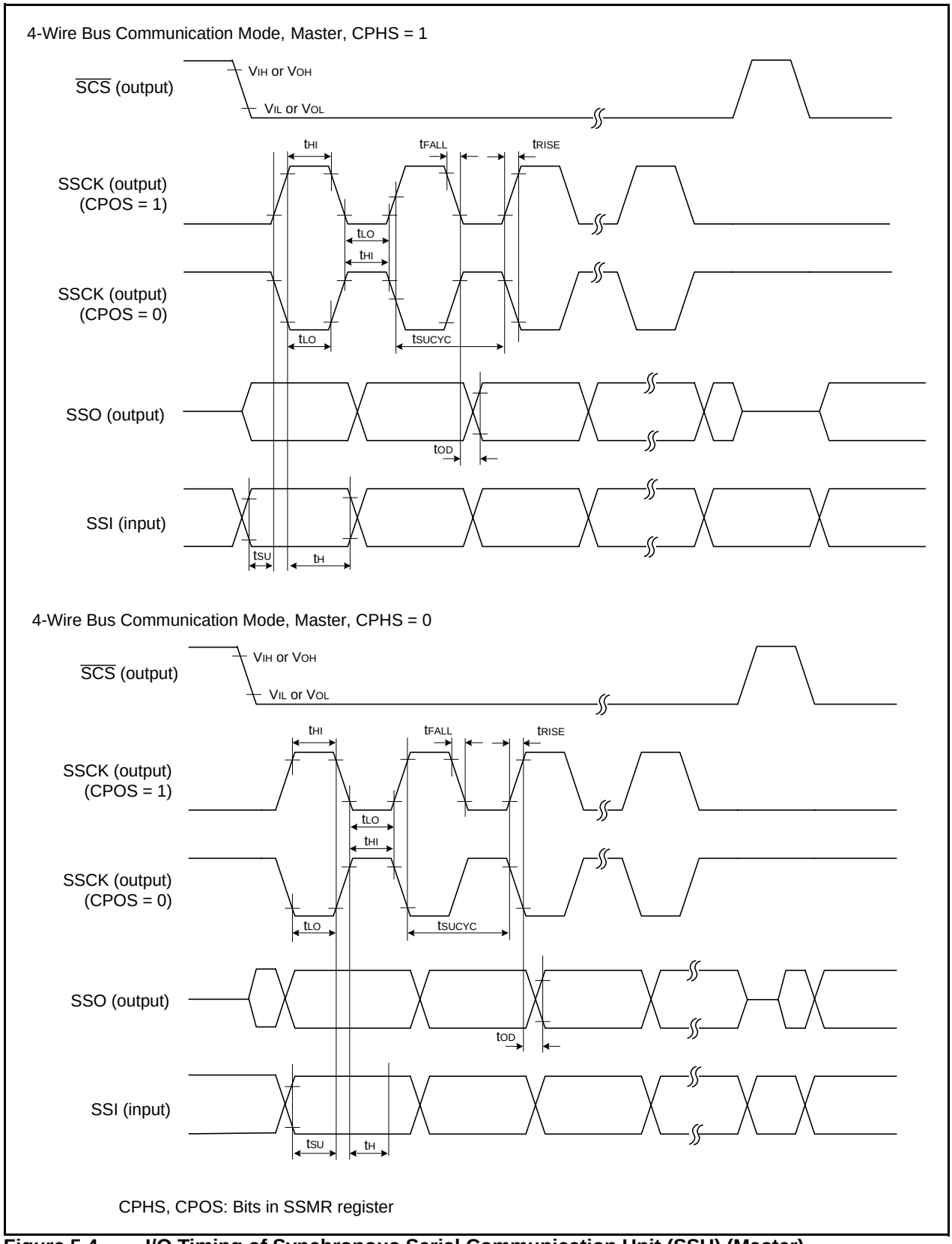


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

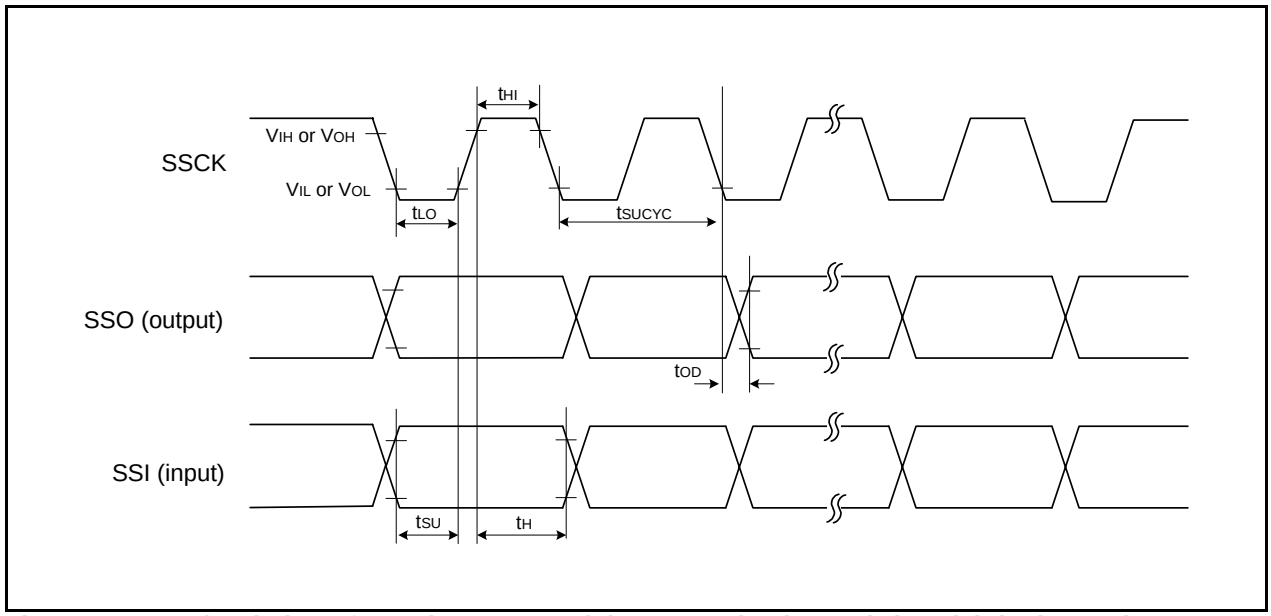
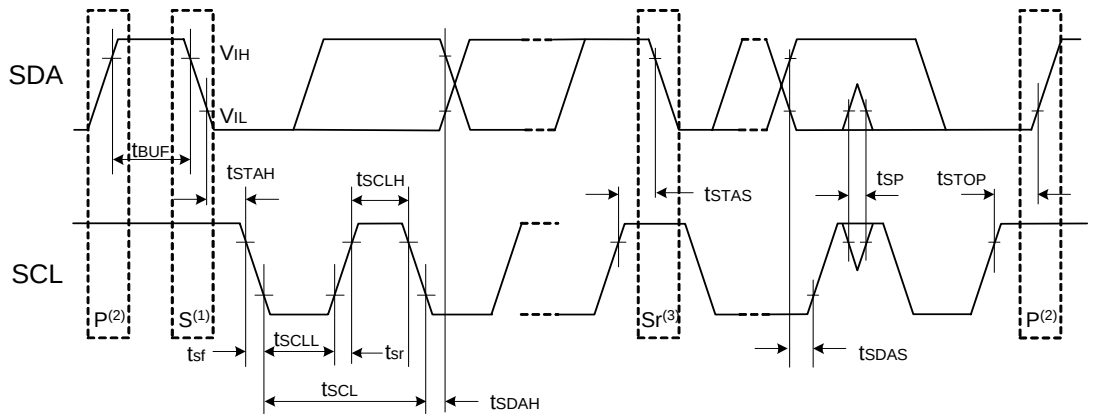


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.24 Timing Requirements of I²C bus Interface (1)
(Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
tSCL	SCL input cycle time		12tCYC + 600 (1)	—	—	ns
tSCLH	SCL input “H” width		3tCYC + 300 (1)	—	—	ns
tSCLL	SCL input “L” width		5tCYC + 500 (1)	—	—	ns
tsf	SCL, SDA input fall time		—	—	300	ns
tSP	SCL, SDA input spike pulse rejection time		—	—	1tCYC (1)	ns
tBUF	SDA input bus-free time		5tCYC (1)	—	—	ns
tSTAH	Start condition input hold time		3tCYC (1)	—	—	ns
tSTAS	Retransmit start condition input setup time		3tCYC (1)	—	—	ns
tSTOP	Stop condition input setup time		3tCYC (1)	—	—	ns
tSDAS	Data input setup time		1tCYC + 40 (1)	—	—	ns
tSDAH	Data input hold time		10	—	—	ns

Note:
1. 1tCYC = 1/f1(s)



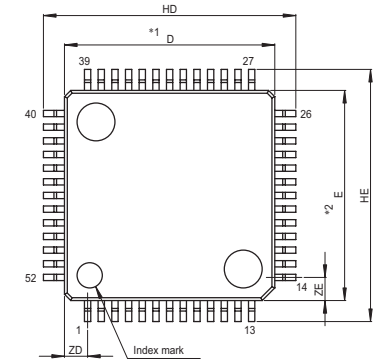
Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

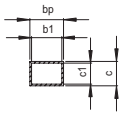
Figure 5.7 I/O Timing of I²C bus Interface

Package Dimensions

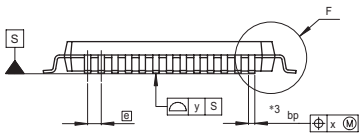
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

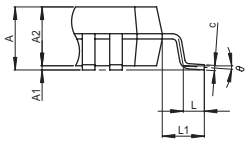
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g





Terminal cross section



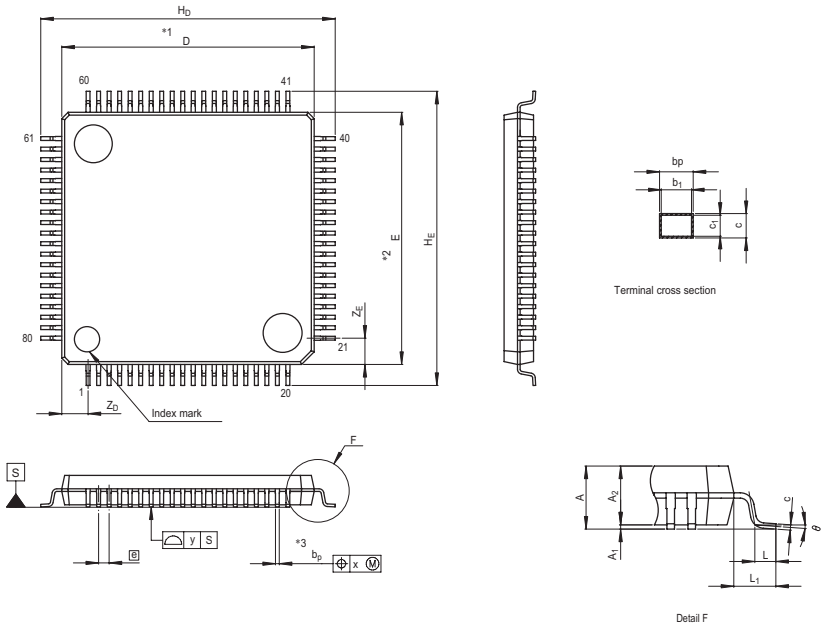


Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

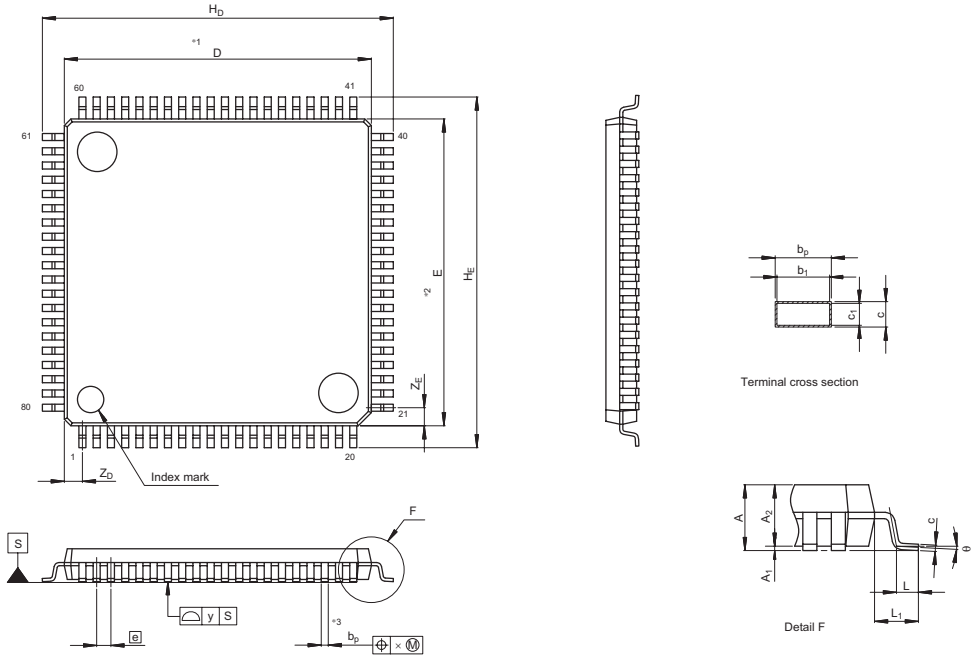
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	R8C/L35C Group, R8C/L36C Group, R8C/L38C Group, R8C/L3AC Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Oct 30, 2009	—	First Edition issued
0.20	Apr 15, 2011	6	Table 1.6 Function deleted, Current consumption revised
		7	1.2 “of R8C/Lx Series” → “for Each Group”
		7 to 10	Tables 1.7 to 1.10 revised
		24	Table 1.15 “Voltage detection circuit” deleted
		29	4. Special Function Registers (SFRs) “The description offered in this chapter is based on the R8C/L3AC Group.” added
		45 to 68	5. Electrical Characteristics added
1.00	Jun 25, 2010	—	“Preliminary” and “Under development” deleted
		1	1.1 revised
		7 to 10	Tables 1.7 to 1.10 revised
		45	Tables 5.1 Note 2 added
		55	Table 5.15 Note 3 added
		69 to 72	Package Dimensions revised
1.01	Apr 15, 2011	2	Table 1.1 revised
		3	Table 1.2 Note 2, Table 1.3 Note 1 revised
		6	Table 1.6 “Flash Memory” revised
		11 to 14	Figure 1.5 to Figure 1.8 revised
		20 to 22	Table 1.11 to Table 1.13 “Voltage Detection Circuit” deleted
		23, 24	Table 1.14 and Table 1.15 title “for R8C/L3AC Group” added
		28	3. “The internal ROM ... with address 0FFFFh.” deleted
		38 to 40	Table 4.10 to Table 4.12 “0248h to 026Fh”, “02A8h to 02BFh”, “02C0h to 02CFh” revised
		48	Table 5.3 “t_{CONV}”, “t_{SAMP}” revised
		57, 59, 61	Table 5.18, Table 5.20, Table 5.22 “High-Speed” → “High-Speed (fOCO-F)”