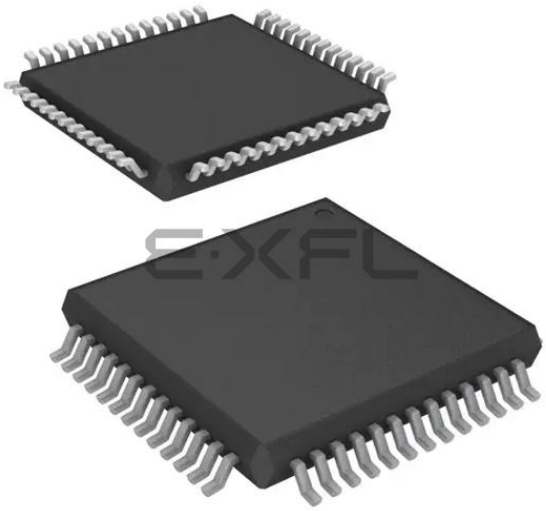


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l35ccnfp-31

Table 1.10 Product List for R8C/L3AC Group **Current of Apr 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L3A7CNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7CNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8CNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8CNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AACNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AACNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3A7CDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7CDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8CDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8CDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AACDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AACDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	

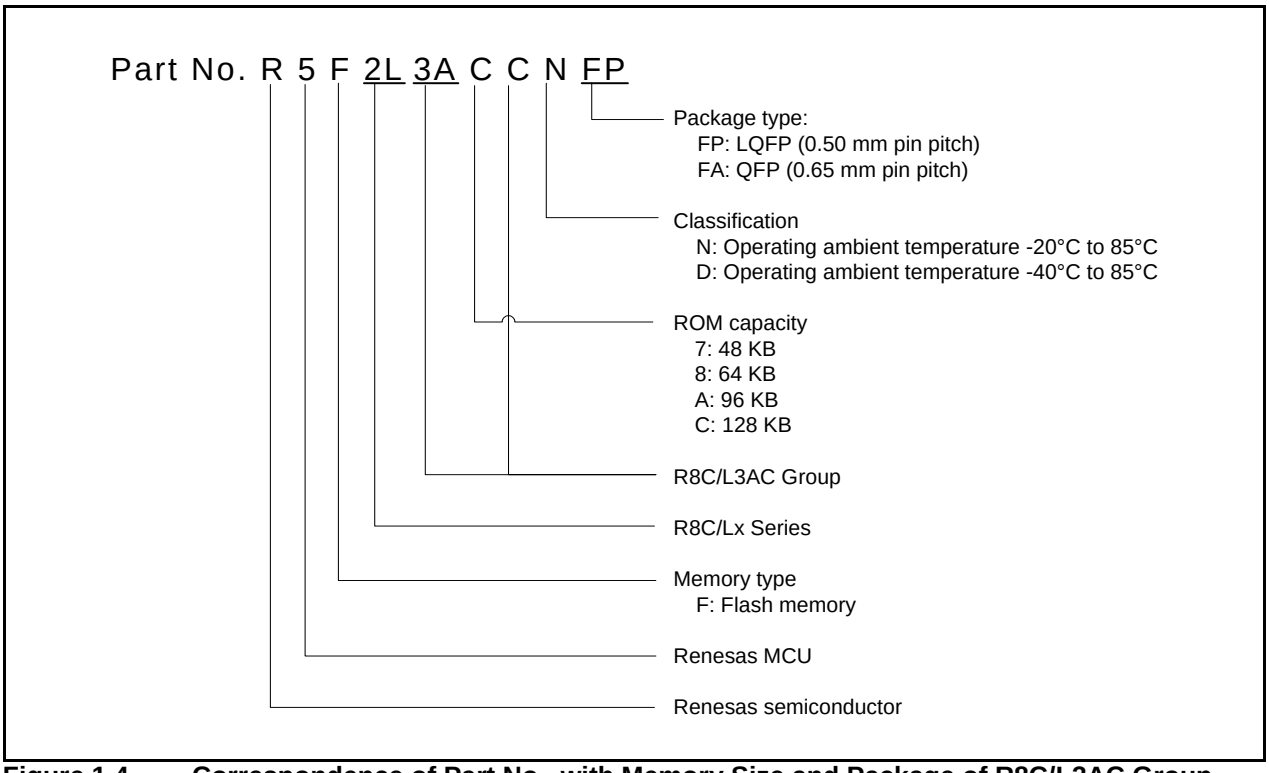


Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/L3AC Group

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/L35C Group. Figure 1.6 shows a Block Diagram of R8C/L36C Group. Figure 1.7 shows a Block Diagram of R8C/L38C Group. Figure 1.8 shows a Block Diagram of R8C/L3AC Group.

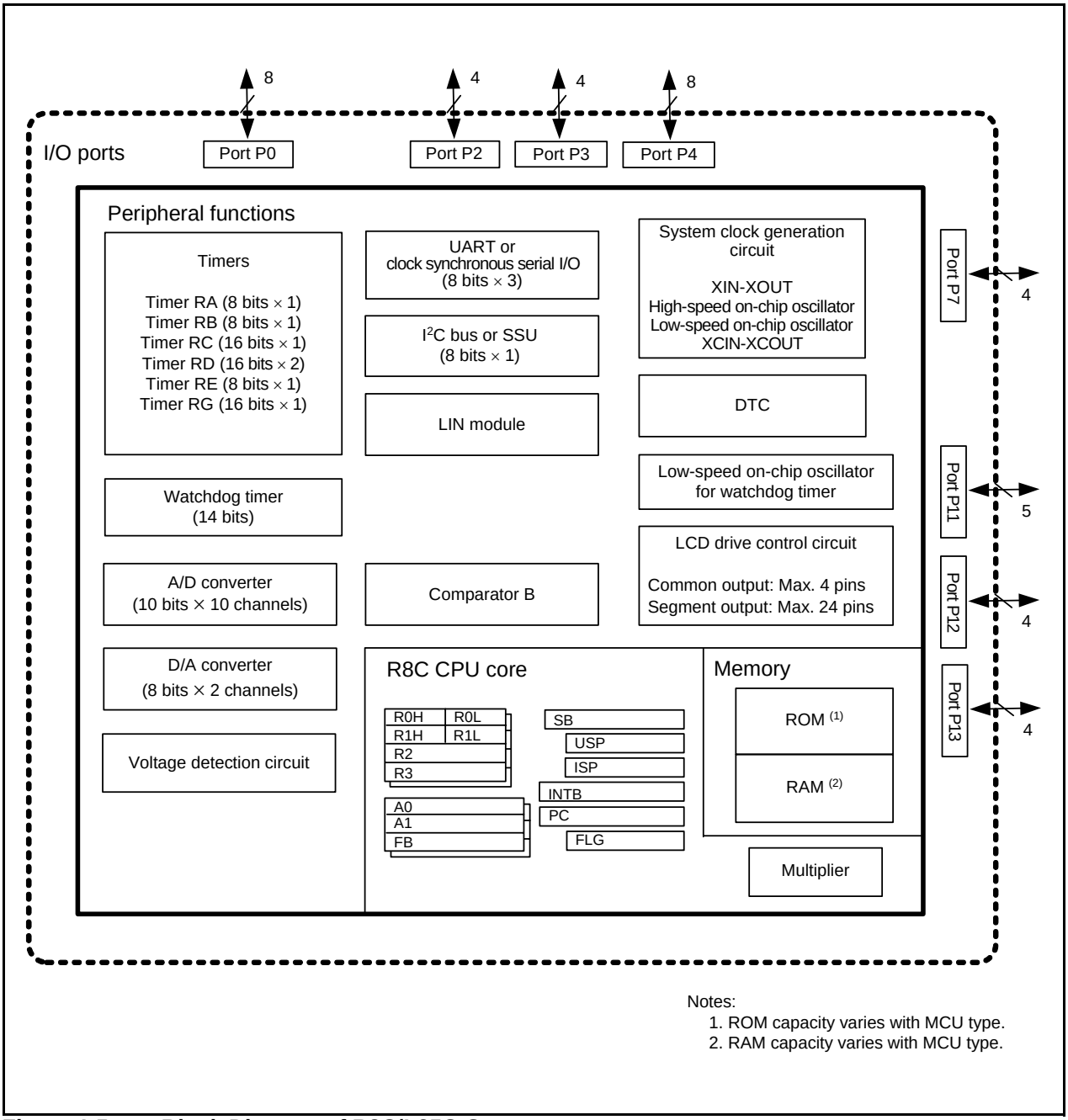
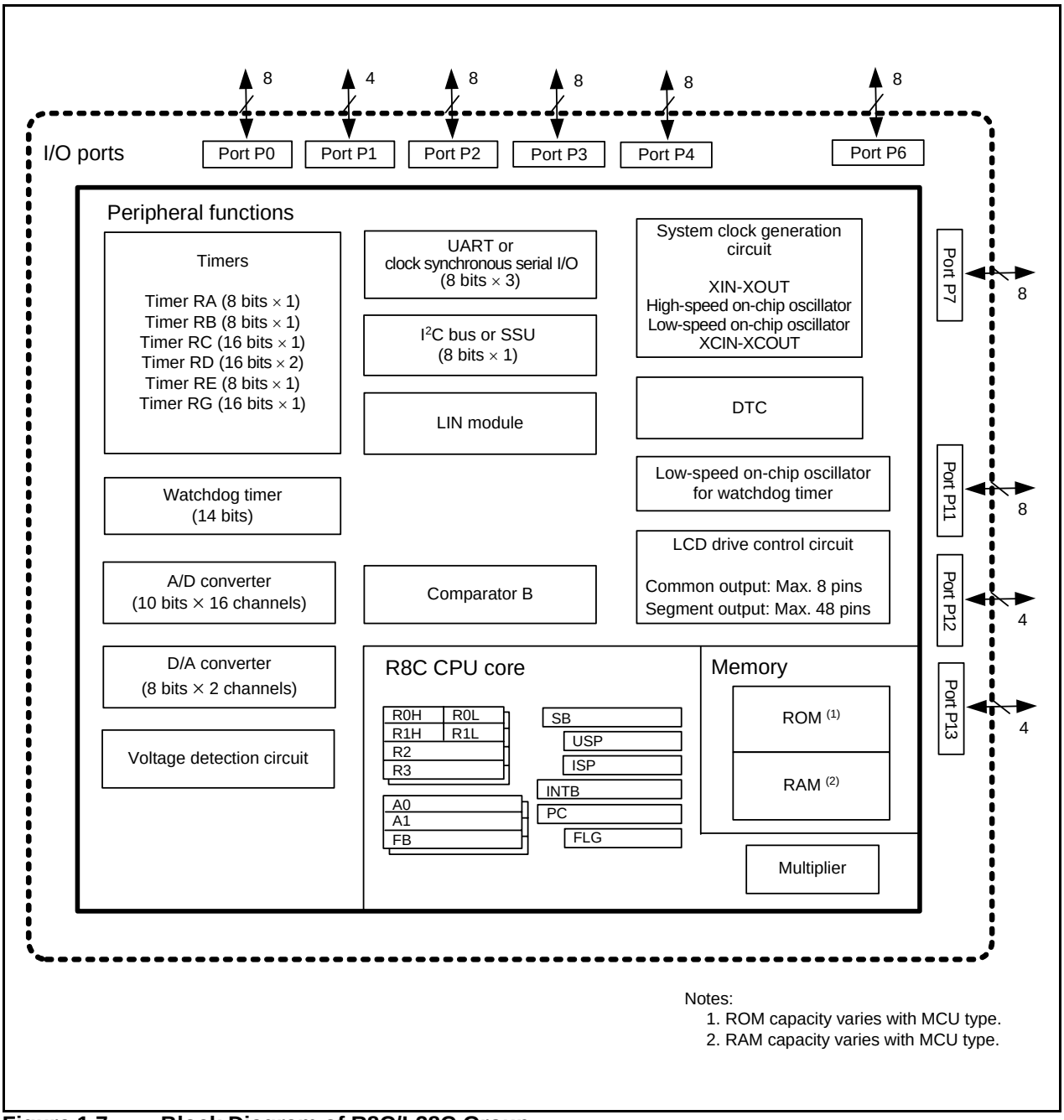
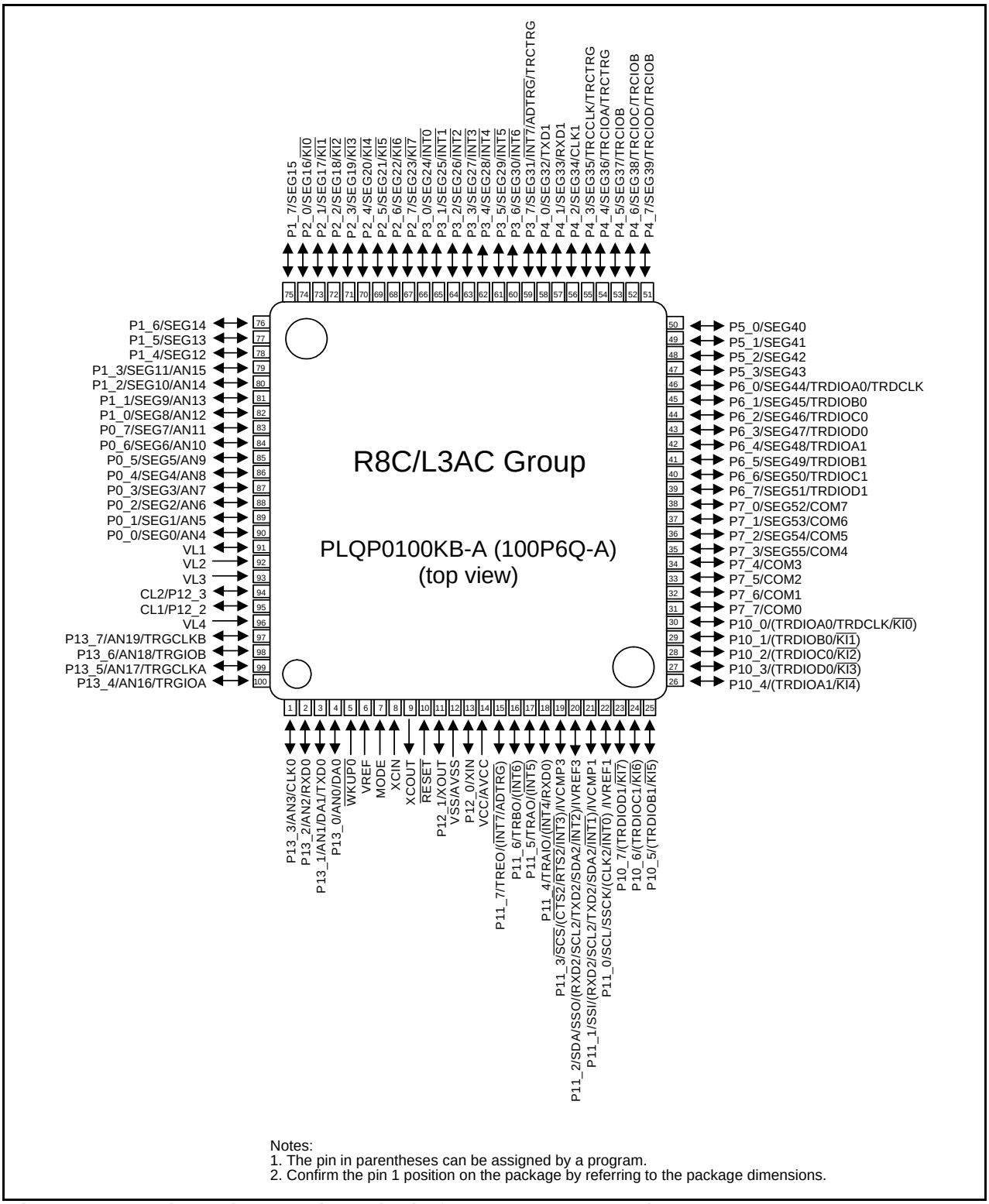


Figure 1.5 Block Diagram of R8C/L35C Group



Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.7 Block Diagram of R8C/L38C Group



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.12 Pin Assignment (Top View) of PLQP0100KB-A Package

Table 1.12 Pin Name Information by Pin Number (2)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
40 [42]	31				P6_6		TRDIOC1					SEG50
41 [43]	32				P6_5		TRDIOB1					SEG49
42 [44]	33				P6_4		TRDIOA1					SEG48
43 [45]	34				P6_3		TRDIOD0					SEG47
44 [46]	35				P6_2		TRDIOC0					SEG46
45 [47]	36				P6_1		TRDIOB0					SEG45
46 [48]	37				P6_0		TRDIOA0/ TRDCLK					SEG44
47 [49]					P5_3							SEG43
48 [50]					P5_2							SEG42
49 [51]					P5_1							SEG41
50 [52]					P5_0							SEG40
51 [53]	38	27	22		P4_7		TRCIOD/ TRCIOB					SEG39
52 [54]	39	28	23		P4_6		TRCIOC/ TRCIOB					SEG38
53 [55]	40	29	24		P4_5		TRCIOB					SEG37
54 [56]	41	30	25		P4_4		TRCIOA/ TRCTRG					SEG36
55 [57]	42	31	26		P4_3		TRCCLK/ TRCTRG					SEG35
56 [58]	43	32	27		P4_2			CLK1				SEG34
57 [59]	44	33	28		P4_1			RXD1				SEG33
58 [60]	45	34	29		P4_0			TXD1				SEG32
59 [61]	46	35			P3_7	$\overline{INT7}$	TRCTRG				$\overline{ADTRG}$	SEG31
60 [62]	47	36			P3_6	$\overline{INT6}$						SEG30
61 [63]	48	37			P3_5	$\overline{INT5}$						SEG29
62 [64]	49	38			P3_4	$\overline{INT4}$						SEG28
63 [65]	50	39	30		P3_3	$\overline{INT3}$						SEG27
64 [66]	51	40	31		P3_2	$\overline{INT2}$						SEG26
65 [67]	52	41	32		P3_1	$\overline{INT1}$						SEG25
66 [68]	53	42	33		P3_0	$\overline{INT0}$						SEG24
67 [69]	54	43	34		P2_7	$\overline{KI7}$						SEG23
68 [70]	55	44	35		P2_6	$\overline{KI6}$						SEG22
69 [71]	56	45	36		P2_5	$\overline{KI5}$						SEG21
70 [72]	57	46	37		P2_4	$\overline{KI4}$						SEG20
71 [73]	58				P2_3	$\overline{KI3}$						SEG19
72 [74]	59				P2_2	$\overline{KI2}$						SEG18
73 [75]	60				P2_1	$\overline{KI1}$						SEG17
74 [76]	61				P2_0	$\overline{KI0}$						SEG16
75 [77]					P1_7							SEG15
76 [78]					P1_6							SEG14
77 [79]					P1_5							SEG13
78 [80]					P1_4							SEG12
79 [81]	62				P1_3						AN15	SEG11
80 [82]	63				P1_2						AN14	SEG10
81 [83]	64				P1_1						AN13	SEG9
82 [84]	65				P1_0						AN12	SEG8
83 [85]	66	47	38		P0_7						AN11 (3)	SEG7
84 [86]	67	48	39		P0_6						AN10 (3)	SEG6

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.
3. Pins AN10 and AN11 are not available in the R8C/L35C, and R8C/L36C Groups.

1.5 Pin Functions

Tables 1.14 and 1.15 list Pin Functions for R8C/L3AC Group.

Table 1.14 Pin Functions for R8C/L3AC Group (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off mode exit input	$\overline{\text{WKUP0}}$	I	This pin is provided for input to exit the mode used in power-off mode. Connect to VSS when not using power-off mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Timer RG	TRGCLKA, TRGCLKB	I	Timer RG input pins
	TRGIOA, TRGIOB	I/O	Timer RG I/O pins
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A 0 Register	DA0	00h
00D9h	D/A 1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P10 Register	P10	XXh
00F5h	Port P11 Register	P11	XXh
00F6h	Port P10 Direction Register	PD10	00h
00F7h	Port P11 Direction Register	PD11	00h
00F8h	Port P12 Register	P12	XXh
00F9h	Port P13 Register	P13	XXh
00FAh	Port P12 Direction Register	PD12	00h
00FBh	Port P13 Direction Register	PD13	00h
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	00h
01E1h	Port P1 Pull-Up Control Register	P1PUR	00h
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h	Port P3 Pull-Up Control Register	P3PUR	00h
01E4h	Port P4 Pull-Up Control Register	P4PUR	00h
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h	Port P6 Pull-Up Control Register	P6PUR	00h
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h			
01E9h			
01EAh	Port 10 Pull-Up Control Register	P10PUR	00h
01EBh	Port 11 Pull-Up Control Register	P11PUR	00h
01ECh	Port 12 Pull-Up Control Register	P12PUR	00h
01EDh	Port 13 Pull-Up Control Register	P13PUR	00h
01EEh			
01EFh			
01F0h	Port P10 Drive Capacity Control Register	P10DRR	00h
01F1h	Port P11 Drive Capacity Control Register	P11DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
02C0h			
02C1h			
02C2h			
02C3h			
02C4h			
02C5h			
02C6h			
02C7h			
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h			
02E1h			
02E2h			
02E3h			
02E4h			
02E5h			
02E6h			
02E7h			
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh			
02FFh			

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.65	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		VL1		–0.3 to VL2	V
		VL2	R8C/L35C	VL1 to VL4	V
			R8C/L36C, R8C/L38C, R8C/L3AC	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		VL3 to 6.5	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.65	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		VL1		–0.3 to VL2 (2)	V
		VL2	R8C/L35C	VL1 to VL4	V
			R8C/L36C, R8C/L38C, R8C/L3AC	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		–0.3 to 6.5	V
		CL1, CL2		–0.3 to 6.5	V
		COM0 to COM7		–0.3 to VL4	V
		SEG0 to SEG55		–0.3 to VL4	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version) / –40 to 85 (D version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be VCC or below.

Table 5.6 Flash Memory (Program ROM) Characteristics
(V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (1)		1,000 (2)	—	—	times
—	Byte program time		—	80	500	µs
—	Block erase time		—	0.3	—	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	ms
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time (6)	Ambient temperature = 55°C	20	—	—	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7 Flash Memory (Data flash Block A to Block D) Characteristics (V_{CC} = 2.7 to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (1)		10,000 (2)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	ms
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		−20 (6)	—	85	°C
—	Data hold time (7)	Ambient temperature = 55 °C	20	—	—	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. −40°C for D version.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

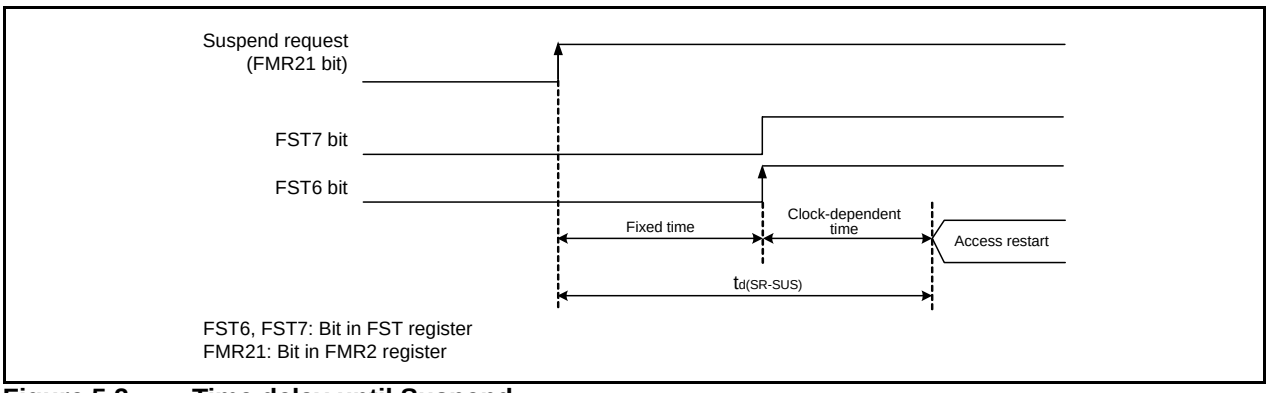


Figure 5.2 Time delay until Suspend

Table 5.19 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Port P10, P11 (1)	I_{OH} = –5 mA	V_{CC} – 0.5	—	V_{CC}	V
		Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	—	—	V
V_{OL}	Output “L” voltage	Port P10, P11 (1)	I_{OL} = 5 mA	—	—	0.5	V
		Other pins	I_{OL} = 1 mA	—	—	0.5	V
		XOUT	I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{INT5}$, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRGCLKA, TRGCLKB, $\overline{TRGIOA}$, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO		0.05	0.4	—	V
		$\overline{RESET}$, $\overline{WKUP0}$		0.1	0.8	—	V
I_{IH}	Input “H” current		VI = 3.0 V, V_{CC} = 3.0 V	—	—	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3.0 V	—	—	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3.0 V	30	100	170	kΩ
R_{fXIN}	Feedback resistance	XIN		—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN		—	14	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.21 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Port P10, P11 (1)	I_{OH} = –2 mA	V_{CC} – 0.5	—	V_{CC}	V
		Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	—	—	V
V_{OL}	Output “L” voltage	Port P10, P11 (1)	I_{OL} = 2 mA	—	—	0.5	V
		Other pins	I_{OL} = 1 mA	—	—	0.5	V
		XOUT	I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, INT7, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRGCLKA, TRGCLKB, $\overline{TRGIOA}$, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO		0.05	0.4	—	V
		$\overline{RESET}$, $\overline{WKUP0}$		0.1	0.8	—	V
I_{IH}	Input “H” current		VI = 1.8 V, V_{CC} = 1.8 V	—	—	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 1.8 V	—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 1.8 V	60	160	420	kΩ
R_{fXIN}	Feedback resistance	XIN		—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN		—	14	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.

5.5 AC Characteristics

Table 5.23 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (1)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (1)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1	t_{CYC} (1)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

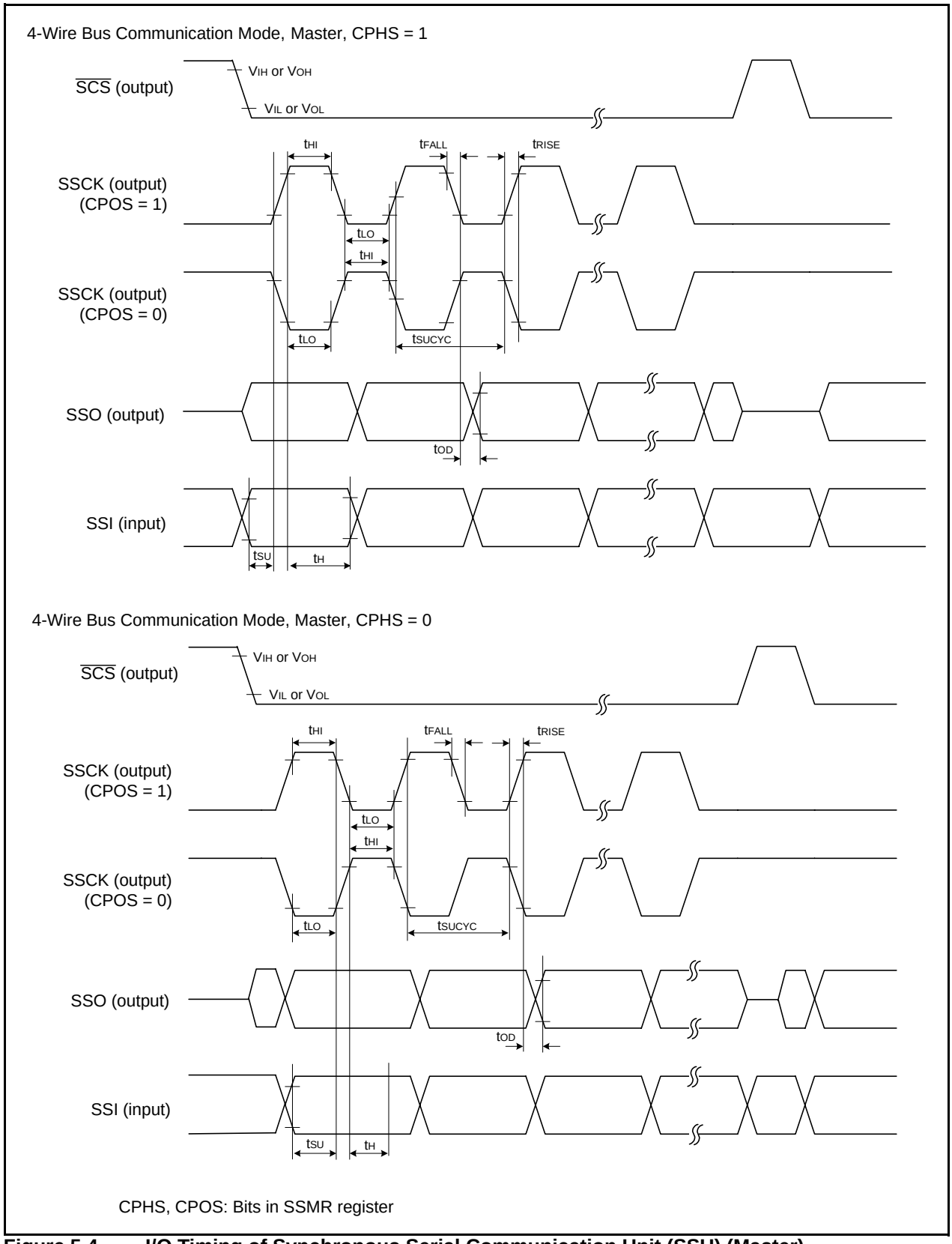
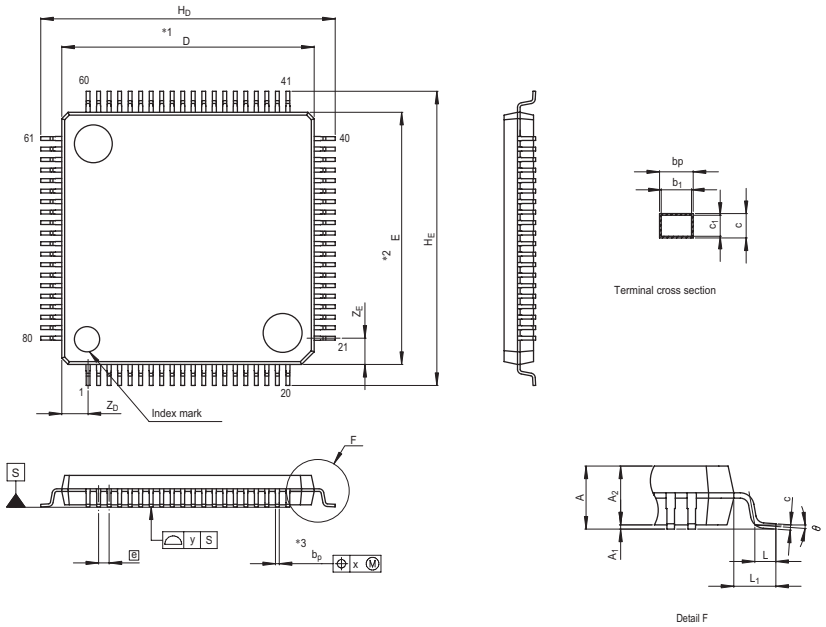


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

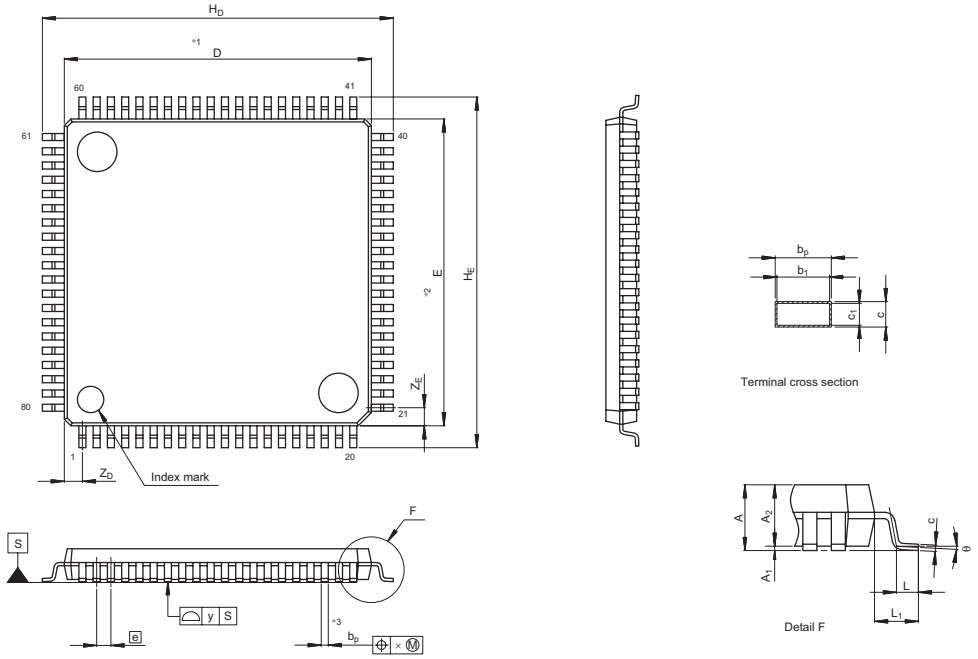
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

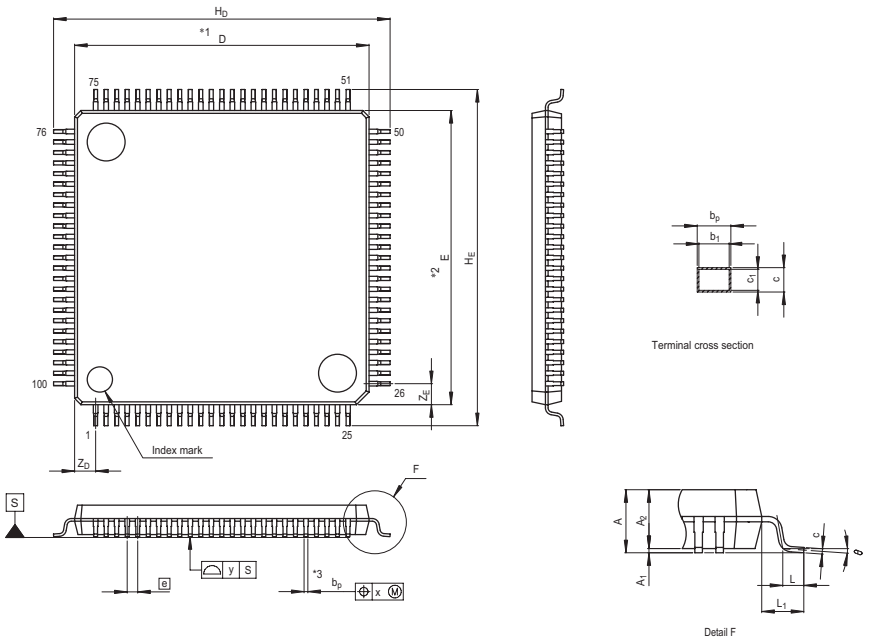
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

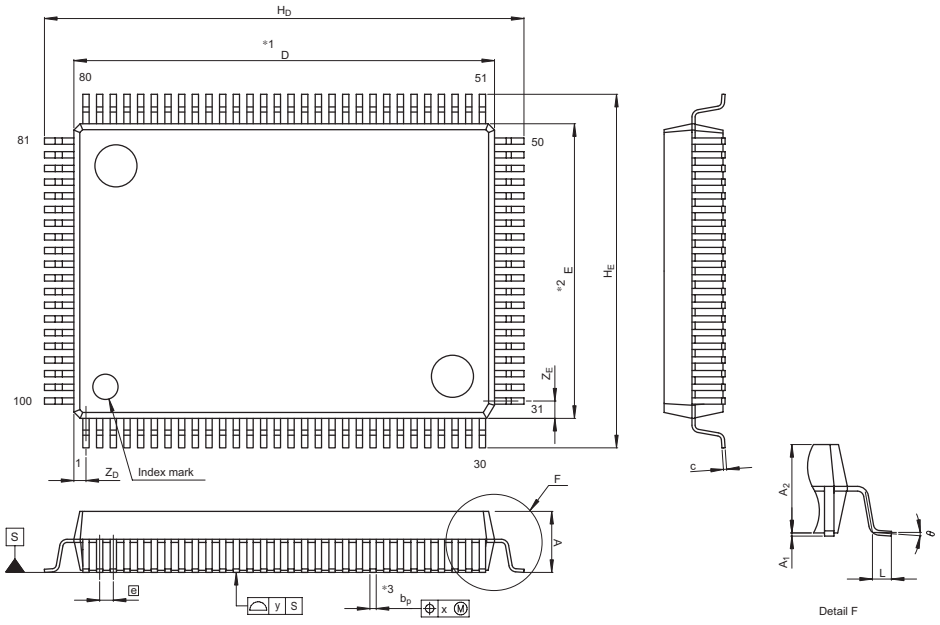
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.