Renesas Electronics America Inc - R5F2L38ACNFA#V0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	68
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l38acnfa-v0

Table 1.2 Programmable I/O Ports Provided for Each Group

Programmable I/O Port	R8C/L35C Group Total: 41 I/O pins								R8C/L36C Group Total: 52 I/O pins								R8C/L38C Group Total: 68 I/O pins								R8C/L3AC Group Total: 88 I/O pins							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	–	–	–	–	✓	✓	✓	✓	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P4	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P5	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	✓	✓	✓	✓
P6	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P7	✓	✓	✓	✓	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P10	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓
P11	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P12	–	–	–	–	✓	✓	✓	✓	–	–	–	–	✓	✓	✓	✓	–	–	–	–	✓	✓	✓	✓	–	–	–	–	✓	✓	✓	✓
P13	–	–	–	–	✓	✓	✓	✓	–	–	–	–	✓	✓	✓	✓	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes:
1. The symbol "✓" indicates a programmable I/O port.
2. The symbol "–" indicates the settings should be made as follows:
   - Set 1 to the corresponding bits in the PDi (i = 1 to 3, 5 to 7, and 10 to 13) register.
   - Set 0 to the corresponding bits in the Pi (i = 1 to 3, 5 to 7, and 10 to 13) register.
   - Set 0 to the corresponding bits in the P10DRR or P11DRR register.

Table 1.3 LCD Display Function Pins Provided for Each Group

Shared I/O Port	L35C Group Common output: Max. 4 Segment output: Max. 24								L36C Group Common output: Max. 8 Segment output: Max. 32								L38C Group Common output: Max. 8 Segment output: Max. 48								L3AC Group Common output: Max. 8 Segment output: Max. 56							
P0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SEG 11	SEG 10	SEG 9	SEG 8	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P2	SEG 23	SEG 22	SEG 21	SEG 20	–	–	–	–	SEG 23	SEG 22	SEG 21	SEG 20	–	–	–	–	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P3	–	–	–	–	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
P4	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
P5	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SEG 43	SEG 42	SEG 41	SEG 40
P6	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SEG 51	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44	SEG 51	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44
P7	COM 0	COM 1	COM 2	COM 3	–	–	–	–	COM 0	COM 1	COM 2	COM 3	SEG 55	SEG 54	SEG 53	SEG 52	COM 0	COM 1	COM 2	COM 3	SEG 55	SEG 54	SEG 53	SEG 52	COM 0	COM 1	COM 2	COM 3	SEG 55	SEG 54	SEG 53	SEG 52
P12	–	–	–	–	CL2	CL1	–	–	–	–	–	–	CL2	CL1	–	–	–	–	–	–	CL2	CL1	–	–	–	–	–	–	CL2	CL1	–	–
–	VL1								VL1								VL1								VL1							
–	VL2								VL2								VL2								VL2							
–	–								VL3								VL3								VL3							
–	VL4								VL4								VL4								VL4							

Notes:
1. The symbol "–" indicates there is no LCD display function. Set the corresponding bits in registers LSE1 to LSE3, LSE5 to LSE7 to 0 for these pins.
2. SEG52 to SEG55 can be used as COM7 to COM4.
   The R8C/L35C Group does not have pins SEG52 to SEG55, so 1/8 duty cannot be selected.
3. The R8C/L35C Group does not have the VL3 pin, so 1/4 bias cannot be selected. When the internal voltage multiplier is used, 1/2 bias cannot also be selected.

Table 1.9 Product List for R8C/L38C Group **Current of Apr 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L387CNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	N Version
R5F2L387CNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080JA-A	
R5F2L388CNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2L388CNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080JA-A	
R5F2L38ACNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38ACNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L38CCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38CCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L387CDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	D Version
R5F2L387CDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080JA-A	
R5F2L388CDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2L388CDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080JA-A	
R5F2L38ACDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38ACDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L38CCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38CCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	

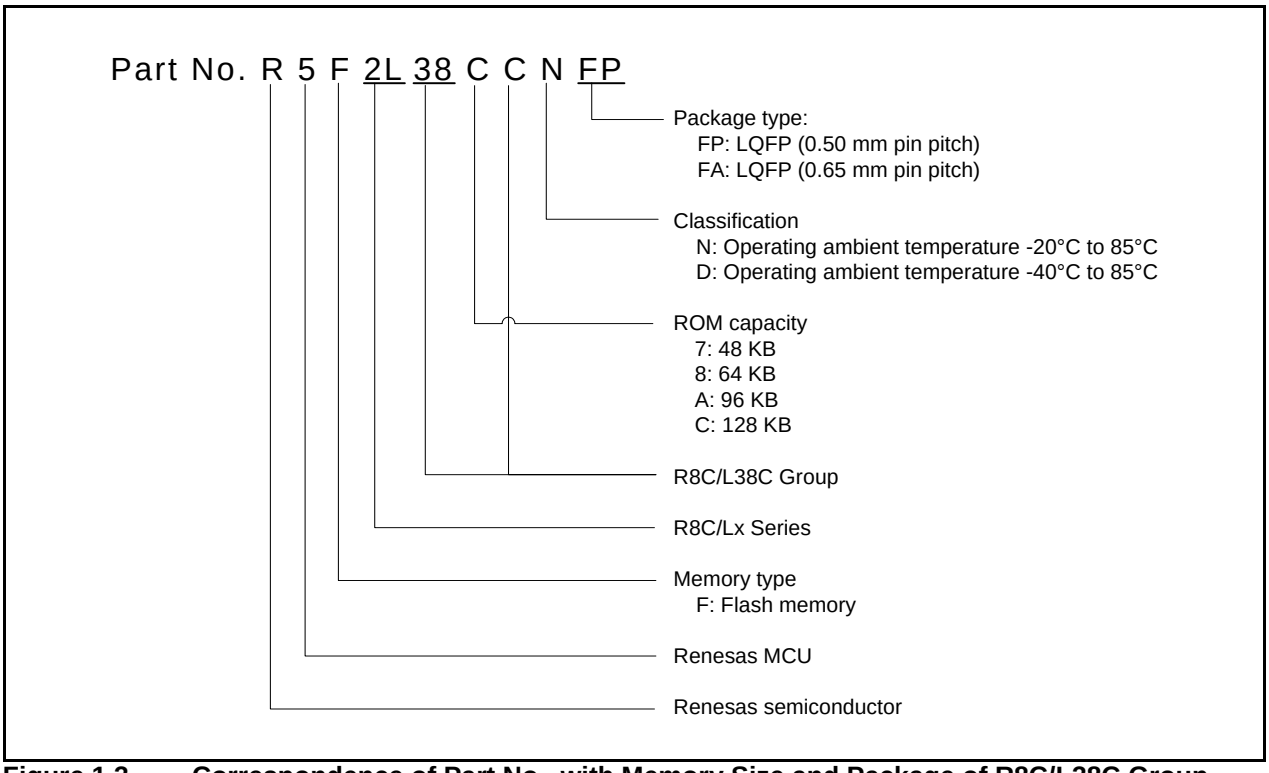
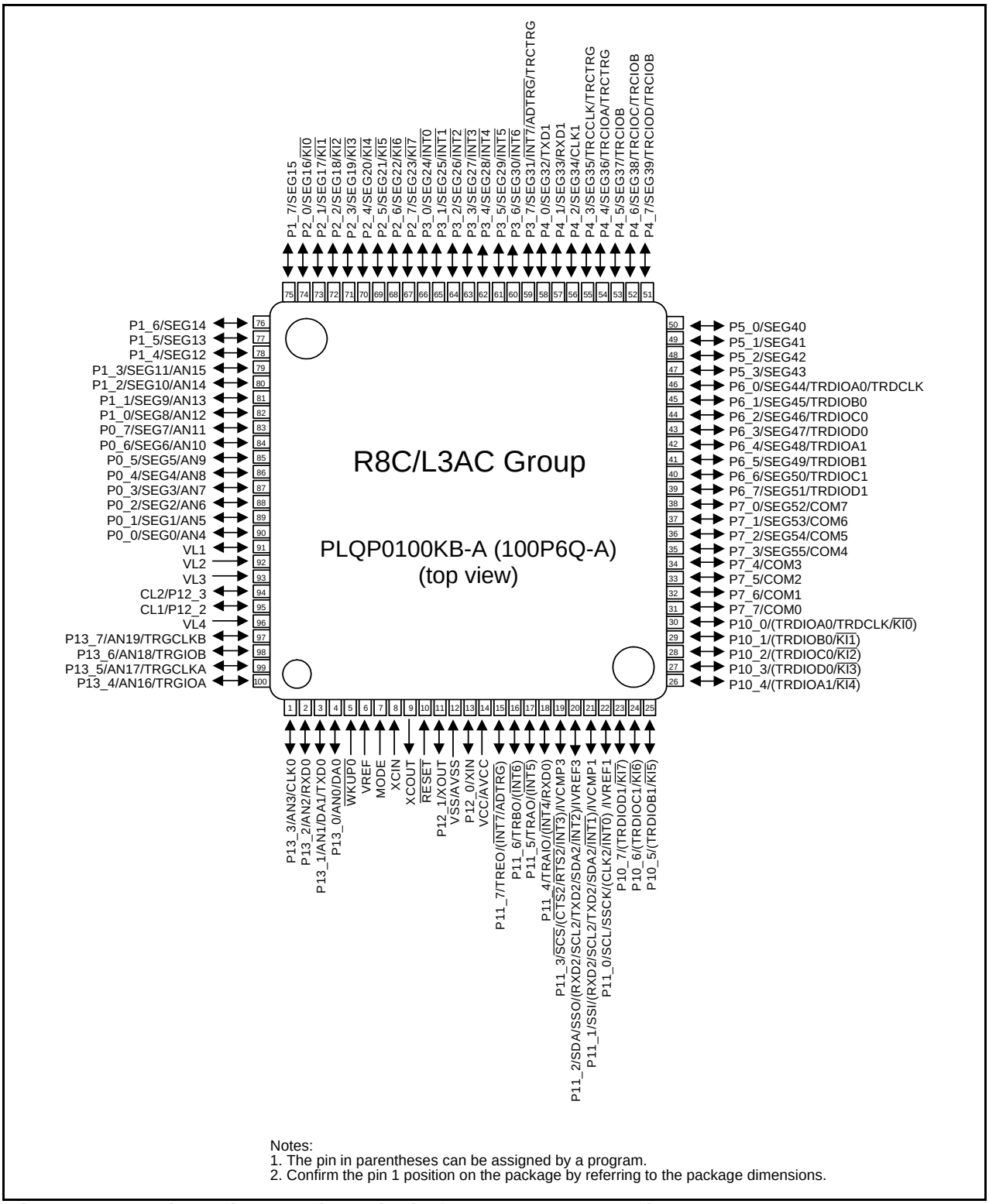
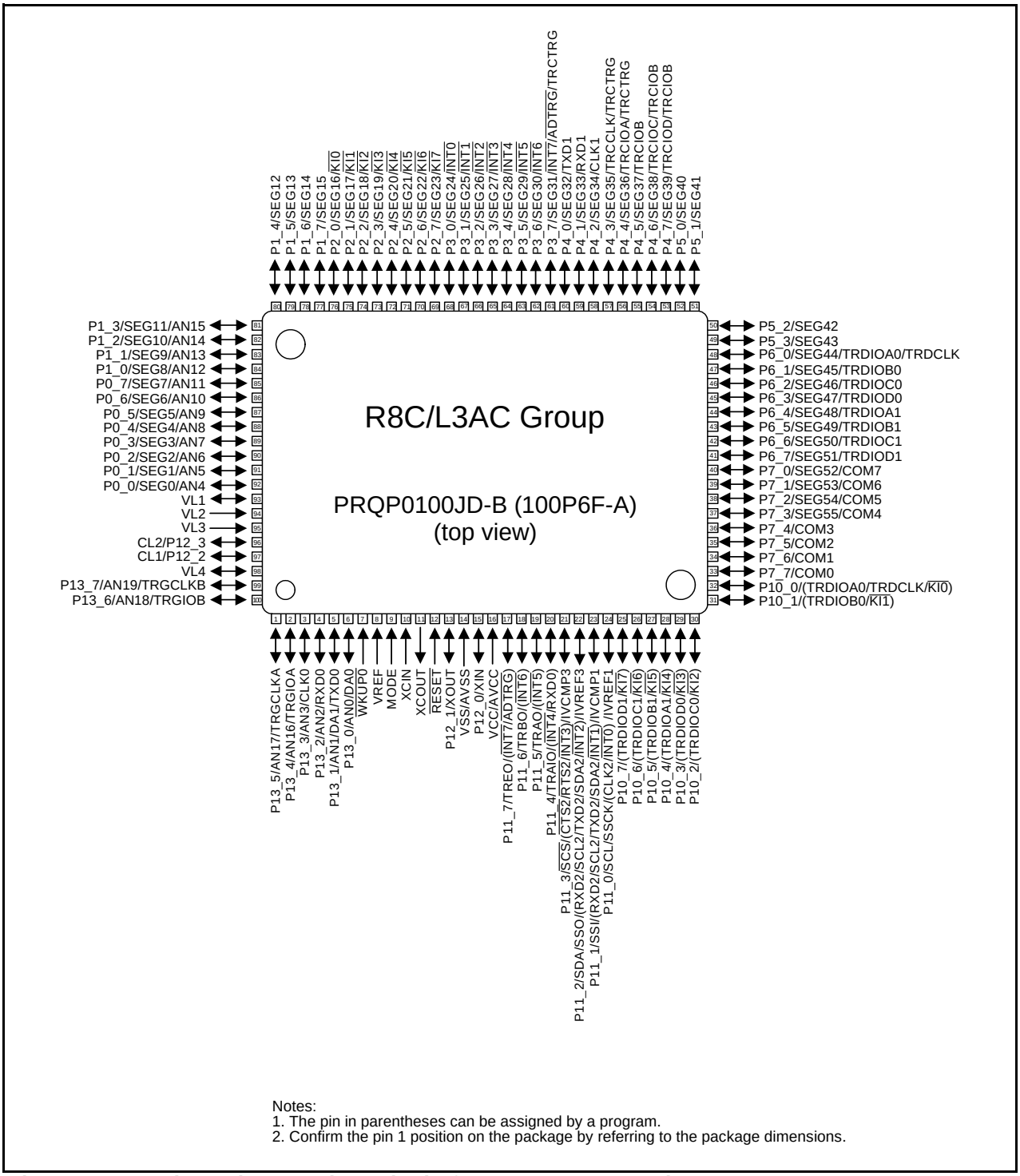


Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/L38C Group



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.12 Pin Assignment (Top View) of PLQP0100KB-A Package



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.13 Pin Assignment (Top View) of PRQP0100JD-B Package

Table 1.11 Pin Name Information by Pin Number (1)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
1 [3]	80	61	51		P13_3			CLK0			AN3	
2 [4]	1	62	52		P13_2			RXD0			AN2	
3 [5]	2	63	1		P13_1			TXD0			AN1/DA1	
4 [6]	3	64	2		P13_0						AN0/DA0	
5 [7]	4	1	3	$\overline{\text{WKUP0}}$								
6 [8]	5	2	4	VREF								
7 [9]	6	3	5	MODE								
8 [10]	7	4	6	XCIN								
9 [11]	8	5	7	XCOUT								
10 [12]	9	6	8	$\overline{\text{RESET}}$								
11 [13]	10	7	9	XOUT	P12_1							
12 [14]	11	8	10	VSS/ AVSS								
13 [15]	12	9	11	XIN	P12_0							
14 [16]	13	10	12	VCC/ AVCC								
15 [17]	14	11			P11_7	($\overline{\text{INT7}}$)	TREO				($\overline{\text{ADTRG}}$)	
16 [18]	15	12			P11_6	($\overline{\text{INT6}}$)	TRBO					
17 [19]	16	13			P11_5	($\overline{\text{INT5}}$)	TRAO					
18 [20]	17	14	13		P11_4	($\overline{\text{INT4}}$)	TRAIO	(RXD0)				
19 [21]	18	15	14		P11_3	($\overline{\text{INT3}}$)		($\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$)	$\overline{\text{SCS}}$		IVCMP3	
20 [22]	19	16	15		P11_2	($\overline{\text{INT2}}$)		(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	IVREF3	
21 [23]	20	17	16		P11_1	($\overline{\text{INT1}}$)		(RXD2/SCL2/ TXD2/SDA2)	SSI		IVCMP1	
22 [24]	21	18	17		P11_0	($\overline{\text{INT0}}$)		(CLK2)	SSCK	SCL	IVREF1	
23 [25]					P10_7	($\overline{\text{KI7}}$)	(TRDIOD1)					
24 [26]					P10_6	($\overline{\text{KI6}}$)	(TRDIOC1)					
25 [27]					P10_5	($\overline{\text{KI5}}$)	(TRDIOB1)					
26 [28]					P10_4	($\overline{\text{KI4}}$)	(TRDIOA1)					
27 [29]					P10_3	($\overline{\text{KI3}}$)	(TRDIOD0)					
28 [30]					P10_2	($\overline{\text{KI2}}$)	(TRDIOC0)					
29 [31]					P10_1	($\overline{\text{KI1}}$)	(TRDIOB0)					
30 [32]					P10_0	($\overline{\text{KI0}}$)	(TRDIOA0/ TRDCLK)					
31 [33]	22	19	18		P7_7							COM0
32 [34]	23	20	19		P7_6							COM1
33 [35]	24	21	20		P7_5							COM2
34 [36]	25	22	21		P7_4							COM3
35 [37]	26	23			P7_3							SEG55/ COM4
36 [38]	27	24			P7_2							SEG54/ COM5
37 [39]	28	25			P7_1							SEG53/ COM6
38 [40]	29	26			P7_0							SEG52/ COM7
39 [41]	30				P6_7		TRDIOD1					SEG51

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

Table 1.13 Pin Name Information by Pin Number (3)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
85 [87]	68	49	40		P0_5						AN9	SEG5
86 [88]	69	50	41		P0_4						AN8	SEG4
87 [89]	70	51	42		P0_3						AN7	SEG3
88 [90]	71	52	43		P0_2						AN6	SEG2
89 [91]	72	53	44		P0_1						AN5	SEG1
90 [92]	73	54	45		P0_0						AN4	SEG0
91 [93]	74	55	46									VL1
92 [94]	75	56	47									VL2
93 [95]	76	57										VL3
94 [96]	77	58	48		P12_3							CL2
95 [97]	78	59	49		P12_2							CL1
96 [98]	79	60	50									VL4
97 [99]					P13_7		TRGCLKB				AN19	
98 [100]					P13_6		TRGIOB				AN18	
99 [1]					P13_5		TRGCLKA				AN17	
100 [2]					P13_4		TRGIOA				AN16	

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

1.5 Pin Functions

Tables 1.14 and 1.15 list Pin Functions for R8C/L3AC Group.

Table 1.14 Pin Functions for R8C/L3AC Group (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off mode exit input	$\overline{\text{WKUP0}}$	I	This pin is provided for input to exit the mode used in power-off mode. Connect to VSS when not using power-off mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Timer RG	TRGCLKA, TRGCLKB	I	Timer RG input pins
	TRGIOA, TRGIOB	I/O	Timer RG I/O pins
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	01000000b
0171h	Timer RG Count Control Register	TRGCNTC	00h
0172h	Timer RG Control Register	TRGCR	10000000b
0173h	Timer RG Interrupt Enable Register	TRGIER	11110000b
0174h	Timer RG Status Register	TRGSR	11100000b
0175h	Timer RG I/O Control Register	TRGIOR	00h
0176h	Timer RG Counter	TRG	00h
0177h			00h
0178h	Timer RG General Register A	TRGGRA	FFh
0179h			FFh
017Ah	Timer RG General Register B	TRGGRB	FFh
017Bh			FFh
017Ch	Timer RG General Register C	TRGGRC	FFh
017Dh			FFh
017Eh	Timer RG General Register D	TRGGRD	FFh
017Fh			FFh

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h			
0187h	Timer RG Pin Select Register	TRGPSR	00h
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh	Key Input Pin Select Register	KISR	00h
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.17 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.65	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		VL1		–0.3 to VL2	V
		VL2	R8C/L35C	VL1 to VL4	V
			R8C/L36C, R8C/L38C, R8C/L3AC	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		VL3 to 6.5	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.65	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		VL1		–0.3 to VL2 (2)	V
		VL2	R8C/L35C	VL1 to VL4	V
			R8C/L36C, R8C/L38C, R8C/L3AC	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		–0.3 to 6.5	V
		CL1, CL2		–0.3 to 6.5	V
		COM0 to COM7		–0.3 to VL4	V
		SEG0 to SEG55		–0.3 to VL4	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version) / –40 to 85 (D version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be VCC or below.

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions
(Vcc = 1.8 to 5.5 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
Vcc/AVcc	Supply voltage					1.8	—	5.5	V
Vss/AVss	Supply voltage					—	0	—	V
VIH	Input “H” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0.8 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.8 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.9 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
VIL	Input “L” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.05 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)				—	—	−160	mA
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(avg)				—	—	−80	mA
IOH(peak)	Peak output “H” current	Port P10, P11 (2)				—	—	−40	mA
		Other pins				—	—	−10	mA
IOH(avg)	Average output “H” current (1)	Port P10, P11 (2)				—	—	−20	mA
		Other pins				—	—	−5	mA
IOL(sum)	Peak sum output “L” current	Sum of all pins IOL(peak)				—	—	160	mA
IOL(sum)	Average sum output “L” current	Sum of all pins IOL(avg)				—	—	80	mA
IOL(peak)	Peak output “L” current	Port P10, P11 (2)				—	—	40	mA
		Other pins				—	—	10	mA
IOL(avg)	Average output “L” current (1)	Port P10, P11 (2)				—	—	20	mA
		Other pins				—	—	5	mA
f(XIN)	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
f(XCIN)	XCIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 5.5 V	—	32.768	50	kHz
fOCO40M	When used as the count source for timer RC, timer RD, or timer RG (3)				2.7 V ≤ Vcc ≤ 5.5 V	32	—	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
—	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
f(BCLK)	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz

Notes:
1. The average output current indicates the average value of current measured during 100 ms.
2. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.
3. fOCO40M can be used as the count source for timer RC, timer RD, or timer RG in the range of Vcc = 2.7 V to 5.5V.

Table 5.12 High-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	VCC = 1.8 V to 5.5 V –20°C ≤ Topr ≤ 85°C	38.4	40	41.6	MHz
		VCC = 1.8 V to 5.5 V –40°C ≤ Topr ≤ 85°C	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (1)	VCC = 1.8 V to 5.5 V –20°C ≤ Topr ≤ 85°C	35.389	36.864	38.338	MHz
		VCC = 1.8 V to 5.5 V –40°C ≤ Topr ≤ 85°C	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	VCC = 1.8 V to 5.5 V –20°C ≤ Topr ≤ 85°C	30.72	32	33.28	MHz
		VCC = 1.8 V to 5.5 V –40°C ≤ Topr ≤ 85°C	30.40	32	33.60	MHz
—	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	—	0.5	3	ms
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	—	400	—	µA

Note:
1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.13 Low-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		112.5	125	137.5	kHz
—	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	—	30	100	µs
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	—	3	—	µA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
—	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	—	30	100	µs
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	—	2	—	µA

Table 5.14 Power Supply Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (1)		—	—	2000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.15 LCD Drive Control Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL4	2.2	—	5.5	V
VL3	VL3 voltage		VL2	—	VL4	V
VL2	VL2 voltage	R8C/L35C	VL1	—	VL4	V
		R8C/L36C, R8C/L38C, R8C/L3AC	VL1	—	VL3	V
VL1	VL1 voltage		1	—	VL2 (3)	V
—	VL1 internally-generated voltage accuracy (1)		Setting voltage –0.2	Setting voltage	Setting voltage +0.2	V
f(FR)	Frame frequency		50	—	180	Hz
ILCD	LCD drive control circuit current		—	(Note 2)	—	µA

Notes:
1. The voltage is selected with bits LVLS0 to LVLS3 in the LCR1 register.
2. Refer to **Table 5.18 DC Characteristics (2)**, **Table 5.20 DC Characteristics (4)**, and **Table 5.22 DC Characteristics (6)**.
3. The VL1 voltage should be VCC or below.

Table 5.16 Power-Off Mode Characteristics (VCC = 2.2 to 5.5 V, VSS = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Power-off mode operating supply voltage		2.2	—	5.5	V

Table 5.20 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	7.0	14.5	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	3.6	10	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—		—	3.0	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—		—	7.0	14.5	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	10 MHz	125 kHz	No division	—		—	4.0	—	mA
			Off	Off	10 MHz	125 kHz	Divide-by-8	—		—	1.7	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		—	85	390	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		—	90	400	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	—	50	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	—	5	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	5	—	µA
										LCD drive control circuit (5) When the internal voltage multiplier is used	—	11	—	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2	5.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off		—	13.0	—	µA
		Power-off mode	Off	Off	Off	Off	—	—	Topr = 25°C		—	0.02	0.2	µA
			Off	Off	Off	Off	—	—	Topr = 85°C		—	0.3	—	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 3.0 V
4. VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
5. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

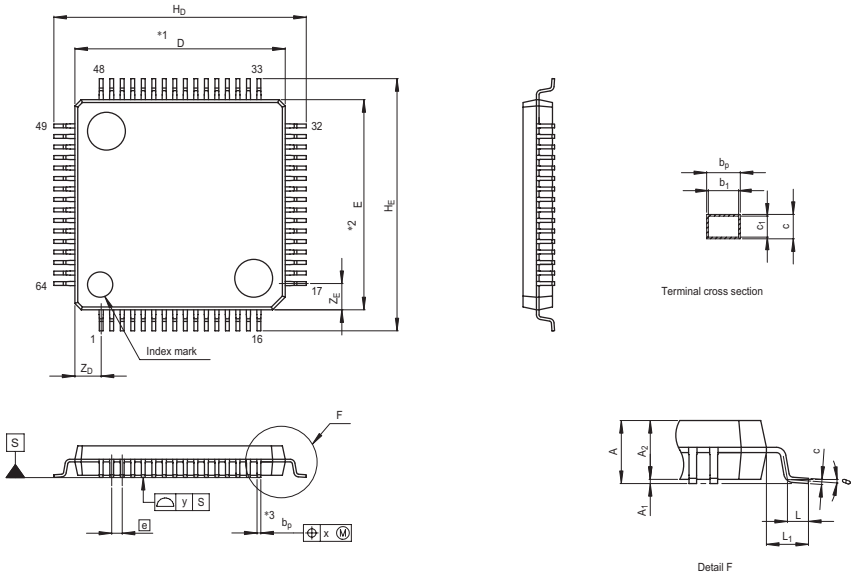
5.5 AC Characteristics

Table 5.23 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (1)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (1)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1	t_{CYC} (1)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

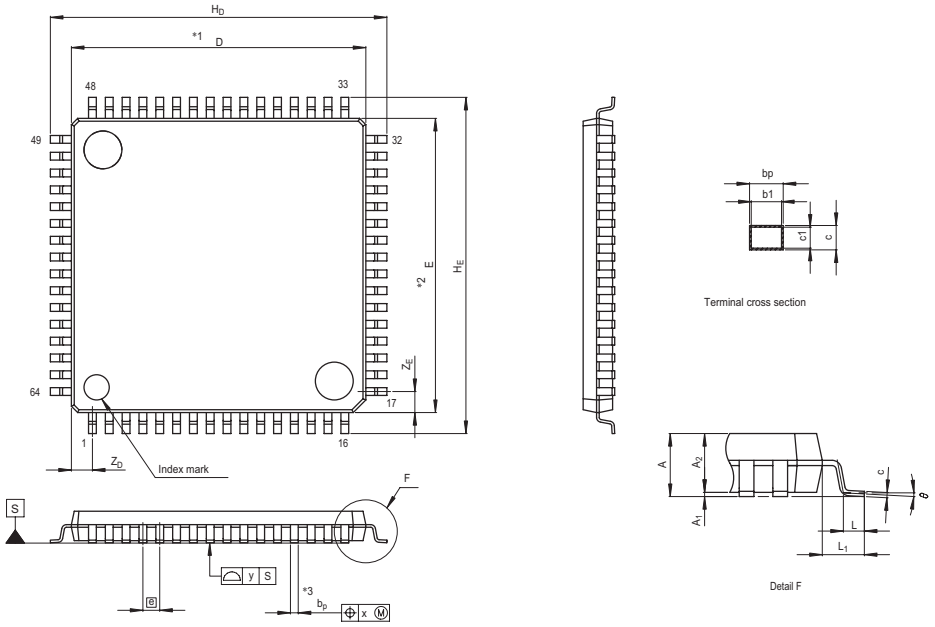
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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