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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	68
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l38acnfa-v1">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l38acnfa-v1</a>

### 1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Table 1.2 lists the Programmable I/O Ports Provided for Each Group, and Table 1.3 lists the LCD Display Function Pins Provided for Each Group. Figures 1.9 to 1.13 show the Pin Assignment for Each Group, and Tables 1.7 to 1.10 list Product Information.

The explanations in the chapters which follow apply to the R8C/L3AC Group only. Note the differences shown below.

**Table 1.1 Differences between Groups**

Item	Function	R8C/L35C Group	R8C/L36C Group	R8C/L38C Group	R8C/L3AC Group
I/O Ports	Programmable I/O ports	41 pins	52 pins	68 pins	88 pins
	High current drive ports	5 pins	8 pins	8 pins	16 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	8 pins	8 pins	8 pins
	Key input interrupt pins	4 pins	4 pins	8 pins	8 pins
Timer RA	Timer RA output pin	None	1 pin	1 pin	1 pin
Timer RB	Timer RB output pin	None	1 pin	1 pin	1 pin
Timer RD	Timer RD I/O pin	None	None	8 pins	8 pins
Timer RE	Timer RE output pin	None	1 pin	1 pin	1 pin
Timer RG	Timer RG I/O pin	None	None	None	2 pins
	Timer RG output pin	None	None	None	2 pins
A/D Converter	Analog input pin	10 pins	10 pins	16 pins	20 pins
LCD Drive Control Circuit	LCD power supply	3 pins (VL1, VL2, VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)
	Common output pins	Max. 4 pins	Max. 8 pins	Max. 8 pins	Max. 8 pins
	Segment output pins	Max. 24 pins	Max. 32 pins	Max. 48 pins	Max. 56 pins
Packages		52-pin LQFP	64-pin LQFP	80-pin LQFP	100-pin LQFP/ 100-pin QFP

Note:

1. I/O ports are shared with I/O functions, such as interrupts or timers.  
Refer to **Tables 1.11 to 1.13, Pin Name Information by Pin Number**, for details.

**Table 1.2 Programmable I/O Ports Provided for Each Group**

Programmable I/O Port	R8C/L35C Group Total: 41 I/O pins								R8C/L36C Group Total: 52 I/O pins								R8C/L38C Group Total: 68 I/O pins								R8C/L3AC Group Total: 88 I/O pins							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P2	✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P4	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P7	✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P10	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P11	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P12	—	—	—	—	✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓
P13	—	—	—	—	✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes:

- The symbol “✓” indicates a programmable I/O port.
- The symbol “—” indicates the settings should be made as follows:
  - Set 1 to the corresponding bits in the PDi (i = 1 to 3, 5 to 7, and 10 to 13) register.
  - Set 0 to the corresponding bits in the Pi (i = 1 to 3, 5 to 7, and 10 to 13) register.
  - Set 0 to the corresponding bits in the P10DRR or P11DRR register.

**Table 1.3 LCD Display Function Pins Provided for Each Group**

Shared I/O Port	L35C Group Common output: Max. 4 Segment output: Max. 24								L36C Group Common output: Max. 8 Segment output: Max. 32								L38C Group Common output: Max. 8 Segment output: Max. 48								L3AC Group Common output: Max. 8 Segment output: Max. 56							
P0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SEG 11	SEG 10	SEG 9	SEG 8	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P2	SEG 23	SEG 22	SEG 21	SEG 20	—	—	—	—	SEG 23	SEG 22	SEG 21	SEG 20	—	—	—	—	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P3	—	—	—	—	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
P4	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
P5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SEG 51	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44	SEG 51	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44
P7	COM 0	COM 1	COM 2	COM 3	—	—	—	—	COM 0	COM 1	COM 2	COM 3	SEG 55	SEG 54	SEG 53	SEG 52	COM 0	COM 1	COM 2	COM 3	SEG 55	SEG 54	SEG 53	SEG 52	COM 0	COM 1	COM 2	COM 3	SEG 55	SEG 54	SEG 53	SEG 52
P12	—	—	—	—	CL2	CL1	—	—	—	—	—	—	—	CL2	CL1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
—	VL1								VL1								VL1								VL1							
—	VL2								VL2								VL2								VL2							
—	—								VL3								VL3								VL3							
—	VL4								VL4								VL4								VL4							

Notes:

- The symbol “—” indicates there is no LCD display function. Set the corresponding bits in registers LSE1 to LSE3, LSE5 to LSE7 to 0 for these pins.
- SEG52 to SEG55 can be used as COM7 to COM4.  
The R8C/L35C Group does not have pins SEG52 to SEG55, so 1/8 duty cannot be selected.
- The R8C/L35C Group does not have the VL3 pin, so 1/4 bias cannot be selected. When the internal voltage multiplier is used, 1/2 bias cannot also be selected.

### 1.1.3 Specifications

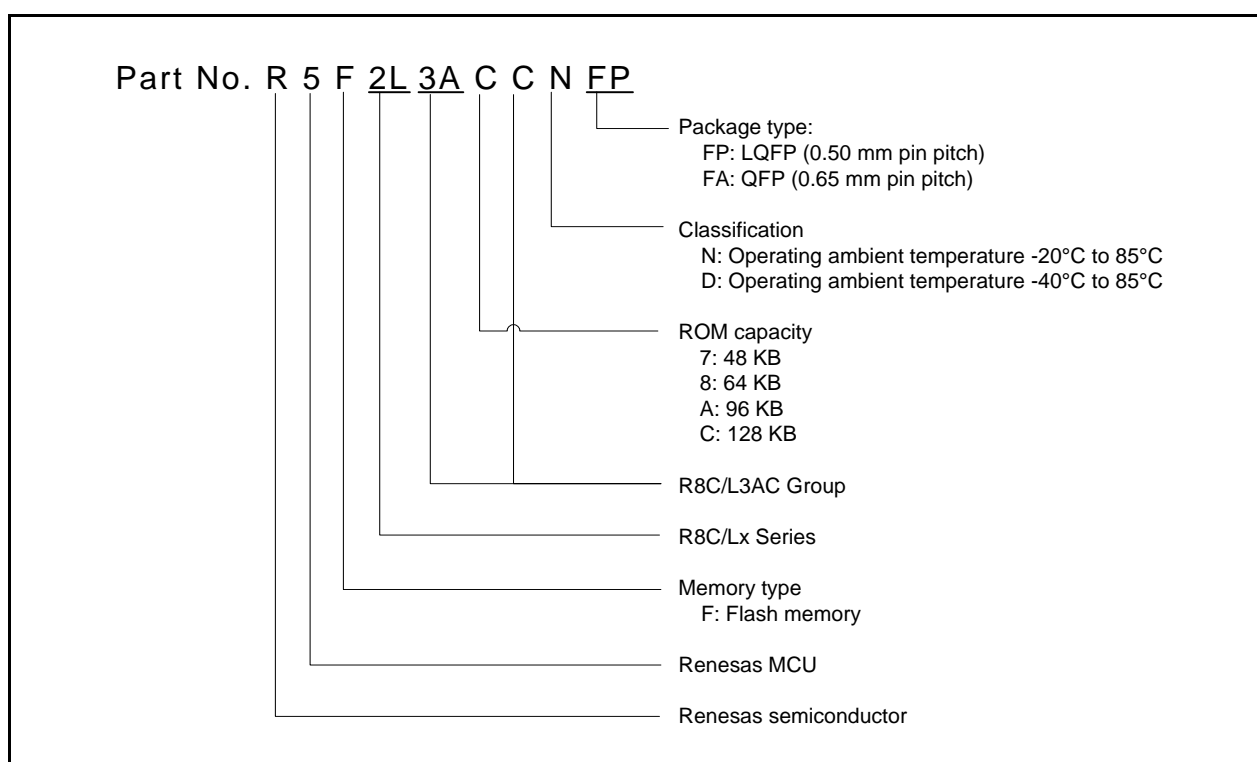
Tables 1.4 to 1.6 list the Specifications.

**Table 1.4 Specifications (1)**

Item	Function		Specification
CPU	Central processing unit		R8C CPU core <ul style="list-style-type: none"><li>• Number of fundamental instructions: 89</li><li>• Minimum instruction execution time:<ul style="list-style-type: none"><li>50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)</li><li>200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)</li></ul></li><li>• Multiplier: 16 bits × 16 bits → 32 bits</li><li>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits</li><li>• Operating mode: Single-chip mode (address space: 1 Mbyte)</li></ul>
Memory	ROM/RAM Data flash		Refer to <b>Tables 1.7 to 1.10 Product Lists</b> .
Power Supply Voltage Detection	Voltage detection circuit		<ul style="list-style-type: none"><li>• Power-on reset</li><li>• Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)</li></ul>
I/O Ports	Programmable I/O ports	R8C/L35C Group	<ul style="list-style-type: none"><li>• CMOS I/O ports: 41, selectable pull-up resistor</li><li>• High current drive ports: 5</li></ul>
		R8C/L36C Group	<ul style="list-style-type: none"><li>• CMOS I/O ports: 52, selectable pull-up resistor</li><li>• High current drive ports: 8</li></ul>
		R8C/L38C Group	<ul style="list-style-type: none"><li>• CMOS I/O ports: 68, selectable pull-up resistor</li><li>• High current drive ports: 8</li></ul>
		R8C/L3AC Group	<ul style="list-style-type: none"><li>• CMOS I/O ports: 88, selectable pull-up resistor</li><li>• High current drive ports: 16</li></ul>
Clock	Clock generation circuits		4 circuits: XIN clock oscillation circuit XCIN clock oscillation circuit (32 kHz) High-speed on-chip oscillator (with frequency adjustment function) Low-speed on-chip oscillator <ul style="list-style-type: none"><li>• Oscillation stop detection: XIN clock oscillation stop detection function</li><li>• Frequency divider circuit: Division ratio selectable from 1, 2, 4, 8, and 16</li><li>• Low-power-consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode</li></ul>
			Real-time clock (timer RE)
Interrupts		R8C/L35C Group	<ul style="list-style-type: none"><li>• Number of interrupt <u>vectors</u>: 69</li><li>• External Interrupt: 9 (INT × 5, key input × 4)</li><li>• Priority levels: 7 levels</li></ul>
		R8C/L36C Group	<ul style="list-style-type: none"><li>• Number of interrupt vectors: 69</li><li>• External Interrupt: 12 (INT × 8, key input × 4)</li><li>• Priority levels: 7 levels</li></ul>
		R8C/L38C Group	<ul style="list-style-type: none"><li>• Number of interrupt vectors: 69</li><li>• External Interrupt: 16 (INT × 8, key input × 8)</li><li>• Priority levels: 7 levels</li></ul>
		R8C/L3AC Group	<ul style="list-style-type: none"><li>• Number of interrupt vectors: 69</li><li>• External Interrupt: 16 (INT × 8, key input × 8)</li><li>• Priority levels: 7 levels</li></ul>
Watchdog Timer			<ul style="list-style-type: none"><li>• 14 bits × 1 (with prescaler)</li><li>• Selectable reset start function</li><li>• Selectable low-speed on-chip oscillator for watchdog timer</li></ul>
DTC (Data Transfer Controller)			<ul style="list-style-type: none"><li>• 1 channel</li><li>• Activation sources: 38</li><li>• Transfer modes: 2 (normal mode, repeat mode)</li></ul>

**Table 1.10 Product List for R8C/L3AC Group****Current of Apr 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L3A7CNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7CNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8CNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8CNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AACNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AACNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3A7CDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7CDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8CDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8CDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AACDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AACDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	

**Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/L3AC Group**

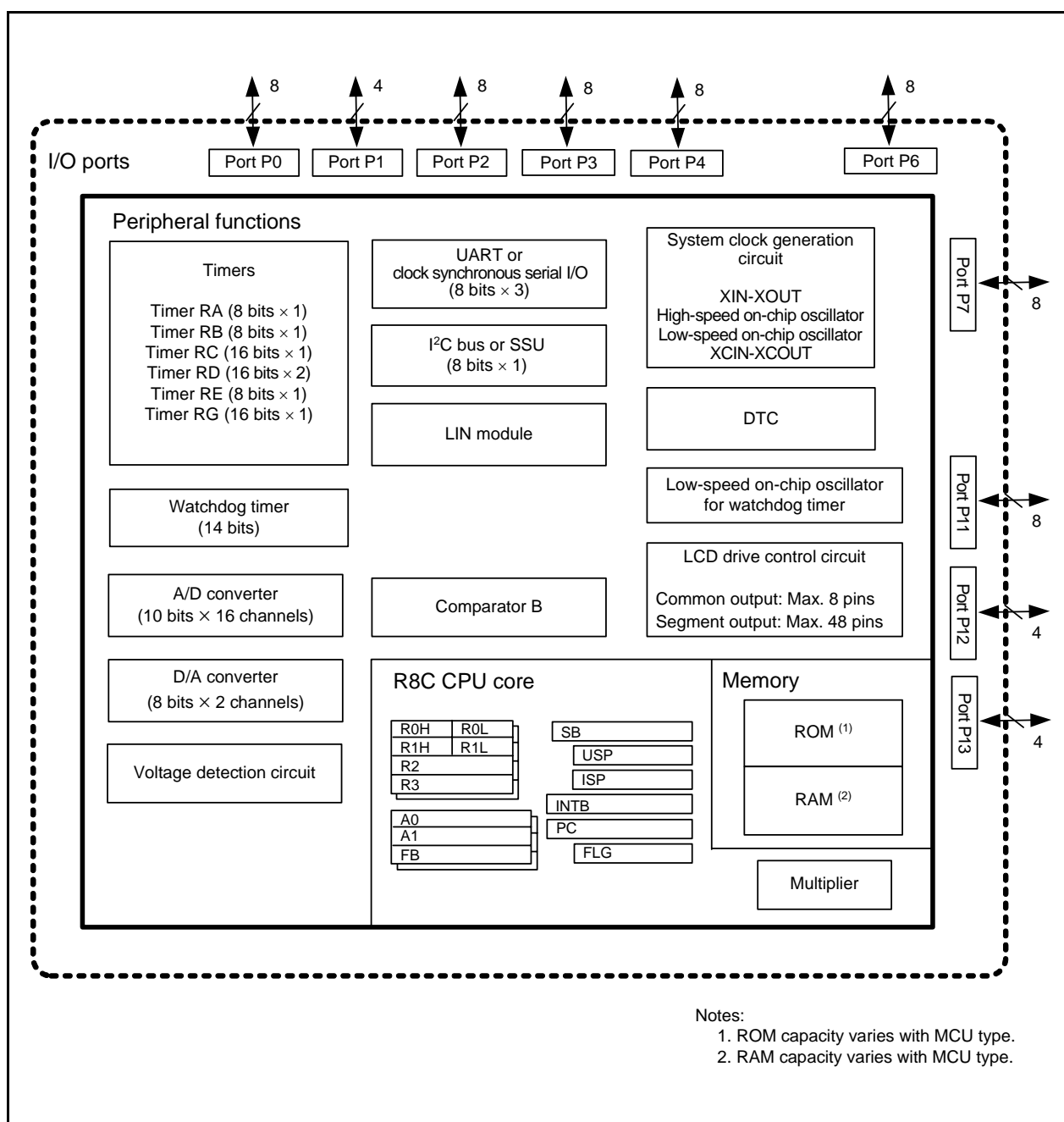


Figure 1.7 Block Diagram of R8C/L38C Group

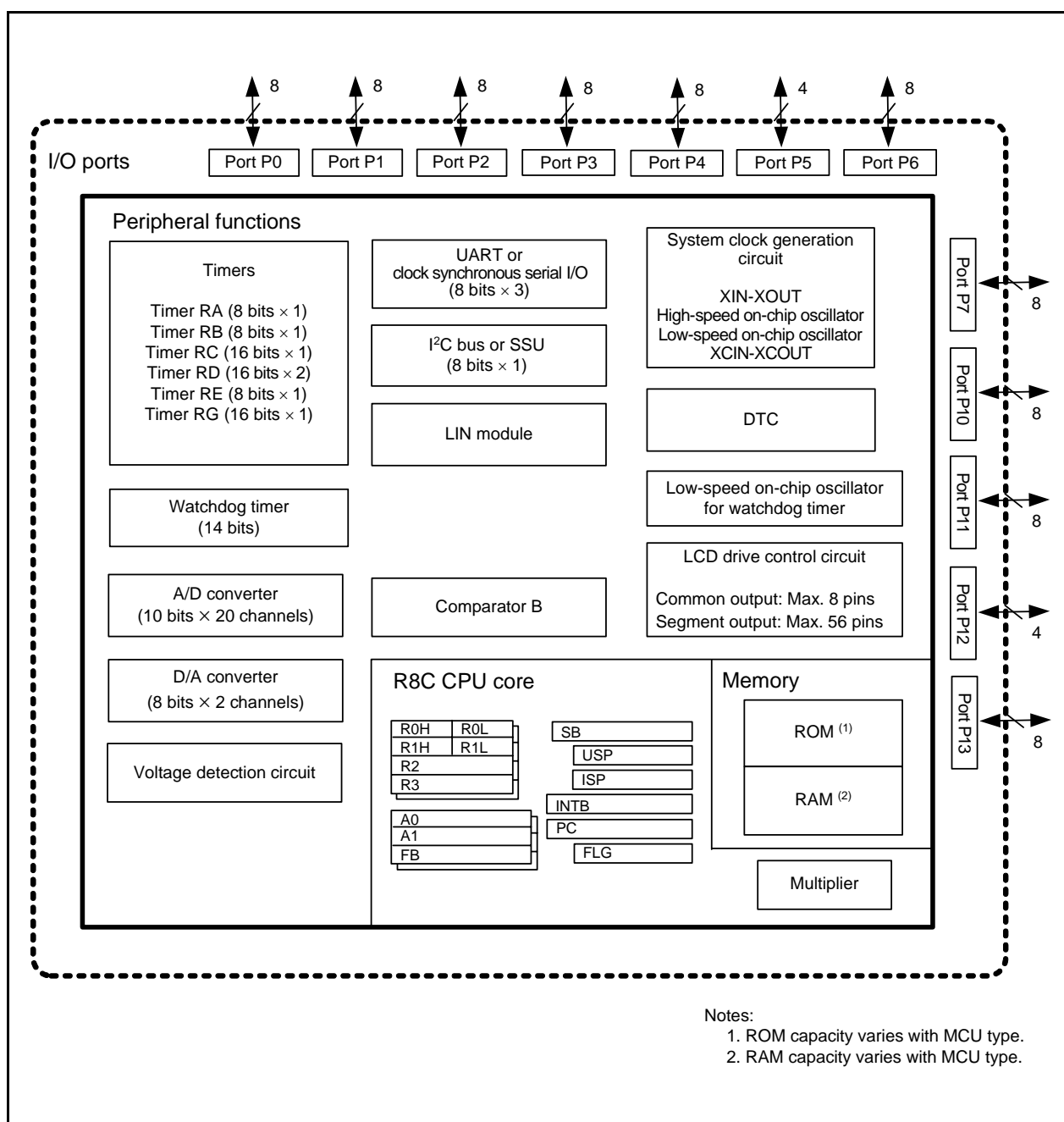


Figure 1.8 Block Diagram of R8C/L3AC Group

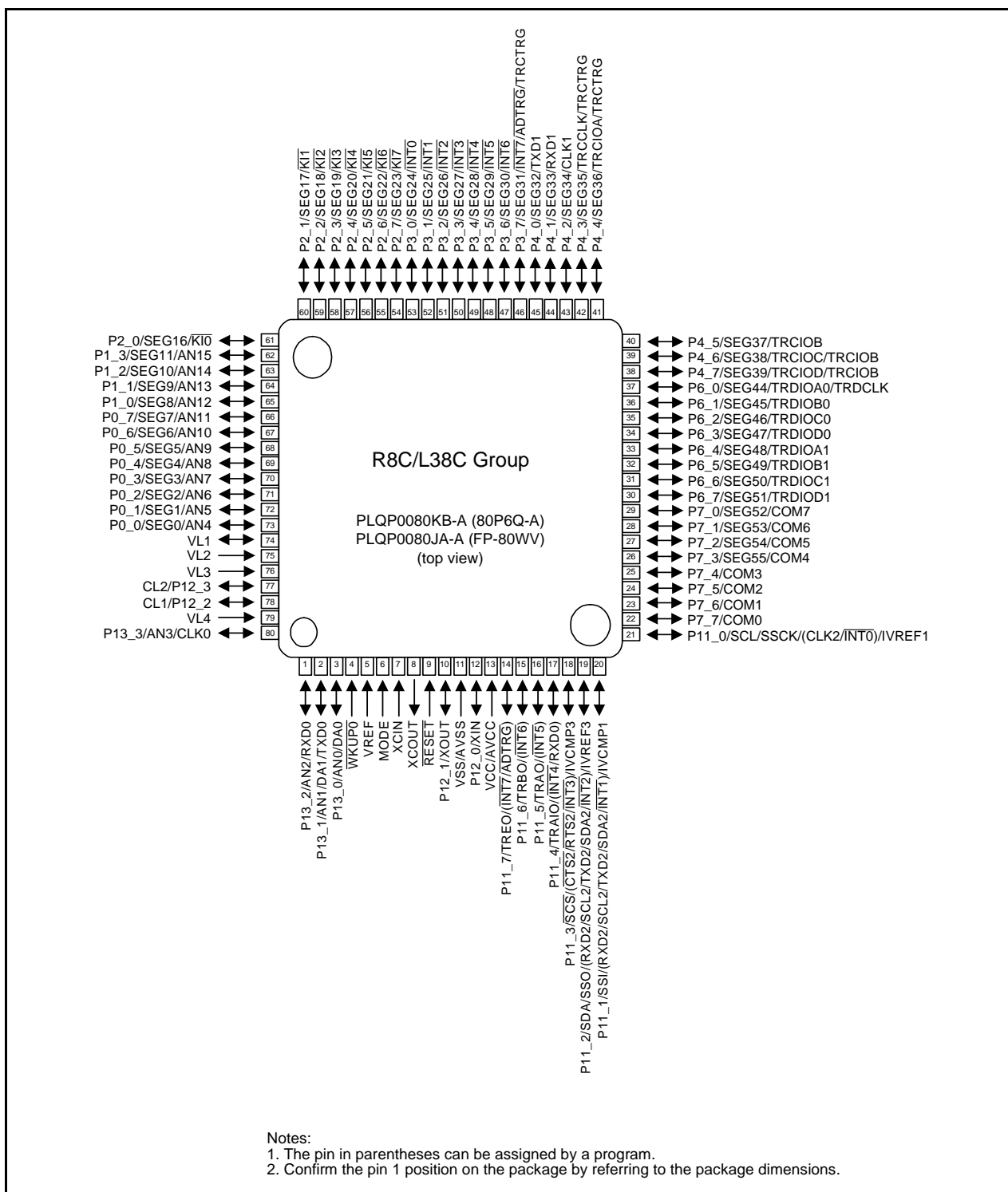


Figure 1.11 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages



**Table 1.13 Pin Name Information by Pin Number (3)**

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I <sup>2</sup> C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
85 [87]	68	49	40		P0_5						AN9	SEG5
86 [88]	69	50	41		P0_4						AN8	SEG4
87 [89]	70	51	42		P0_3						AN7	SEG3
88 [90]	71	52	43		P0_2						AN6	SEG2
89 [91]	72	53	44		P0_1						AN5	SEG1
90 [92]	73	54	45		P0_0						AN4	SEG0
91 [93]	74	55	46									VL1
92 [94]	75	56	47									VL2
93 [95]	76	57										VL3
94 [96]	77	58	48		P12_3							CL2
95 [97]	78	59	49		P12_2							CL1
96 [98]	79	60	50									VL4
97 [99]					P13_7		TRGCLKB				AN19	
98 [100]					P13_6		TRGIOB				AN18	
99 [1]					P13_5		TRGCLKA				AN17	
100 [2]					P13_4		TRGIOA				AN16	

Notes:

1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

**Table 1.15 Pin Functions for R8C/L3AC Group (2)**

Item	Pin Name	I/O Type	Description
I <sup>2</sup> C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter and the D/A converter
A/D converter	AN0 to AN11	I	A/D converter analog input pins
	$\overline{\text{ADTRG}}$	I	A/D external trigger input pin
D/A converter	DA0, DA1	O	D/A converter output pins
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0, P5_3, P6_0 to P6_7, P7_0 to P7_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_3, P13_0 to P13_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Ports P10_0 to P10_7 and P11_0 to P11_7 can be used as LED drive ports.
Segment output	SEG0 to SEG55	O	LCD segment output pins
Common output	COM0 to COM7	O	LCD common output pins
Voltage multiplier capacity connect pins	CL1, CL2	O	Connect pins for the LCD control voltage multiplier
LCD power supply	VL1	I/O	Apply the voltage: $0 \leq \text{VL1} \leq \text{VL2} \leq \text{VL3} \leq \text{VL4}$ .
	VL2 to VL4	I	VL1 can be used as the reference potential input or output pin when setting the voltage multiplier.

I: Input      O: Output      I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

### **2.8.7 Interrupt Enable Flag (I)**

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### **2.8.8 Stack Pointer Select Flag (U)**

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### **2.8.9 Processor Interrupt Priority Level (IPL)**

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### **2.8.10 Reserved Bit**

If necessary, set to 0. When read, the content is undefined.

**Table 4.4 SFR Information (4) (1)**

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A 0 Register	DA0	00h
00D9h	D/A 1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P10 Register	P10	XXh
00F5h	Port P11 Register	P11	XXh
00F6h	Port P10 Direction Register	PD10	00h
00F7h	Port P11 Direction Register	PD11	00h
00F8h	Port P12 Register	P12	XXh
00F9h	Port P13 Register	P13	XXh
00FAh	Port P12 Direction Register	PD12	00h
00FBh	Port P13 Direction Register	PD13	00h
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.9 SFR Information (9) <sup>(1)</sup>**

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h	LCD Bias Control Register	LCR1	00h
0202h	LCD Display Control Register	LCR2	X0000000b
0203h	LCD Clock Control Register	LCR3	00h
0204h			
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h	LCD Port Select Register 3	LSE3	00h
020Ah	LCD Port Select Register 4	LSE4	00h
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch	LCD Port Select Register 6	LSE6	00h
020Dh	LCD Port Select Register 7	LSE7	00h
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh		LRA27L	XXh
022Ch		LRA28L	XXh
022Dh		LRA29L	XXh
022Eh		LRA30L	XXh
022Fh		LRA31L	XXh
0230h		LRA32L	XXh
0231h		LRA33L	XXh
0232h		LRA34L	XXh
0233h		LRA35L	XXh
0234h		LRA36L	XXh
0235h		LRA37L	XXh
0236h		LRA38L	XXh
0237h		LRA39L	XXh
0238h		LRA40L	XXh
0239h		LRA41L	XXh
023Ah		LRA42L	XXh
023Bh		LRA43L	XXh
023Ch		LRA44L	XXh
023Dh		LRA45L	XXh
023Eh		LRA46L	XXh
023Fh		LRA47L	XXh

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.15 SFR Information (15) (1)**

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

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## 5. Electrical Characteristics

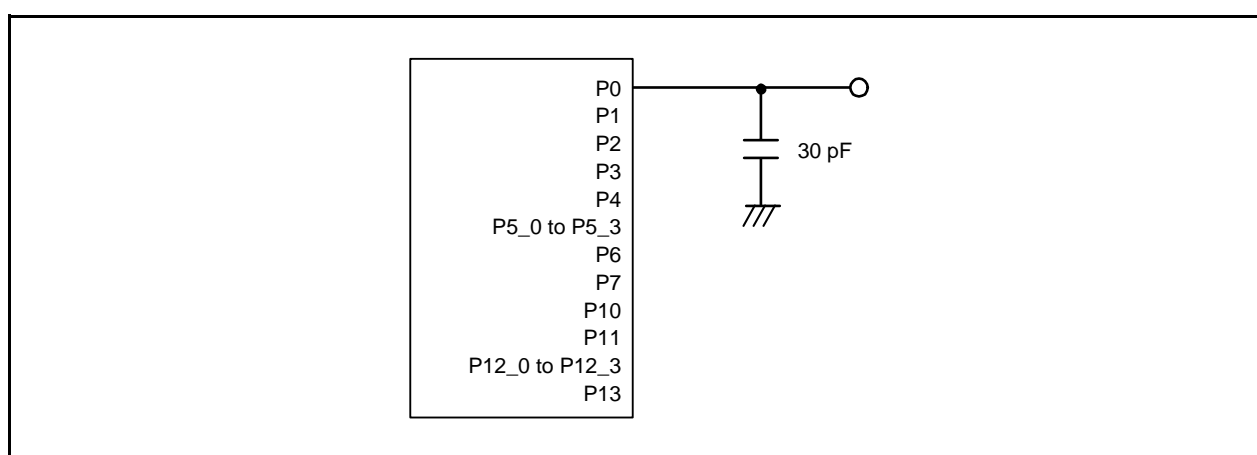
### 5.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Ratings**

Symbol	Parameter		Condition	Rated Value	Unit
V <sub>cc</sub> /AV <sub>cc</sub>	Supply voltage			−0.3 to 6.5	V
V <sub>i</sub>	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>	−0.3 to 1.65	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup>	−0.3 to V <sub>cc</sub> + 0.3	V
		VL1		−0.3 to VL2	V
		VL2	R8C/L35C	VL1 to VL4	V
			R8C/L36C, R8C/L38C, R8C/L3AC	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		VL3 to 6.5	V
		Other pins		−0.3 to V <sub>cc</sub> + 0.3	V
V <sub>o</sub>	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>	−0.3 to 1.65	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup>	−0.3 to V <sub>cc</sub> + 0.3	V
		VL1		−0.3 to VL2 <sup>(2)</sup>	V
		VL2	R8C/L35C	VL1 to VL4	V
			R8C/L36C, R8C/L38C, R8C/L3AC	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		−0.3 to 6.5	V
		CL1, CL2		−0.3 to 6.5	V
		COM0 to COM7		−0.3 to VL4	V
		SEG0 to SEG55		−0.3 to VL4	V
		Other pins		−0.3 to V <sub>cc</sub> + 0.3	V
P <sub>d</sub>	Power dissipation		−40°C ≤ T <sub>opr</sub> ≤ 85°C	500	mW
T <sub>opr</sub>	Operating ambient temperature			−20 to 85 (N version) / −40 to 85 (D version)	°C
T <sub>stg</sub>	Storage temperature			−65 to 150	°C

Notes:

- For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
- The VL1 voltage should be VCC or below.



**Figure 5.1** Ports P0 to P4, P5\_0 to P5\_3, P6, P7, P10, P11, P12\_0 to P12\_3, and P13 Timing Measurement Circuit



**Table 5.4 D/A Converter Characteristics**  
**( $V_{CC}/AV_{CC} = V_{ref} = 2.7$  to  $5.5$  V and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version) /  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
$t_{su}$	Setup time		—	—	3	$\mu\text{s}$
$R_o$	Output resistor		—	6	—	$\text{k}\Omega$
$I_{vref}$	Reference power input current	(Note 1)	—	—	1.5	mA

Note:

1. This applies when one D/A converter is used and the value of the DAI register ( $i = 0$  or  $1$ ) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

**Table 5.5 Comparator B Characteristics**  
**( $V_{CC} = 2.7$  to  $5.5$  V and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version) /  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$V_{ref}$	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
$V_i$	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
$t_d$	Comparator output delay time <sup>(1)</sup>	$V_i = V_{ref} \pm 100$ mV	—	0.1	—	$\mu\text{s}$
$I_{CMP}$	Comparator operating current	$V_{CC} = 5.0$ V	—	17.5	—	$\mu\text{A}$

Note:

1. When the digital filter is disabled.

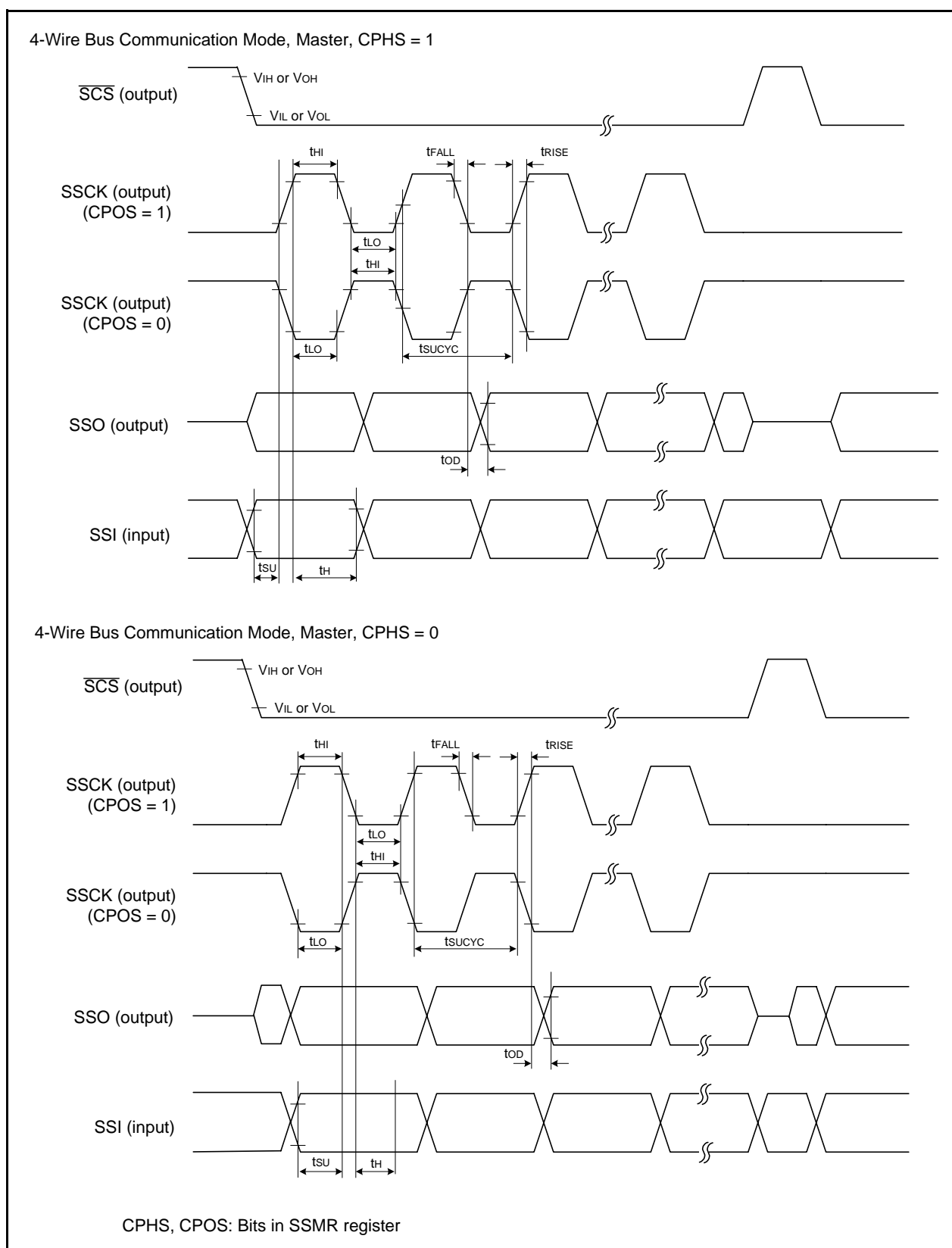
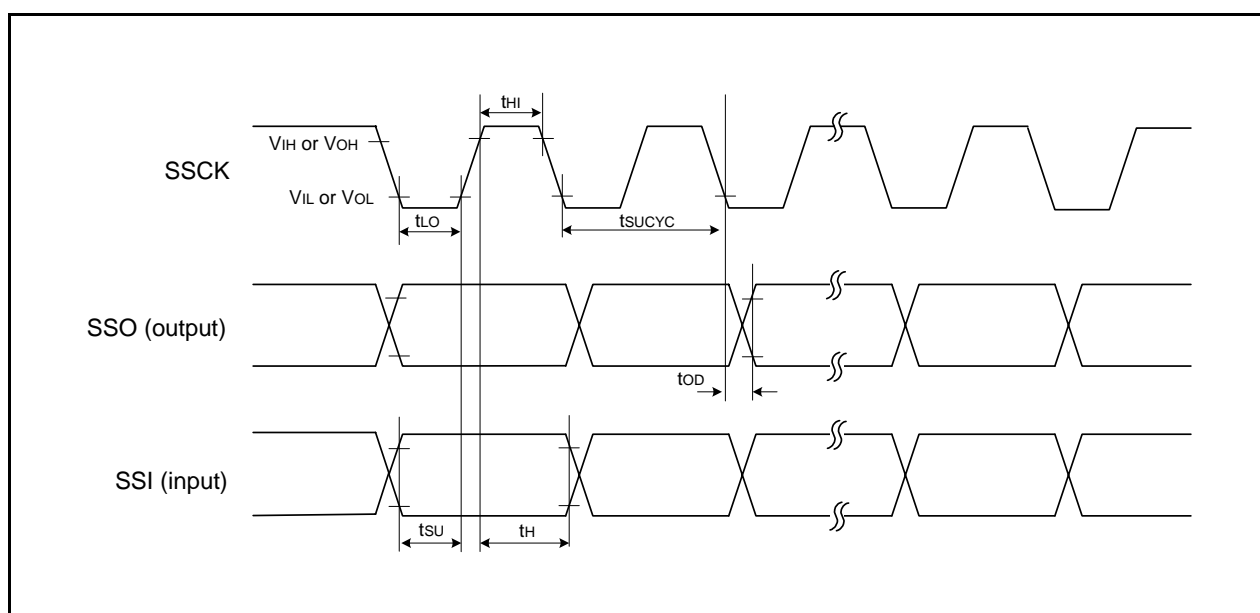


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

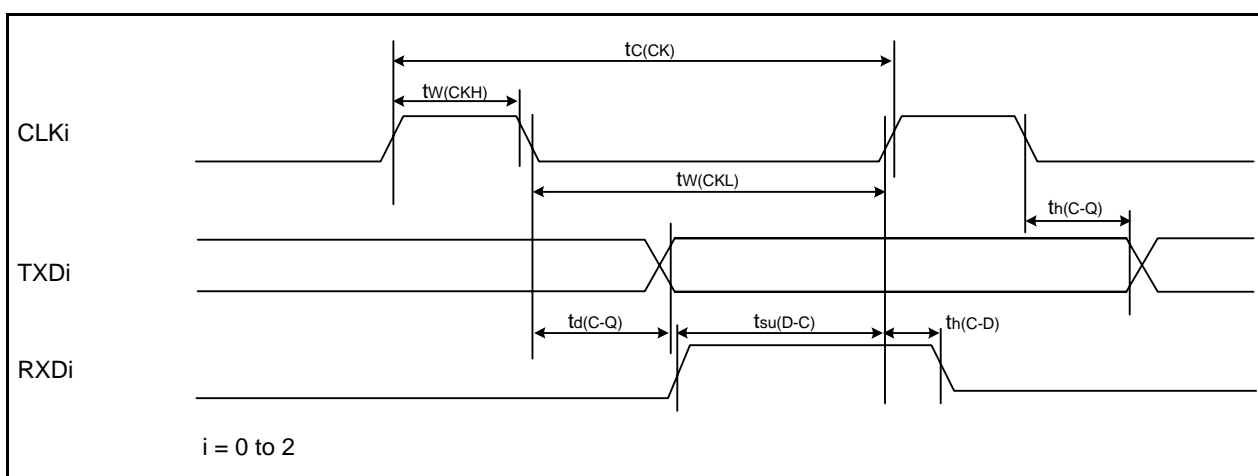


**Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)**

**Table 5.27 Timing Requirements of Serial Interface**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Standard						Unit
		V <sub>CC</sub> = 2.2V, T <sub>opr</sub> = 25°C		V <sub>CC</sub> = 3V, T <sub>opr</sub> = 25°C		V <sub>CC</sub> = 5V, T <sub>opr</sub> = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>c</sub> (CK)	CLKi input cycle time	800	—	300	—	200	—	ns
t <sub>w</sub> (CKH)	CLKi input “H” width	400	—	150	—	100	—	ns
t <sub>w</sub> (CKL)	CLKi input “L” width	400	—	150	—	100	—	ns
t <sub>d</sub> (C-Q)	TXDi output delay time	—	200	—	80	—	50	ns
t <sub>h</sub> (C-Q)	TXDi hold time	0	—	0	—	0	—	ns
t <sub>su</sub> (D-C)	RXDi input setup time	150	—	70	—	50	—	ns
t <sub>h</sub> (C-D)	RXDi input hold time	90	—	90	—	90	—	ns

i = 0 to 2



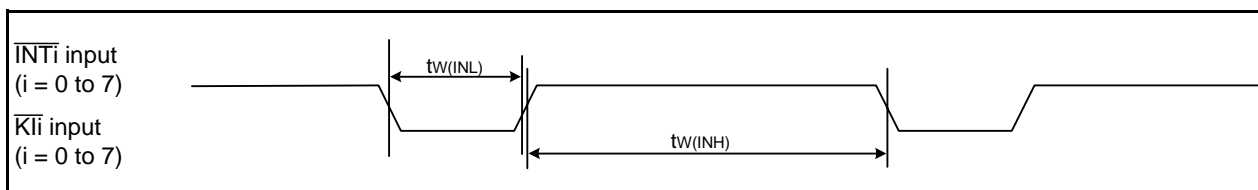
**Figure 5.10 Input and Output Timing of Serial Interface**

**Table 5.28 Timing Requirements of External Interrupt  $\overline{\text{INT}}_i$  (i = 0 to 7) and Key Input Interrupt  $\overline{\text{KLI}}_i$  (i = 0 to 7)**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tw(INH)	$\overline{\text{INTi}}$ input “H” width, $\overline{\text{KLi}}$ input “H” width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
tw(INL)	$\overline{\text{INTi}}$ input “L” width, $\overline{\text{KLi}}$ input “L” width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

Notes:

- When selecting the digital filter by the  $\overline{\text{INT}}_i$  input filter select bit, use an  $\overline{\text{INT}}_i$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the  $\overline{\text{INT}}_i$  input filter select bit, use an  $\overline{\text{INT}}_i$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



**Figure 5.11 Input Timing of External Interrupt  $\overline{\text{INT}}_i$  and Key Input Interrupt  $\overline{\text{KLI}}_i$**

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