1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Table 1.2 lists the Programmable I/O Ports Provided for Each Group, and Table 1.3 lists the LCD Display Function Pins Provided for Each Group. Figures 1.9 to 1.13 show the Pin Assignment for Each Group, and Tables 1.7 to 1.10 list Product Information.
The explanations in the chapters which follow apply to the R8C/L3AC Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/L35C Group	R8C/L36C Group	R8C/L38C Group	R8C/L3AC Group
I/O Ports	Programmable I/O ports	41 pins	52 pins	68 pins	88 pins
	High current drive ports	5 pins	8 pins	8 pins	16 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	8 pins	8 pins	8 pins
	Key input interrupt pins	4 pins	4 pins	8 pins	8 pins
Timer RA	Timer RA output pin	None	1 pin	1 pin	1 pin
Timer RB	Timer RB output pin	None	1 pin	1 pin	1 pin
Timer RD	Timer RD I/O pin	None	None	8 pins	8 pins
Timer RE	Timer RE output pin	None	1 pin	1 pin	1 pin
Timer RG	Timer RG I/O pin	None	None	None	2 pins
	Timer RG output pin	None	None	None	2 pins
A/D Converter	Analog input pin	10 pins	10 pins	16 pins	20 pins
LCD Drive Control Circuit	LCD power supply	3 pins (VL1, VL2, VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)
	Common output pins	Max. 4 pins	Max. 8 pins	Max. 8 pins	Max. 8 pins
	Segment output pins	Max. 24 pins	Max. 32 pins	Max. 48 pins	Max. 56 pins
Packages		52-pin LQFP	64-pin LQFP	80-pin LQFP	100-pin LQFP/ 100-pin QFP

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
Refer to **Tables 1.11 to 1.13, Pin Name Information by Pin Number**, for details.

Table 1.8 Product List for R8C/L36C Group Current of Apr 2011

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L367CNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	N Version
R5F2L367CNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368CNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368CNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36ACNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36ACNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L367CDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	D Version
R5F2L367CDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368CDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368CDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36ACDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36ACDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	

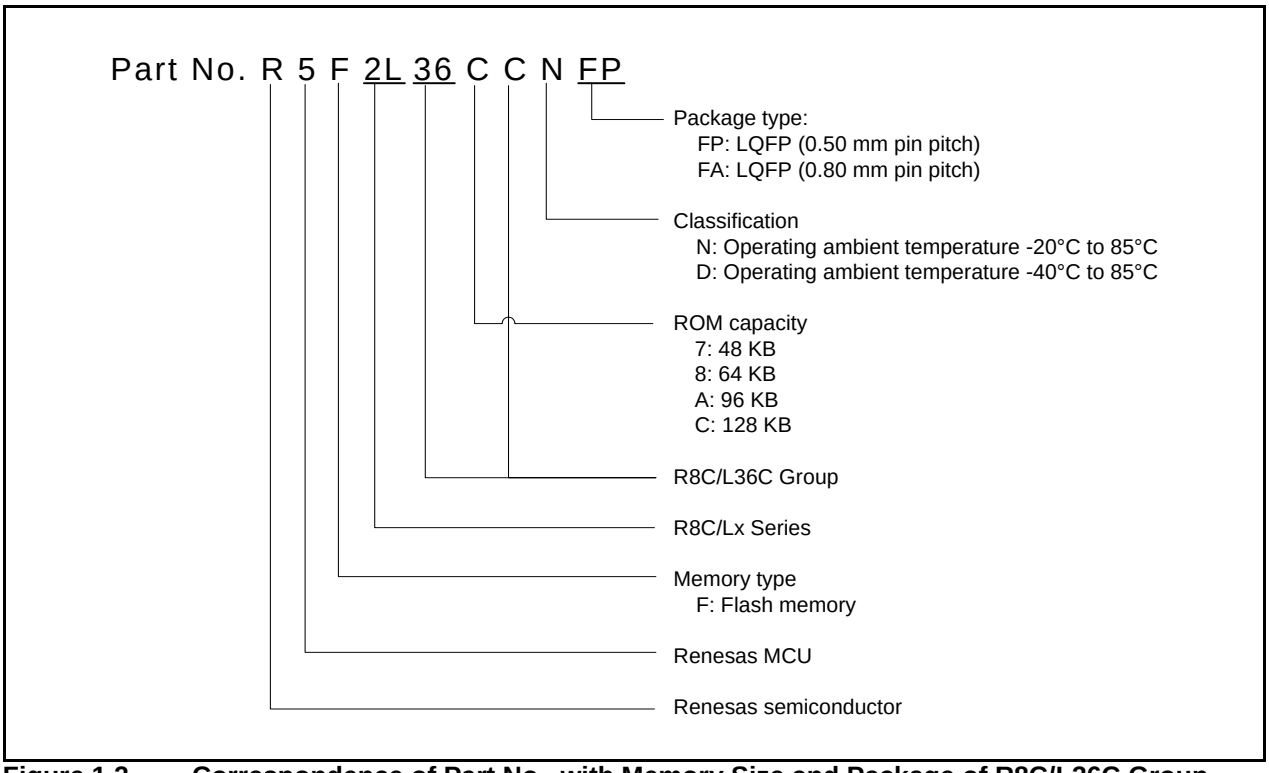


Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/L36C Group

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/L35C Group. Figure 1.6 shows a Block Diagram of R8C/L36C Group. Figure 1.7 shows a Block Diagram of R8C/L38C Group. Figure 1.8 shows a Block Diagram of R8C/L3AC Group.

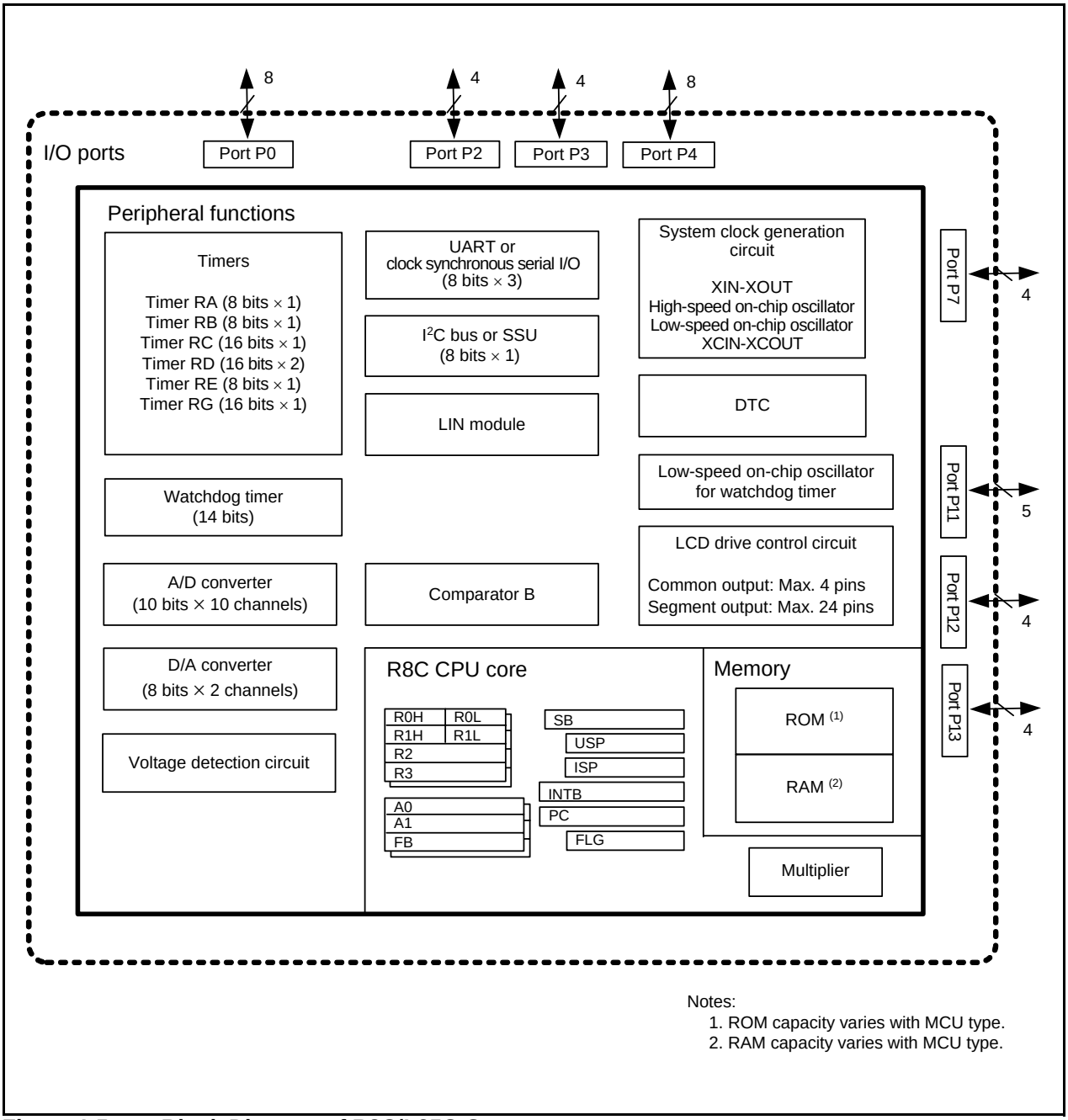
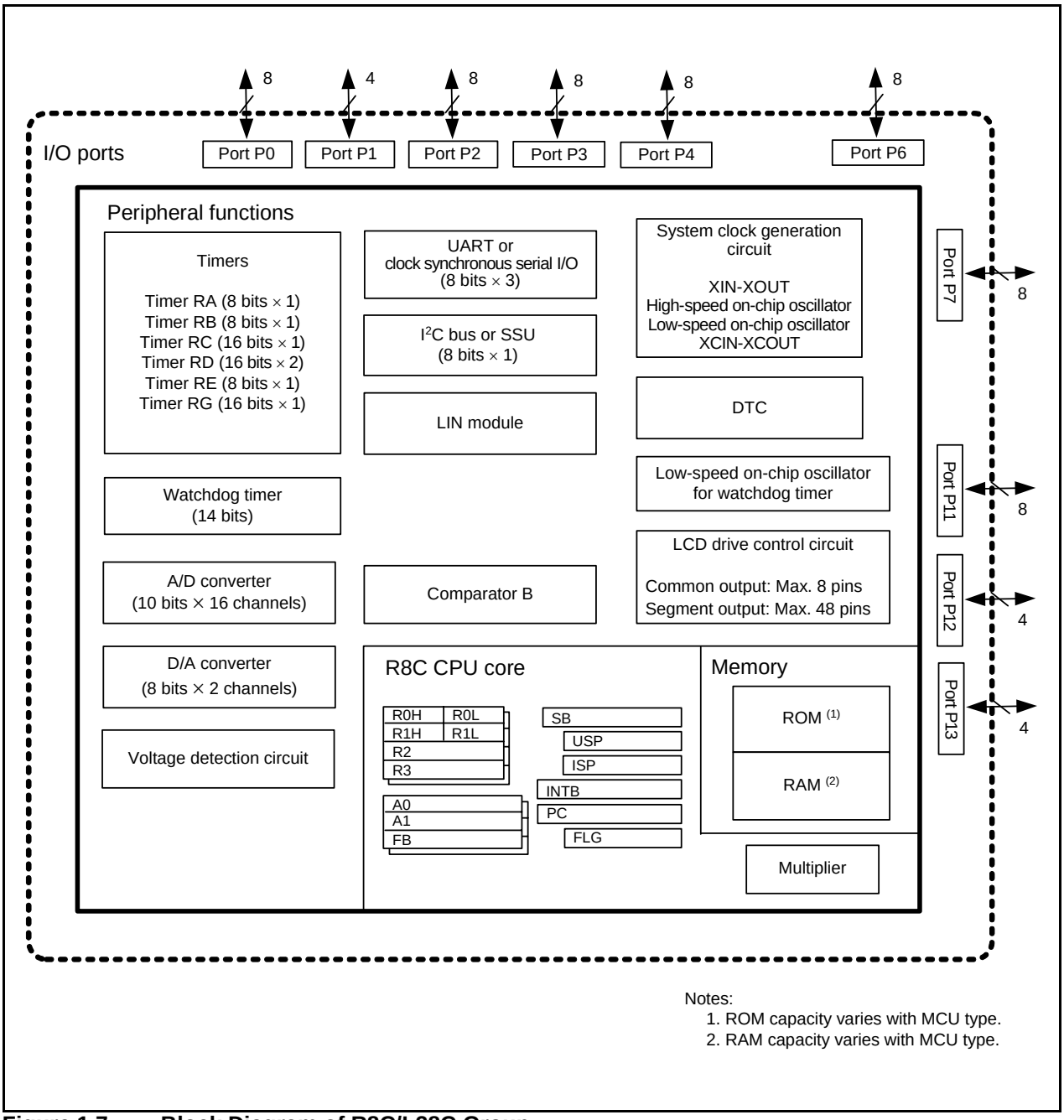
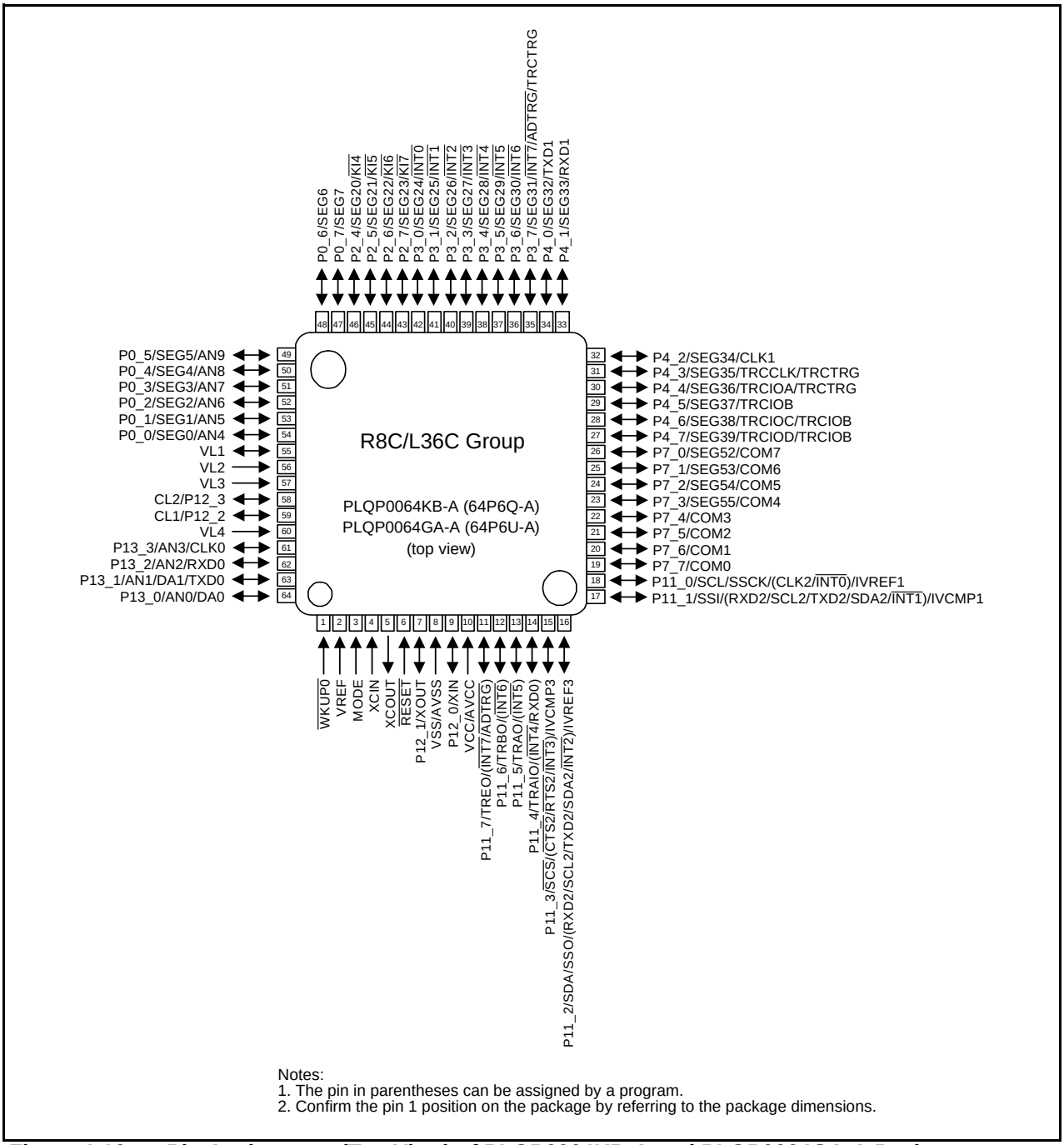


Figure 1.5 Block Diagram of R8C/L35C Group



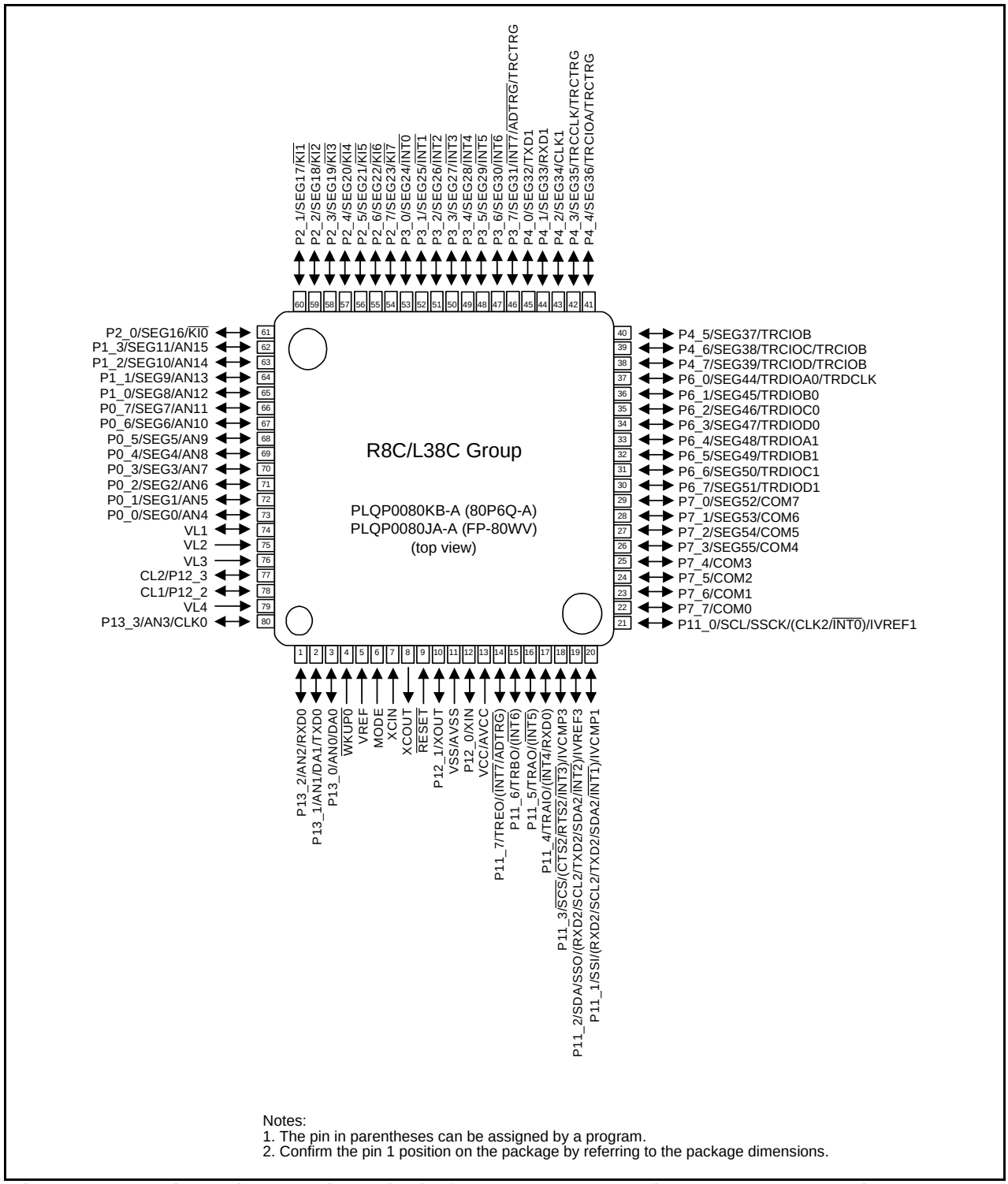
Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.7 Block Diagram of R8C/L38C Group



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.10 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.11 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages

Table 1.12 Pin Name Information by Pin Number (2)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
40 [42]	31				P6_6		TRDIOC1					SEG50
41 [43]	32				P6_5		TRDIOB1					SEG49
42 [44]	33				P6_4		TRDIOA1					SEG48
43 [45]	34				P6_3		TRDIOD0					SEG47
44 [46]	35				P6_2		TRDIOC0					SEG46
45 [47]	36				P6_1		TRDIOB0					SEG45
46 [48]	37				P6_0		TRDIOA0/ TRDCLK					SEG44
47 [49]					P5_3							SEG43
48 [50]					P5_2							SEG42
49 [51]					P5_1							SEG41
50 [52]					P5_0							SEG40
51 [53]	38	27	22		P4_7		TRCIOD/ TRCIOB					SEG39
52 [54]	39	28	23		P4_6		TRCIOC/ TRCIOB					SEG38
53 [55]	40	29	24		P4_5		TRCIOB					SEG37
54 [56]	41	30	25		P4_4		TRCIOA/ TRCTRG					SEG36
55 [57]	42	31	26		P4_3		TRCCLK/ TRCTRG					SEG35
56 [58]	43	32	27		P4_2			CLK1				SEG34
57 [59]	44	33	28		P4_1			RXD1				SEG33
58 [60]	45	34	29		P4_0			TXD1				SEG32
59 [61]	46	35			P3_7	$\overline{INT7}$	TRCTRG				$\overline{ADTRG}$	SEG31
60 [62]	47	36			P3_6	$\overline{INT6}$						SEG30
61 [63]	48	37			P3_5	$\overline{INT5}$						SEG29
62 [64]	49	38			P3_4	$\overline{INT4}$						SEG28
63 [65]	50	39	30		P3_3	$\overline{INT3}$						SEG27
64 [66]	51	40	31		P3_2	$\overline{INT2}$						SEG26
65 [67]	52	41	32		P3_1	$\overline{INT1}$						SEG25
66 [68]	53	42	33		P3_0	$\overline{INT0}$						SEG24
67 [69]	54	43	34		P2_7	$\overline{KI7}$						SEG23
68 [70]	55	44	35		P2_6	$\overline{KI6}$						SEG22
69 [71]	56	45	36		P2_5	$\overline{KI5}$						SEG21
70 [72]	57	46	37		P2_4	$\overline{KI4}$						SEG20
71 [73]	58				P2_3	$\overline{KI3}$						SEG19
72 [74]	59				P2_2	$\overline{KI2}$						SEG18
73 [75]	60				P2_1	$\overline{KI1}$						SEG17
74 [76]	61				P2_0	$\overline{KI0}$						SEG16
75 [77]					P1_7							SEG15
76 [78]					P1_6							SEG14
77 [79]					P1_5							SEG13
78 [80]					P1_4							SEG12
79 [81]	62				P1_3						AN15	SEG11
80 [82]	63				P1_2						AN14	SEG10
81 [83]	64				P1_1						AN13	SEG9
82 [84]	65				P1_0						AN12	SEG8
83 [85]	66	47	38		P0_7						AN11 (3)	SEG7
84 [86]	67	48	39		P0_6						AN10 (3)	SEG6

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.
3. Pins AN10 and AN11 are not available in the R8C/L35C, and R8C/L36C Groups.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

3. Memory

Figure 3.1 is a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

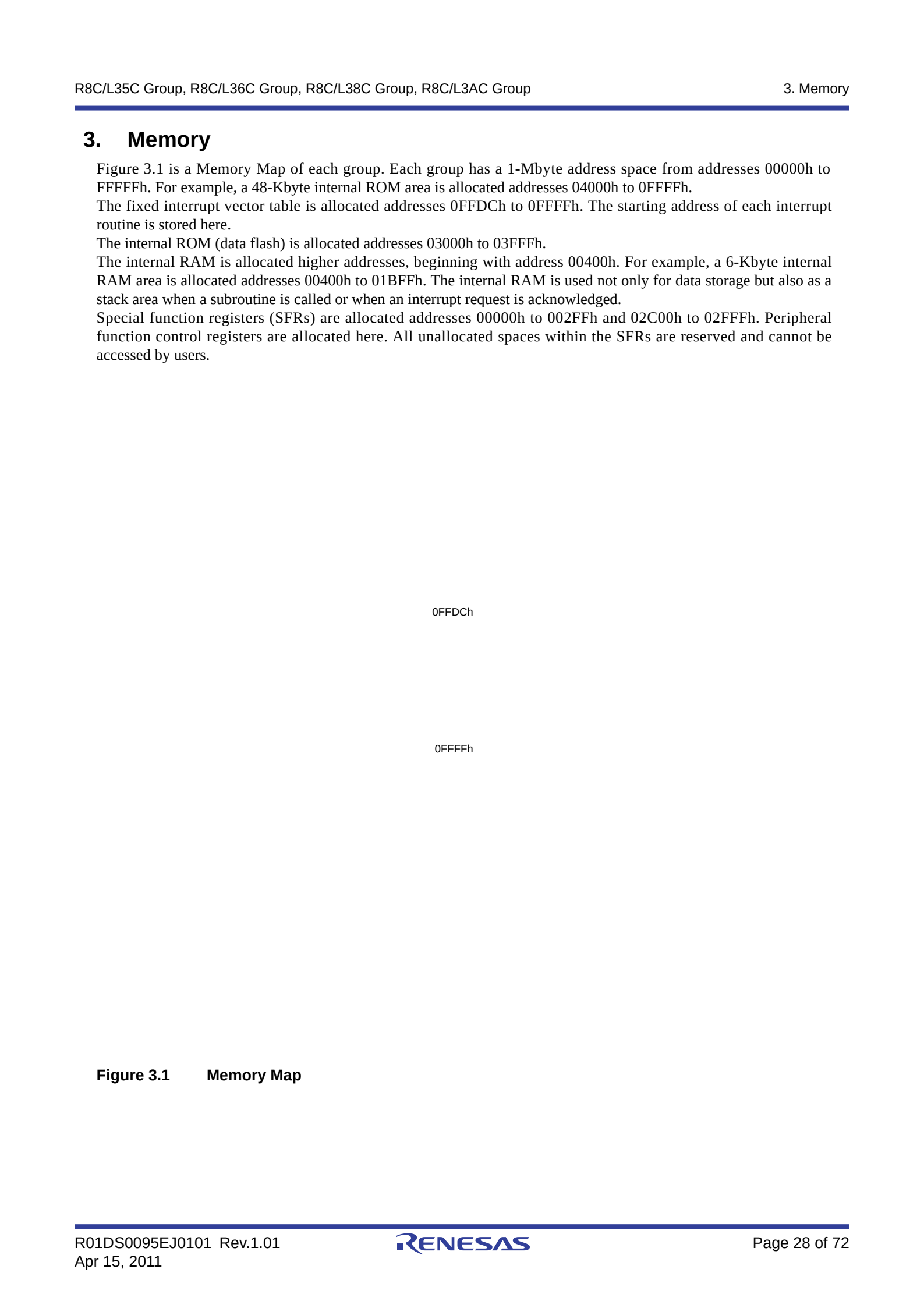


Figure 3.1 Memory Map

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h	LCD Bias Control Register	LCR1	00h
0202h	LCD Display Control Register	LCR2	X0000000b
0203h	LCD Clock Control Register	LCR3	00h
0204h			
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h	LCD Port Select Register 3	LSE3	00h
020Ah	LCD Port Select Register 4	LSE4	00h
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch	LCD Port Select Register 6	LSE6	00h
020Dh	LCD Port Select Register 7	LSE7	00h
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh		LRA27L	XXh
022Ch		LRA28L	XXh
022Dh		LRA29L	XXh
022Eh		LRA30L	XXh
022Fh		LRA31L	XXh
0230h		LRA32L	XXh
0231h		LRA33L	XXh
0232h		LRA34L	XXh
0233h		LRA35L	XXh
0234h		LRA36L	XXh
0235h		LRA37L	XXh
0236h		LRA38L	XXh
0237h		LRA39L	XXh
0238h		LRA40L	XXh
0239h		LRA41L	XXh
023Ah		LRA42L	XXh
023Bh		LRA43L	XXh
023Ch		LRA44L	XXh
023Dh		LRA45L	XXh
023Eh		LRA46L	XXh
023Fh		LRA47L	XXh

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

5.3 Peripheral Function Characteristics

Table 5.3 A/D Converter Characteristics
(V_{CC}/AV_{CC} = Vref = 2.2 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V_{ref} = AV_{CC}		—	—	10	Bit
—	Absolute accuracy (2)	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN19 input	—	—	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN19 input	—	—	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN19 input	—	—	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN19 input	—	—	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN19 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN19 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN19 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN19 input	—	—	±2	LSB
ϕAD	A/D conversion clock		4.0 ≤ V_{ref} = AV_{CC} ≤ 5.5 V (1)		2	—	20	MHz
			3.2 ≤ V_{ref} = AV_{CC} ≤ 5.5 V (1)		2	—	16	MHz
			2.7 ≤ V_{ref} = AV_{CC} ≤ 5.5 V (1)		2	—	10	MHz
			2.2 ≤ V_{ref} = AV_{CC} ≤ 5.5 V (1)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	—	—	µs
I_{Vref}	V_{ref} current		Vcc = 5 V, XIN = f1 = ϕAD = 20 MHz		—	45	—	µA
V_{ref}	Reference voltage				2.2	—	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	—	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.18 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	7.0	15	mA
			16 MHz	Off	Off	125 kHz	No division	—		—	5.6	12.5	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	3.6	—	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—		—	3.0	—	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	—		—	2.2	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		—	90	400	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		—	100	400	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	—	55	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	100	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	90	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	7	—	µA
										LCD drive control circuit (5) When the internal voltage multiplier is used	—	12	—	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2.0	5.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off		—	15	—	µA
		Power-off mode	Off	Off	Off	Off	—	—	Topr = 25°C		—	0.02	0.2	µA
			Off	Off	Off	Off	—	—	Topr = 85°C		—	0.4	—	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V
4. VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
5. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

Table 5.24 Timing Requirements of I²C bus Interface (1)
(Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
tSCL	SCL input cycle time		12tCYC + 600 (1)	—	—	ns
tSCLH	SCL input “H” width		3tCYC + 300 (1)	—	—	ns
tSCLL	SCL input “L” width		5tCYC + 500 (1)	—	—	ns
tsf	SCL, SDA input fall time		—	—	300	ns
tSP	SCL, SDA input spike pulse rejection time		—	—	1tCYC (1)	ns
tBUF	SDA input bus-free time		5tCYC (1)	—	—	ns
tSTAH	Start condition input hold time		3tCYC (1)	—	—	ns
tSTAS	Retransmit start condition input setup time		3tCYC (1)	—	—	ns
tSTOP	Stop condition input setup time		3tCYC (1)	—	—	ns
tSDAS	Data input setup time		1tCYC + 40 (1)	—	—	ns
tSDAH	Data input hold time		10	—	—	ns

Note:
1. 1tCYC = 1/f1(s)

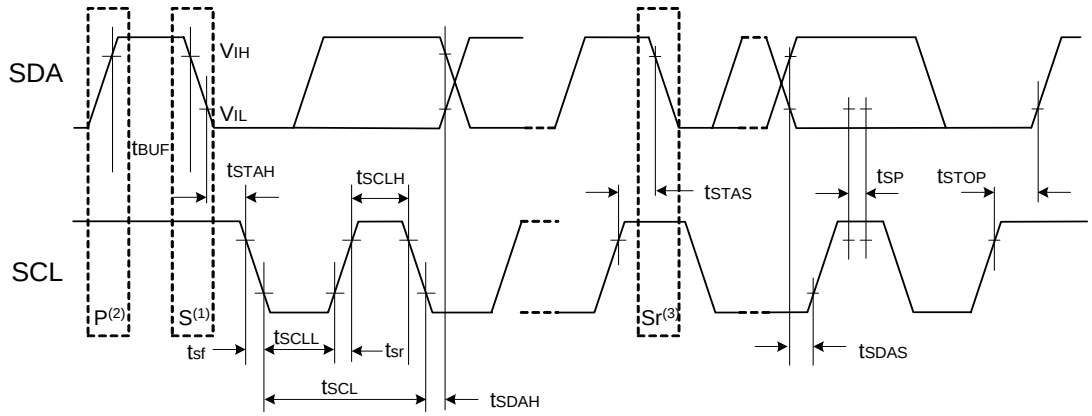
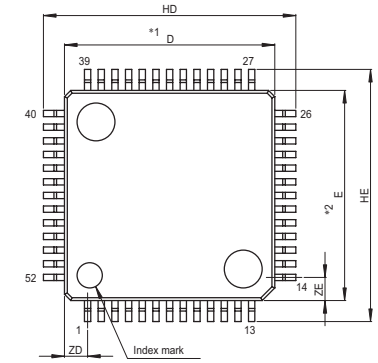


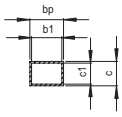
Figure 5.7 I/O Timing of I²C bus Interface

Package Dimensions

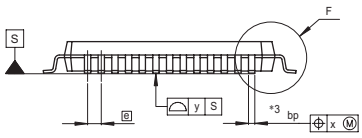
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

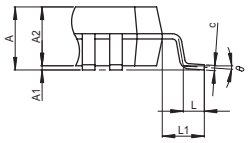
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g





Terminal cross section



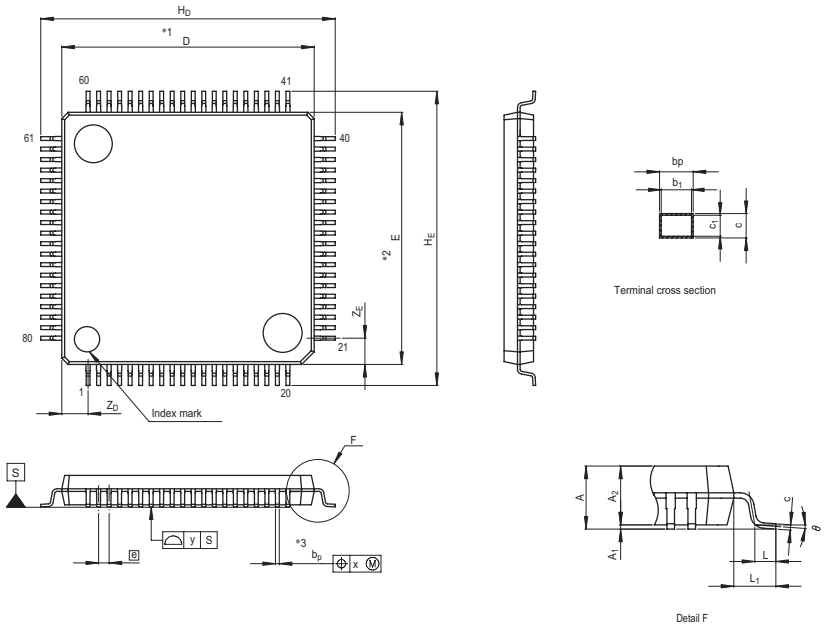


Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

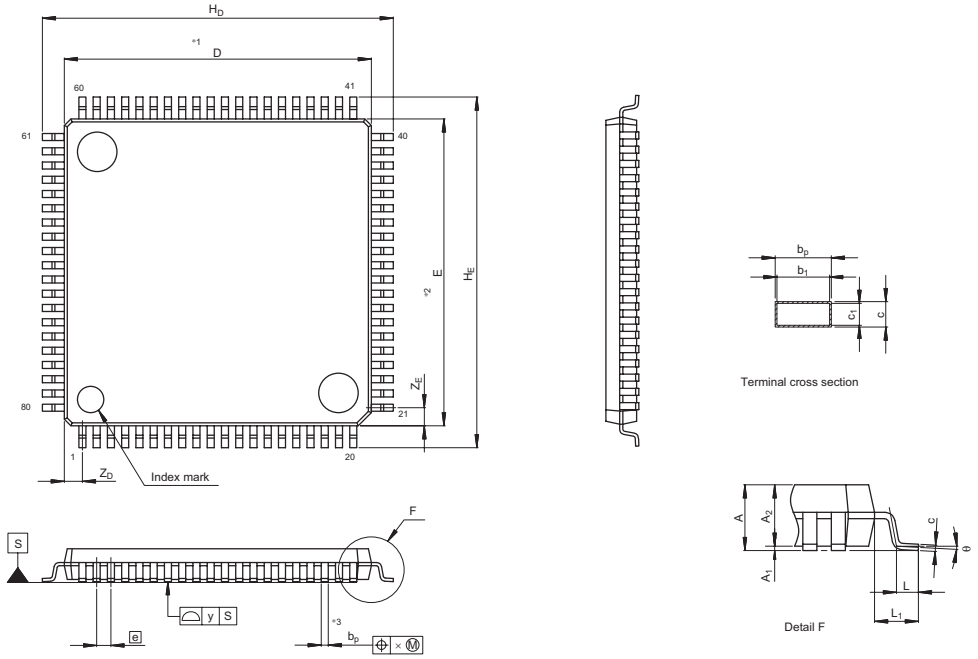
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

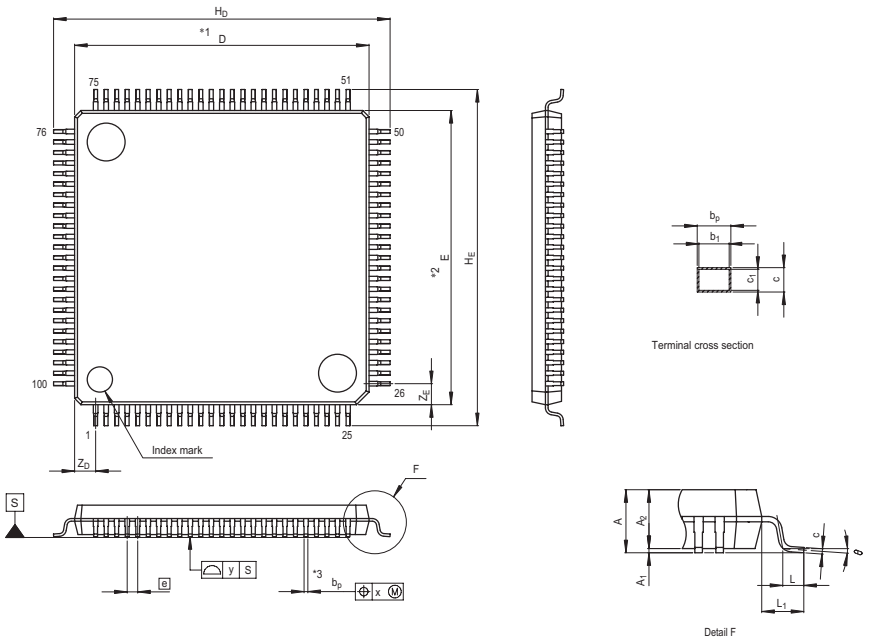
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

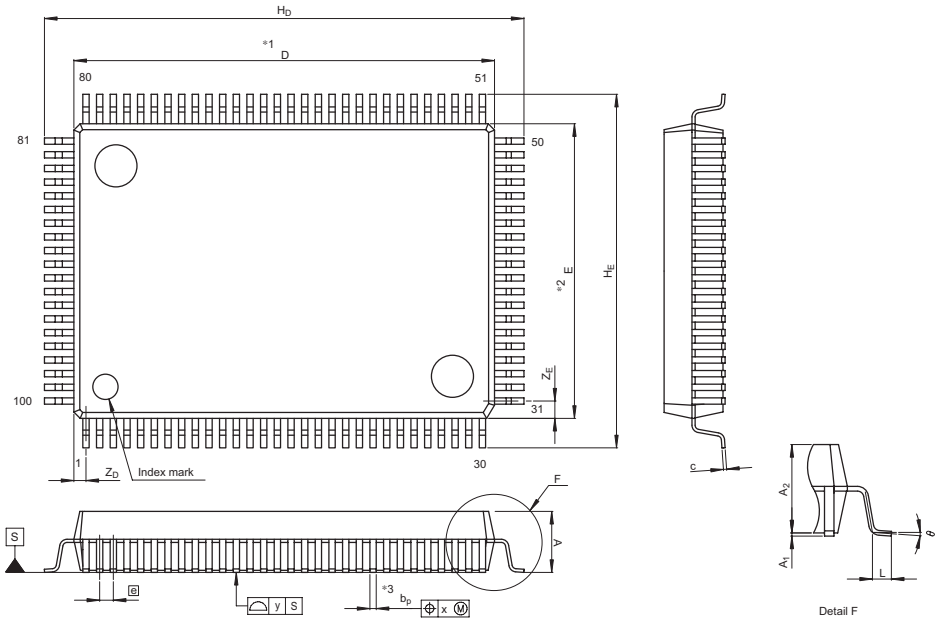
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8