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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Last Time Buy
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l38ccnfp-30

1.1.3 Specifications

Tables 1.4 to 1.6 list the Specifications.

Table 1.4 Specifications (1)

Item	Function		Specification
CPU	Central processing unit		R8C CPU core - Number of fundamental instructions: 89 - Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V) - Multiplier: 16 bits × 16 bits → 32 bits - Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits - Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM/RAM Data flash		Refer to Tables 1.7 to 1.10 Product Lists .
Power Supply Voltage Detection	Voltage detection circuit		- Power-on reset - Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	R8C/L35C Group	- CMOS I/O ports: 41, selectable pull-up resistor - High current drive ports: 5
		R8C/L36C Group	- CMOS I/O ports: 52, selectable pull-up resistor - High current drive ports: 8
		R8C/L38C Group	- CMOS I/O ports: 68, selectable pull-up resistor - High current drive ports: 8
		R8C/L3AC Group	- CMOS I/O ports: 88, selectable pull-up resistor - High current drive ports: 16
Clock	Clock generation circuits		4 circuits: XIN clock oscillation circuit XCIN clock oscillation circuit (32 kHz) High-speed on-chip oscillator (with frequency adjustment function) Low-speed on-chip oscillator - Oscillation stop detection: XIN clock oscillation stop detection function - Frequency divider circuit: Division ratio selectable from 1, 2, 4, 8, and 16 - Low-power-consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode
			Real-time clock (timer RE)
Interrupts	R8C/L35C Group		- Number of interrupt vectors: 69 - External Interrupt: 9 ($\overline{INT} \times 5$, key input × 4) - Priority levels: 7 levels
	R8C/L36C Group		- Number of interrupt vectors: 69 - External Interrupt: 12 ($\overline{INT} \times 8$, key input × 4) - Priority levels: 7 levels
	R8C/L38C Group		- Number of interrupt vectors: 69 - External Interrupt: 16 ($\overline{INT} \times 8$, key input × 8) - Priority levels: 7 levels
	R8C/L3AC Group		- Number of interrupt vectors: 69 - External Interrupt: 16 ($\overline{INT} \times 8$, key input × 8) - Priority levels: 7 levels
Watchdog Timer			14 bits × 1 (with prescaler) - Selectable reset start function - Selectable low-speed on-chip oscillator for watchdog timer
DTC (Data Transfer Controller)			1 channel - Activation sources: 38 - Transfer modes: 2 (normal mode, repeat mode)

Table 1.8 Product List for R8C/L36C Group**Current of Apr 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L367CNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	N Version
R5F2L367CNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368CNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368CNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36ACNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36ACNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L367CDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	D Version
R5F2L367CDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368CDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368CDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36ACDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36ACDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	

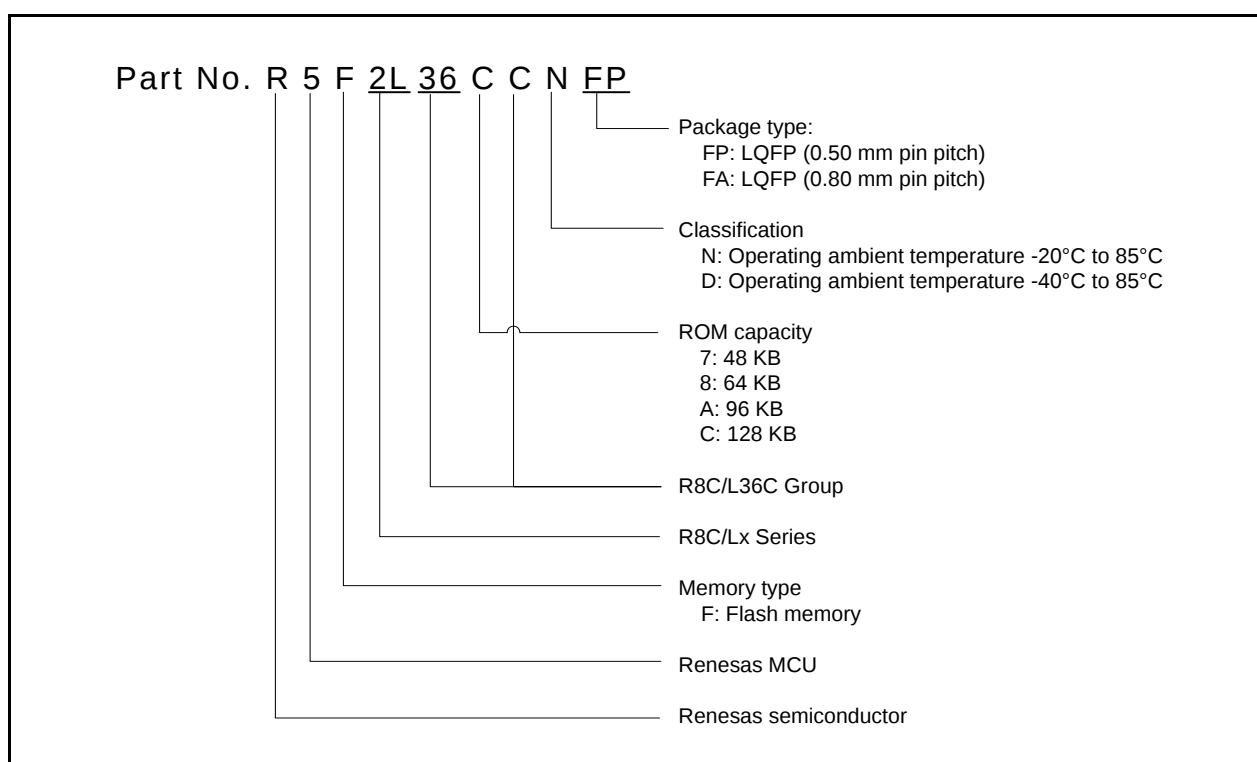
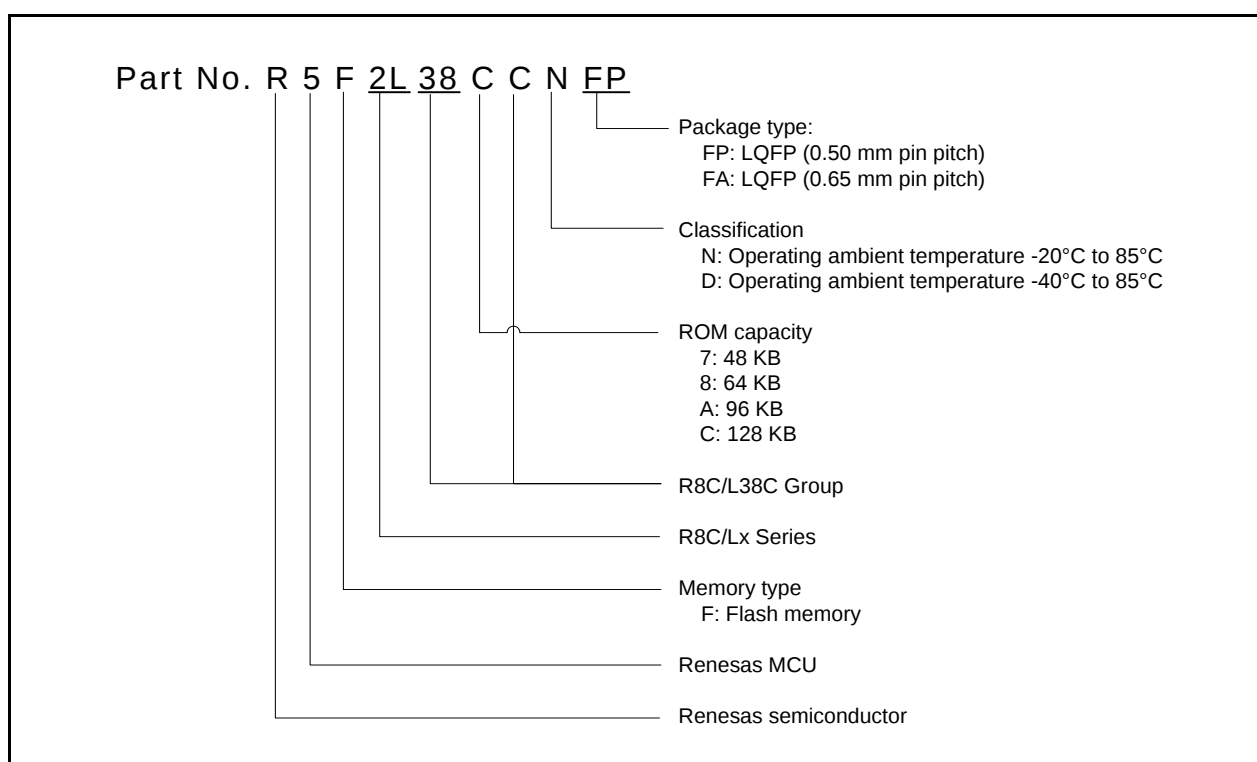
**Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/L36C Group**

Table 1.9 Product List for R8C/L38C Group**Current of Apr 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L387CNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	N Version
R5F2L387CNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080JA-A	
R5F2L388CNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2L388CNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080JA-A	
R5F2L38ACNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38ACNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L38CCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38CCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L387CDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	D Version
R5F2L387CDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080JA-A	
R5F2L388CDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2L388CDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080JA-A	
R5F2L38ACDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38ACDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L38CCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38CCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	

**Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/L38C Group**

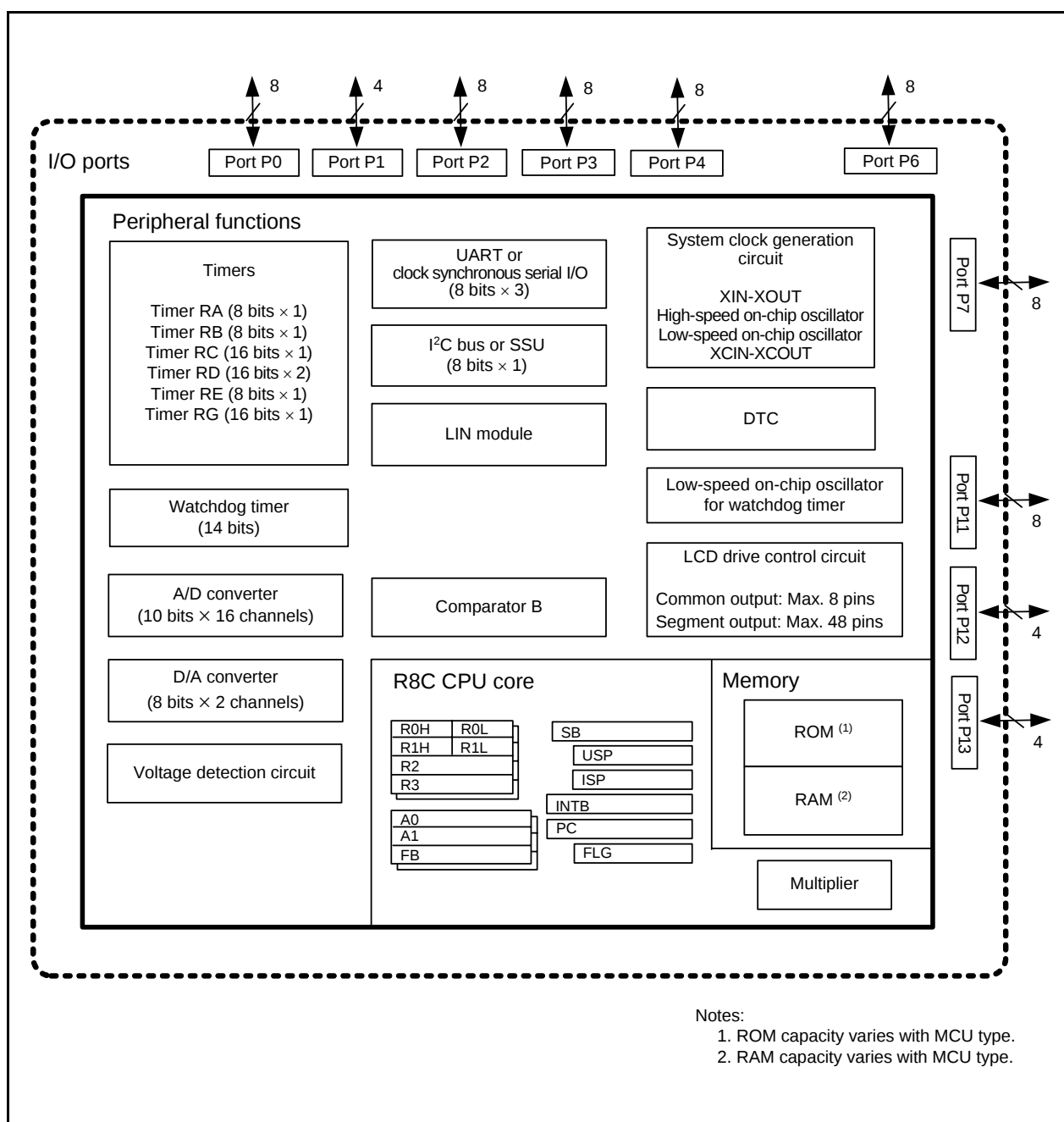


Figure 1.7 Block Diagram of R8C/L38C Group

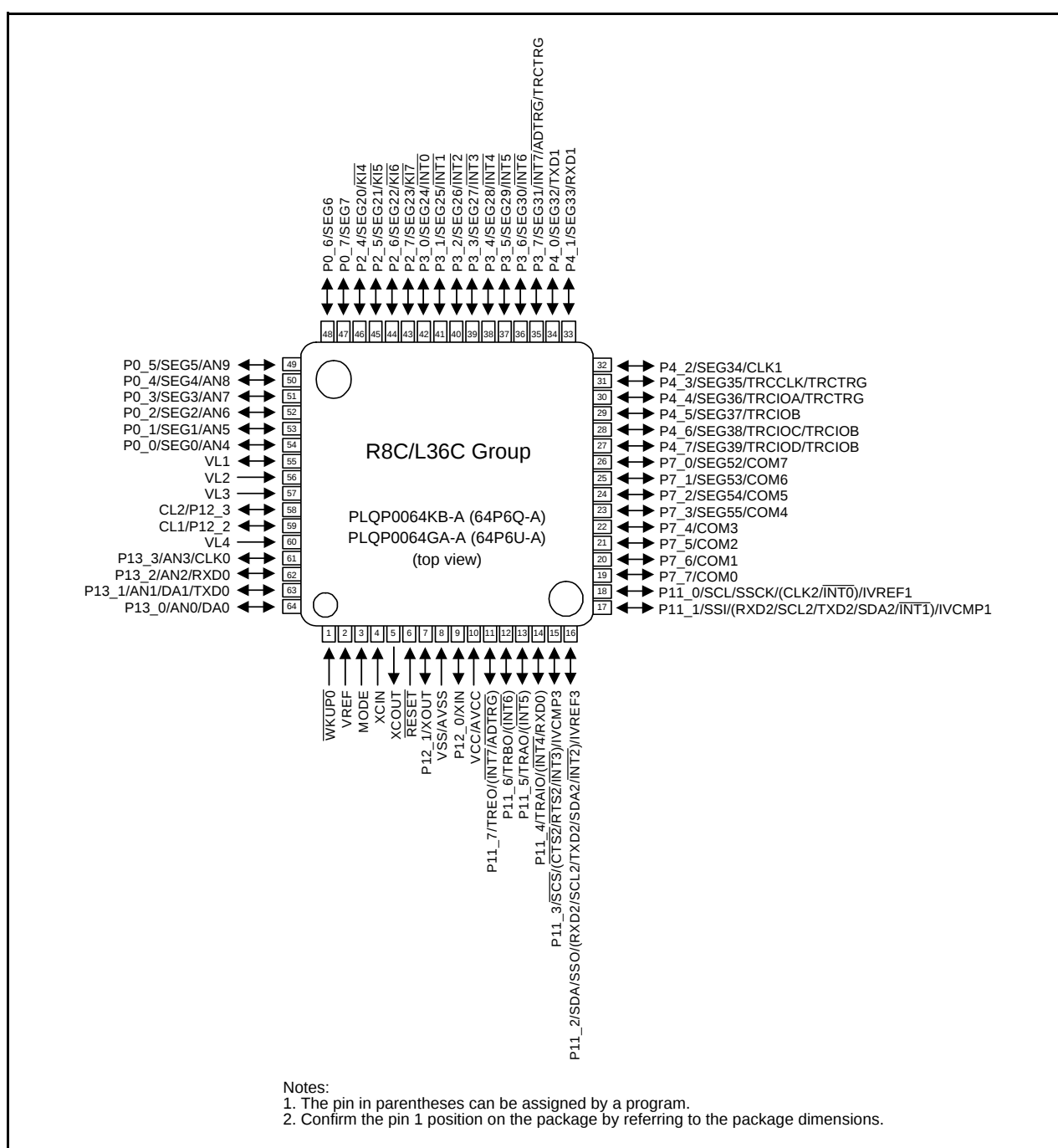


Figure 1.10 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages

Table 1.12 Pin Name Information by Pin Number (2)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
40 [42]	31				P6_6		TRDIOC1					SEG50
41 [43]	32				P6_5		TRDIOB1					SEG49
42 [44]	33				P6_4		TRDIOA1					SEG48
43 [45]	34				P6_3		TRDIOD0					SEG47
44 [46]	35				P6_2		TRDIOC0					SEG46
45 [47]	36				P6_1		TRDIOB0					SEG45
46 [48]	37				P6_0		TRDIOA0/ TRDCLK					SEG44
47 [49]					P5_3							SEG43
48 [50]					P5_2							SEG42
49 [51]					P5_1							SEG41
50 [52]					P5_0							SEG40
51 [53]	38	27	22		P4_7		TRCIOD/ TRCIOB					SEG39
52 [54]	39	28	23		P4_6		TRCIOA/ TRCIOB					SEG38
53 [55]	40	29	24		P4_5		TRCIOB					SEG37
54 [56]	41	30	25		P4_4		TRCIOA/ TRCTRG					SEG36
55 [57]	42	31	26		P4_3		TRCCLK/ TRCTRG					SEG35
56 [58]	43	32	27		P4_2			CLK1				SEG34
57 [59]	44	33	28		P4_1			RXD1				SEG33
58 [60]	45	34	29		P4_0			TXD1				SEG32
59 [61]	46	35			P3_7	INT7	TRCTRG				ADTRG	SEG31
60 [62]	47	36			P3_6	INT6						SEG30
61 [63]	48	37			P3_5	INT5						SEG29
62 [64]	49	38			P3_4	INT4						SEG28
63 [65]	50	39	30		P3_3	INT3						SEG27
64 [66]	51	40	31		P3_2	INT2						SEG26
65 [67]	52	41	32		P3_1	INT1						SEG25
66 [68]	53	42	33		P3_0	INT0						SEG24
67 [69]	54	43	34		P2_7	K17						SEG23
68 [70]	55	44	35		P2_6	K16						SEG22
69 [71]	56	45	36		P2_5	K15						SEG21
70 [72]	57	46	37		P2_4	K14						SEG20
71 [73]	58				P2_3	K13						SEG19
72 [74]	59				P2_2	K12						SEG18
73 [75]	60				P2_1	K11						SEG17
74 [76]	61				P2_0	K10						SEG16
75 [77]					P1_7							SEG15
76 [78]					P1_6							SEG14
77 [79]					P1_5							SEG13
78 [80]					P1_4							SEG12
79 [81]	62				P1_3						AN15	SEG11
80 [82]	63				P1_2						AN14	SEG10
81 [83]	64				P1_1						AN13	SEG9
82 [84]	65				P1_0						AN12	SEG8
83 [85]	66	47	38		P0_7						AN11 ⁽³⁾	SEG7
84 [86]	67	48	39		P0_6						AN10 ⁽³⁾	SEG6

Notes:

1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.
3. Pins AN10 and AN11 are not available in the R8C/L35C, and R8C/L36C Groups.

Table 1.13 Pin Name Information by Pin Number (3)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
85 [87]	68	49	40		P0_5						AN9	SEG5
86 [88]	69	50	41		P0_4						AN8	SEG4
87 [89]	70	51	42		P0_3						AN7	SEG3
88 [90]	71	52	43		P0_2						AN6	SEG2
89 [91]	72	53	44		P0_1						AN5	SEG1
90 [92]	73	54	45		P0_0						AN4	SEG0
91 [93]	74	55	46									VL1
92 [94]	75	56	47									VL2
93 [95]	76	57										VL3
94 [96]	77	58	48		P12_3							CL2
95 [97]	78	59	49		P12_2							CL1
96 [98]	79	60	50									VL4
97 [99]					P13_7		TRGCLKB				AN19	
98 [100]					P13_6		TRGIOB				AN18	
99 [1]					P13_5		TRGCLKA				AN17	
100 [2]					P13_4		TRGIOA				AN16	

Notes:

1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.16 list SFR Informations and Table 4.17 lists the ID Code Areas and Option Function Select Area. The description offered in this chapter is based on the R8C/L3AC Group.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXh (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	X0000000b
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
- The CSPROINI bit in the OFS register is set to 0.
- The LVDAS bit in the OFS register is set to 1.
- The LVDAS bit in the OFS register is set to 0.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A 0 Register	DA0	00h
00D9h	D/A 1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P10 Register	P10	XXh
00F5h	Port P11 Register	P11	XXh
00F6h	Port P10 Direction Register	PD10	00h
00F7h	Port P11 Direction Register	PD11	00h
00F8h	Port P12 Register	P12	XXh
00F9h	Port P13 Register	P13	XXh
00FAh	Port P12 Direction Register	PD12	00h
00FBh	Port P13 Direction Register	PD13	00h
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	After Reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIOA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIOA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11100000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	01000000b
0171h	Timer RG Count Control Register	TRGCNTC	00h
0172h	Timer RG Control Register	TRGCR	10000000b
0173h	Timer RG Interrupt Enable Register	TRGIER	11110000b
0174h	Timer RG Status Register	TRGSR	11100000b
0175h	Timer RG I/O Control Register	TRGIOR	00h
0176h	Timer RG Counter	TRG	00h
0177h			00h
0178h	Timer RG General Register A	TRGGRA	FFh
0179h			FFh
017Ah	Timer RG General Register B	TRGGRB	FFh
017Bh			FFh
017Ch	Timer RG General Register C	TRGGRC	FFh
017Dh			FFh
017Eh	Timer RG General Register D	TRGGRD	FFh
017Fh			FFh

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{cc} /AV _{cc}	Supply voltage			−0.3 to 6.5	V
V _i	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) ⁽¹⁾	−0.3 to 1.65	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) ⁽¹⁾	−0.3 to V _{cc} + 0.3	V
		VL1		−0.3 to VL2	V
		VL2	R8C/L35C	VL1 to VL4	V
			R8C/L36C, R8C/L38C, R8C/L3AC	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		VL3 to 6.5	V
		Other pins		−0.3 to V _{cc} + 0.3	V
V _o	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) ⁽¹⁾	−0.3 to 1.65	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) ⁽¹⁾	−0.3 to V _{cc} + 0.3	V
		VL1		−0.3 to VL2 ⁽²⁾	V
		VL2	R8C/L35C	VL1 to VL4	V
			R8C/L36C, R8C/L38C, R8C/L3AC	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		−0.3 to 6.5	V
		CL1, CL2		−0.3 to 6.5	V
		COM0 to COM7		−0.3 to VL4	V
		SEG0 to SEG55		−0.3 to VL4	V
		Other pins		−0.3 to V _{cc} + 0.3	V
P _d	Power dissipation		−40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature			−20 to 85 (N version) / −40 to 85 (D version)	°C
T _{stg}	Storage temperature			−65 to 150	°C

Notes:

- For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
- The VL1 voltage should be VCC or below.

Table 5.4 D/A Converter Characteristics
($V_{CC}/AV_{CC} = V_{ref} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
t_{su}	Setup time		—	—	3	μs
R_o	Output resistor		—	6	—	$\text{k}\Omega$
I_{vref}	Reference power input current	(Note 1)	—	—	1.5	mA

Note:

1. This applies when one D/A converter is used and the value of the DAI register ($i = 0$ or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator B Characteristics
($V_{CC} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
V_i	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time ⁽¹⁾	$V_i = V_{ref} \pm 100$ mV	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0$ V	—	17.5	—	μA

Note:

1. When the digital filter is disabled.

Table 5.6 Flash Memory (Program ROM) Characteristics
(V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽¹⁾		1,000 ⁽²⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	ms
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁶⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. Definition of programming/erasure endurance
 The programming and erasure endurance is defined on a per-block basis.
 If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7 Flash Memory (Data flash Block A to Block D) Characteristics
(V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽¹⁾		10,000 ⁽²⁾	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	ms
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20 ⁽⁶⁾	—	85	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

- Definition of programming/erasure endurance
 The programming and erasure endurance is defined on a per-block basis.
 If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 40°C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.

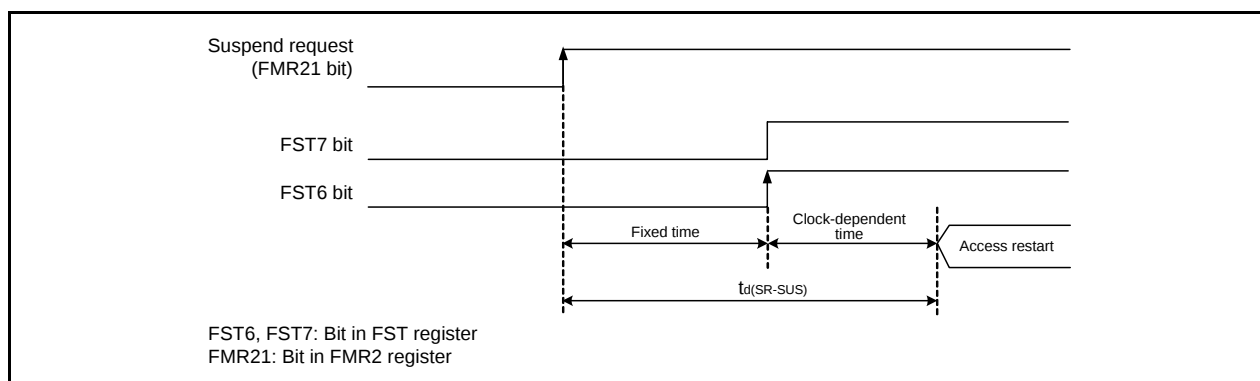


Figure 5.2 Time delay until Suspend

Table 5.20 DC Characteristics (4) [2.7 V ≤ V_{CC} < 4.0 V]
(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition							Standard			Unit		
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)		Max.	
XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed												
I _{CC}	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—			—	7.0	14.5	mA	
			10 MHz	Off	Off	125 kHz	No division	—			—	3.6	10	mA	
			20 MHz	Off	Off	125 kHz	Divide-by-8	—			—	3.0	—	mA	
			10 MHz	Off	Off	125 kHz	Divide-by-8	—			—	1.5	—	mA	
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—			—	7.0	14.5	mA	
			Off	Off	20 MHz	125 kHz	Divide-by-8	—			—	3.0	—	mA	
			Off	Off	10 MHz	125 kHz	No division	—			—	4.0	—	mA	
			Off	Off	10 MHz	125 kHz	Divide-by-8	—			—	1.7	—	mA	
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			—	1	—	mA	
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	85	390	μA	
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	90	400	μA	
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM			—	50	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	15	90	μA	
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	5	80	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	5	—	μA	
									LCD drive control circuit (5) When the internal voltage multiplier is used			—	11	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	μA	
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	T _{opr} = 25°C Peripheral clock off		—	2	5.0	μA	
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	T _{opr} = 85°C Peripheral clock off		—	13.0	—	μA	
		Power-off mode	Off	Off	Off	Off	—	—	T _{opr} = 25°C		—	0.02	0.2	μA	
			Off	Off	Off	Off	—	—	T _{opr} = 85°C		—	0.3	—	μA	

Notes:

- V_{CC} = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are V_{SS}.
- XIN is set to square wave input.
- V_{CC} = 3.0 V
- V_{LCD} = V_{CC}, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
- The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

5.5 AC Characteristics

Table 5.23 Timing Requirements of Synchronous Serial Communication Unit (SSU)
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	—	—	tcyc (1)
tHI	SSCK clock "H" width			0.4	—	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	—	0.6	tsucyc
tRISE	SSCK clock rising time	Master		—	—	1	tcyc (1)
		Slave		—	—	1	μs
tFALL	SSCK clock falling time	Master		—	—	1	tcyc (1)
		Slave		—	—	1	μs
tsu	SSO, SSI data input setup time			100	—	—	ns
tH	SSO, SSI data input hold time			1	—	—	tcyc (1)
tLEAD	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	—	—	ns
tLAG	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	—	—	ns
tOD	SSO, SSI data output delay time			—	—	1	tcyc (1)
tsA	SSI slave access time		$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	—	—	$1.5\text{tcyc} + 100$	ns
			$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	$1.5\text{tcyc} + 200$	ns
toR	SSI slave out open time		$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	—	—	$1.5\text{tcyc} + 100$	ns
			$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	$1.5\text{tcyc} + 200$	ns

Note:

1. $1\text{tcyc} = 1/f_1(\text{s})$

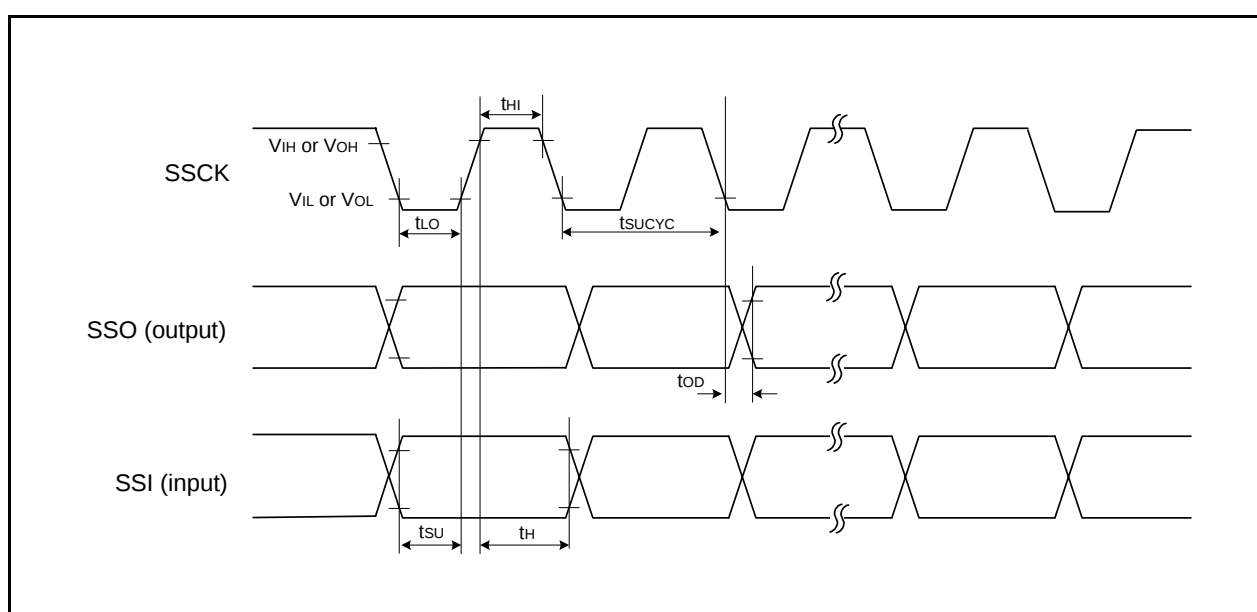


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.25 External Clock Input (XIN, XCIN)
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		VCC = 2.2V, Topr = 25°C		VCC = 3V, Topr = 25°C		VCC = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tC(XIN)	XIN input cycle time	200	—	50	—	50	—	ns
tWH(XIN)	XIN input "H" width	90	—	24	—	24	—	ns
tWL(XIN)	XIN input "L" width	90	—	24	—	24	—	ns
tC(XCIN)	XCIN input cycle time	14	—	14	—	14	—	μs
tWH(XCIN)	XCIN input "H" width	7	—	7	—	7	—	μs
tWL(XCIN)	XCIN input "L" width	7	—	7	—	7	—	μs

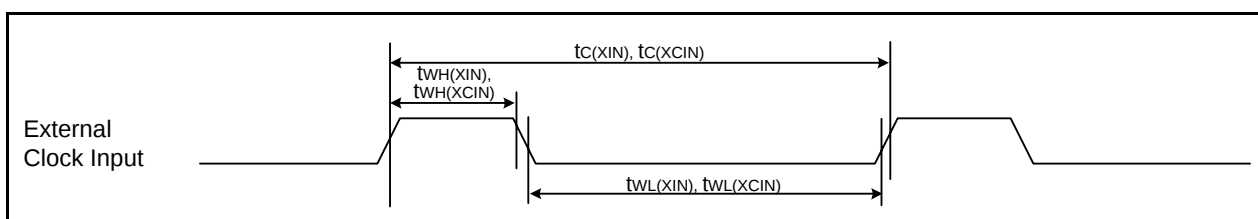


Figure 5.8 External Clock Input Timing Diagram

Table 5.26 Timing Requirements of TRAIO
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		VCC = 2.2V, Topr = 25°C		VCC = 3V, Topr = 25°C		VCC = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (TRAIO)	TRAIO input cycle time	500	—	300	—	100	—	ns
t _{WH} (TRAIO)	TRAIO input “H” width	200	—	120	—	40	—	ns
t _{WL} (TRAIO)	TRAIO input “L” width	200	—	120	—	40	—	ns

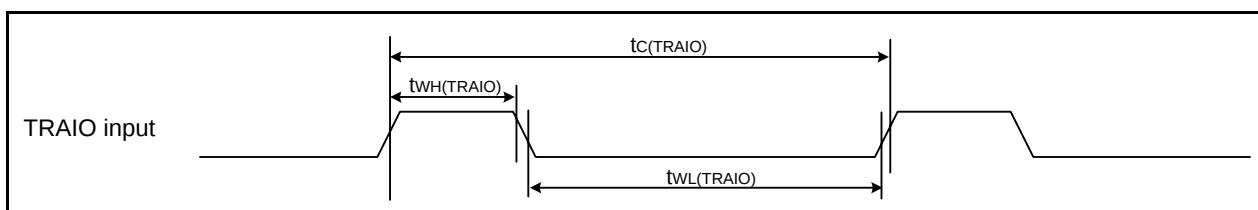


Figure 5.9 Input Timing of TRAIO

Table 5.27 Timing Requirements of Serial Interface
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (CK)	CLKi input cycle time	800	—	300	—	200	—	ns
t _w (CKH)	CLKi input “H” width	400	—	150	—	100	—	ns
t _w (CKL)	CLKi input “L” width	400	—	150	—	100	—	ns
t _d (C-Q)	TXDi output delay time	—	200	—	80	—	50	ns
t _h (C-Q)	TXDi hold time	0	—	0	—	0	—	ns
t _{su} (D-C)	RXDi input setup time	150	—	70	—	50	—	ns
t _h (C-D)	RXDi input hold time	90	—	90	—	90	—	ns

$i = 0$ to 2

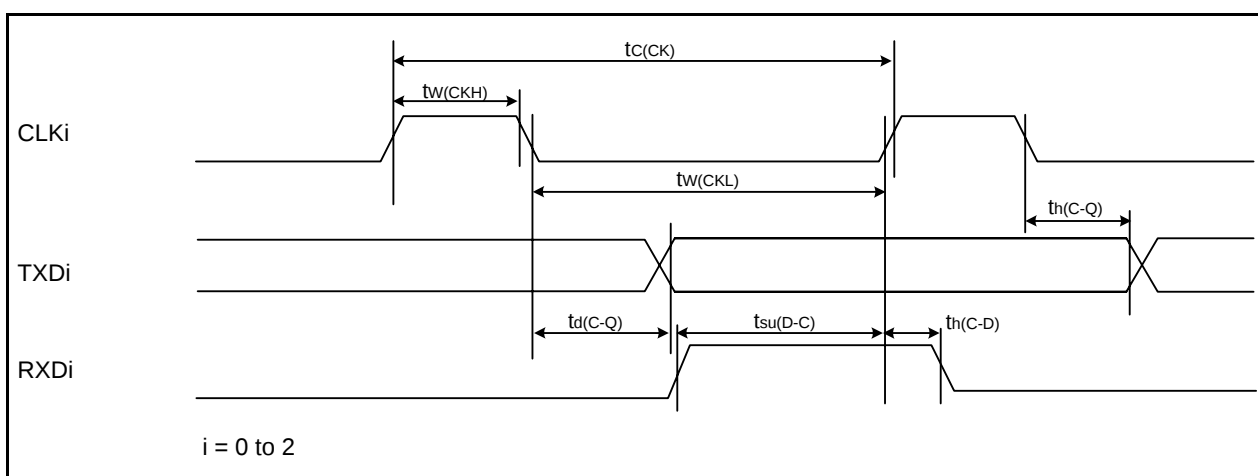


Figure 5.10 Input and Output Timing of Serial Interface

Table 5.28 Timing Requirements of External Interrupt $\overline{\text{INT}}i$ ($i = 0$ to 7) and Key Input Interrupt $\overline{\text{KLI}}i$ ($i = 0$ to 7)
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tw(INH)	$\overline{\text{INTi}}$ input “H” width, $\overline{\text{KLi}}$ input “H” width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
tw(INL)	$\overline{\text{INTi}}$ input “L” width, $\overline{\text{KLi}}$ input “L” width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

Notes:

- When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

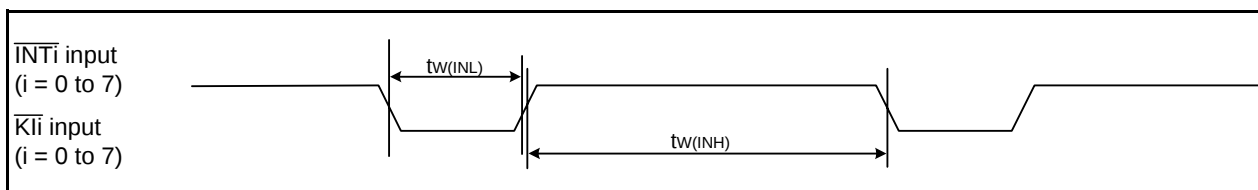


Figure 5.11 Input Timing of External Interrupt $\overline{\text{INT}}i$ and Key Input Interrupt $\overline{\text{KLI}}i$