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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	88
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l3a7cnfp-30

Email: info@E-XFL.COM

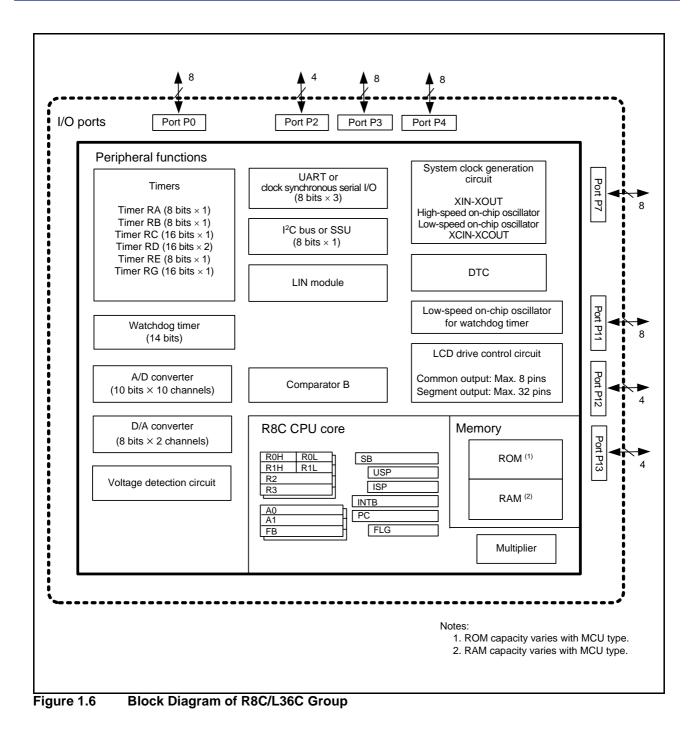
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Item	Specification
Flash Memory	<ul> <li>Programming and erasure voltage: VCC = 2.7 to 5.5 V</li> </ul>
	<ul> <li>Programming and erasure endurance: 10,000 times (data flash)</li> </ul>
	1,000 times (program ROM)
	<ul> <li>Program security: ROM code protect, ID code check</li> </ul>
	On-chip debug function
	On-board flash rewrite function
	<ul> <li>Background operation (BGO) function</li> </ul>
Operating Frequency/	f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Supply Voltage	f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)
Current Consumption	Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
	Typ. 3.6 mA (VCC = 3.0 V, f(XIN) = 10 MHz)
	Typ. 3.5 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz))
	Typ. 2 µA (VCC = 3.0 V, stop mode)
	Typ. 0.02 $\mu$ A (VCC = 3.0 V, power-off mode)
Operating Ambient Temperature	-20 to 85°C (N version)
	-40 to 85°C (D version) <sup>(1)</sup>

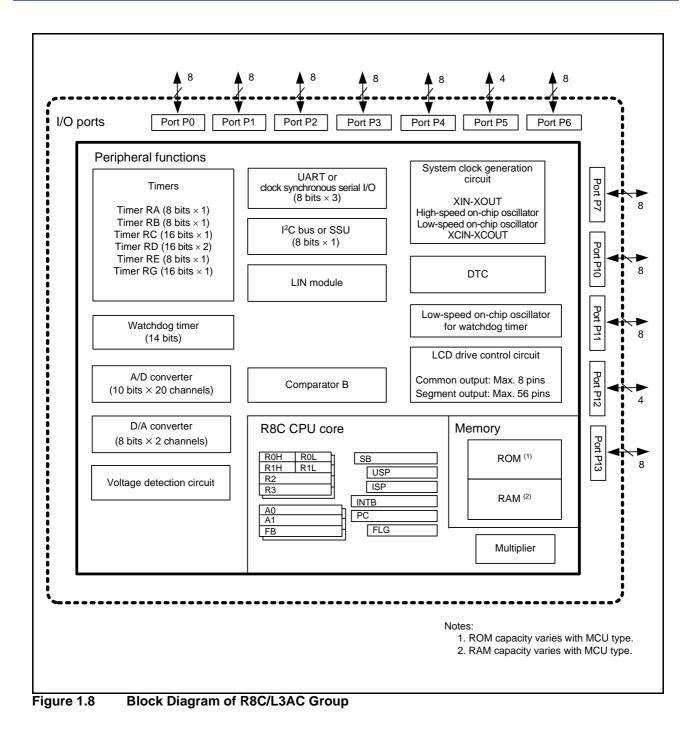
**Specifications (3)** Table 1.6

Note: 1. Specify the D version if D version functions are to be used.



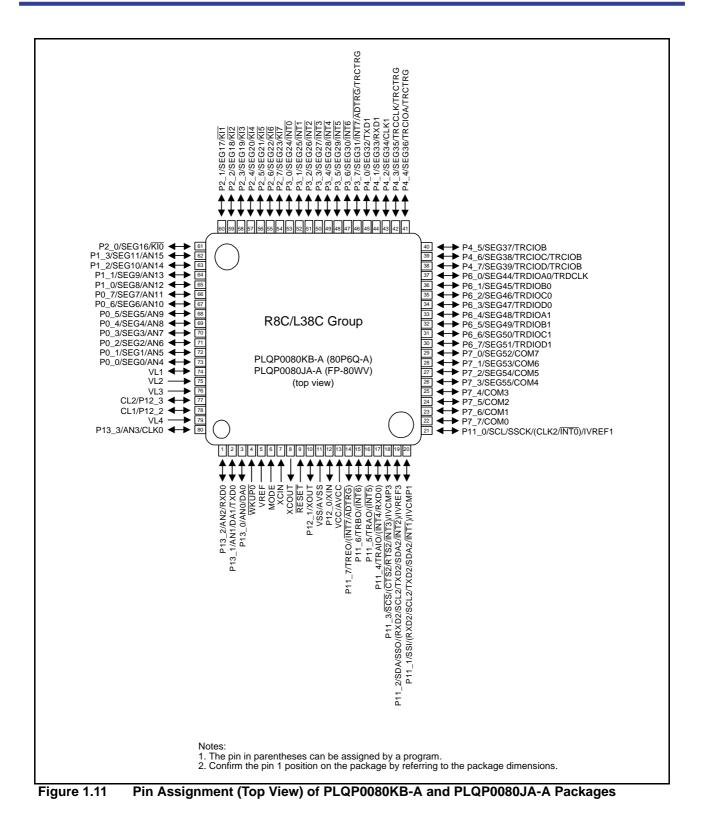














LSAC         Desc         LSAC         Pin         Port         Interrupt         Timer         Serial Interace         SSU         Pic Us         Diversity         Control Comparisor B         Control B	P	in Nun	nber				İ	I/O	Pin Functions	for Per	ipheral	Modules	
(Note 2)         Image         Image         Image         Image         Image         SSD         Low         Controverted, Comparator B         Controverted, Comparator B         Controverted, Comparator B         Controverted, SEG49           40 (42)         31         -         P6.6         TRDIOCI         -         -         BE         SEG49           42 (44)         33         -         P6.6         TRDIOCI         -         -         SEG47           42 (44)         3         -         P6.2         TRDIOCI         -         -         SEG47           42 (44)         3         -         P6.2         TRDIOCIO         -         -         SEG47           44 (48)         37         -         -         P6.2         TRDIOCIO         -         -         SEG47           45 (14)         3         -         -         P6.2         TRCIOCIO         -         -         SEG47           16 (15)         -         P6.7         TRCIOCIO         -         -         SEG47           17 (2016)         18         38         27         24         P4.4         TRCIOCIO         -         -         -         SEG39           515 (51)		1	1	1050	Control	Dent				1			LCD drive
Image: Constraint of the second of		L380	L36C	L35C	Pin	Pon	Interrupt	Timer		SSU		D/A Converter,	control
4143         32         b         PR5.5         TRDOB1         b         b         SEG48           4343         34         -         PR5.3         TRDOON         -         -         SEG48           43461         35         -         PR5.3         TRDOON         -         SEG46           41461         35         -         PR5.1         TRDOKO         -         SEG46           41697         36         -         PR5.2         TRDOKO         -         SEG46           46(48)         37         -         PS5.2         -         -         SEG41           47(49)         -         PS5.2         -         -         -         SEG43           48(50)         -         PS5.2         -         -         -         SEG43           51(51         -         PS5.2         -         -         -         SEG39           51(51         41         30         25         P4.4         TRCIOD/ TRCIOB         -         -         SEG36           51(51         41         30         25         P4.4         TRCIOK/ TRCIAG         -         SEG37           54(58)         43         32 <t< td=""><td>(Note 2)</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>interface</td><td></td><td>bus</td><td>Comparator B</td><td>circuit</td></t<>	(Note 2)								interface		bus	Comparator B	circuit
42 [44]         33         b         PE6.4         TRDIOAL         D         D         SEGAF           44 [46]         35         -         PE6.2         TRDIODO         -         -         SEGAF           44 [46]         35         -         PE6.1         TRDIOAD         -         D         SEGAF           46 [46]         37         -         -         PE6.1         TRDIOAD         -         D         SEGAF           47 [40]         -         -         PE5.1         -         PE5.2         -         -         SEGAF           48 [50]         -         -         P5.1         -         -         SEGAF           49 [51]         -         -         P5.1         -         -         SEGAF           51 [51]         38         27         22         P4.7         TRCIOB         -         D         SEGAF           51 [51]         39         28         23         P4.6         TRCIOB         -         D         SEGAF           51 [51]         30         22         P4.4         TRCIOB         -         D         SEGAF           51 [51]         41         30         25		31											
43 (46)         34          P6.3         TRDOOD           SEG47           44 (46)         35          P6_1         TRDOK0          SEG45           45 (47)         36          P6_1         TRDOK0          SEG45           46 (43)           P6_0         TRDOK0          SEG47           47 (43)           P6_5           SEG47           47 (43)           P6_0         TRDOK0          SEG47           51 (51)           P6_0         TRCIOC/          SEG47           51 (51)           P6_0         TRCIOC/           SEG39           52 (54)         39         28         23         P4_6         TRCIOC/           SEG36           53 (55)         41         30         25         P4_3         TRCIOR/           SEG36           56 (53)         43         32         27         P4_2         TRCIOR/		32											
44 461         35         P6.2         TRD/OC0         P6.2         TRD/OC0         P6.2         TRD/OR0         SEC46           46 (48)         37         P6.1         TRD/OR0         P6.1         TRD/OR0         SEC43           47 (40)         P6.2         P6.3         P6.1         TRD/OR0         P6.2         SEC43           48 (50)         P6.2         P5.3         P5.2         P6.1         P6.2         P5.2         P6.2         P6													
Image: state of the state													
46 [48]         37         Pe.0         TRDOAN TRDCA         Pe.0         SEG44           47 [49]         Pe.3         Pe.3         Pe.3         Pe.3         Pe.4         SEG43           48 [50]         Pe.7         Pe.7         Pe.7         SEG43         SEG43           50 [52]         Pe.7         Pe.7         TRCIOB         SEG43         SEG43           51 [53]         38         27         22         Pe.7         TRCIOB         SEG39           52 [54]         39         28         23         Pe.4.5         TRCIOB         SEG39           53 [55]         42         31         26         Pe.4.4         TRCIOC/ TRCIOB         SEG34         SEG35           54 [56]         41         30         25         Pe.4.4         TRCICK/ TRCICK         SEG34         SEG35           57 [57]         42         31         26         Pe.3.0         TRCTKG         SEG35           58 [60]         45         34         29         Pe.0         TRCTKG         SEG32           58 [61]         43         32         P3.7         INT7         TRCTKG         ADTRG           59 [61]         43         38         P3.6													
46         46         47         40         4         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40         40 </td <td>45 [47]</td> <td>36</td> <td></td> <td></td> <td></td> <td>P6_1</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>SEG45</td>	45 [47]	36				P6_1							SEG45
Hat [G0]       L       L       PP5_2       L       L       PS24       L       SEG41         49 [51]       L       PS_0       L       PS_0       L       SEG41         51 [53]       38       27       22       P4_7       TRCIOD/ TRCIOB       SEG39         52 [54]       39       28       23       P4_6       TRCIOD/ TRCIOB       L       SEG39         53 [55]       40       29       24       P4_5       TRCIOB       L       SEG39         54 [56]       41       30       25       P4_4       TRCIRG       L       SEG36         56 [57]       42       31       26       P4_3       TRCIRG       L       SEG36         56 [58]       43       32       27       P4_2       CLK1       SEG33       SEG34         57 [59]       44       33       28       P4_1       RXD1       SEG33       SEG33         58 [60]       45       34       29       P4_0       RXD1       SEG34       SEG34         60 [61]       46       35       P3_6       INT6       ADTRG       SEG34         60 [62]       47       36       P3_6       INT6 <td< td=""><td></td><td>37</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></td<>		37											
49 (51)       -       -       P5_1       -       P5_0       -       SEG41         50 [52]       -       -       P4_0       TRCIOD/ TRCIOB       -       SEG39         51 [53]       38       27       22       P4_6       TRCIOD/ TRCIOB       -       SEG39         52 [54]       39       28       23       P4_6       TRCIOC/ TRCIOB       -       SEG37         54 [56]       41       30       25       P4_4       TRCIOA/ TRCIAG       SEG36       SEG36         55 [57]       42       31       26       P4_3       TRCICAK TRCIAG       SEG36       SEG36         57 [59]       44       33       28       P4_1       RXD1       SEG33       SEG33         58 [60]       45       34       29       P4_0       TRCIAG       XDTRG       SEG31         59 [61]       46       35       P3_7       INT7       TRCTRG       XDTRG       SEG39         61 [63]       48       37       P3_6       INT6       SEG39       SEG39       SEG39         61 [64]       51       40       31       P3_2       INT7       CLK1       SEG32         62 [64]       49       <													
50 [52]         D         P5_0         TRCIDD         TRCIDD         SEG40           51 [53]         38         27         22         P4_7         TRCIDB         SEG39           52 [54]         39         28         23         P4_6         TRCIDB         SEG39           53 [55]         40         29         24         P4_5         TRCIDB         SEG37           54 [56]         41         30         25         P4_4         TRCIDM         SEG36           55 [57]         42         31         26         P4_3         TRCIDK         SEG34           56 [58]         43         32         27         P4_2         CLK1         SEG34           57 [59]         44         33         28         P4_1         RXD1         SEG34           59 [61]         46         35         P3_7         INT7         TRCTRG         MADRG         SEG31           60 [62]         47         36         P3_6         INT6         NADRG         SEG36           61 [63]         48         37         Image: P3_4         INT4         Image: P3_4         Image: P3_4           65 [7]         52         41         32         P3_3													
51         38         27         22         P4_7         TRCIOD TRCIOB         SEG39           52         54         39         28         23         P4_6         TRCIOB         SEG38           53         54         60         29         24         P4_6         TRCIOB         SEG37           54         56         41         30         25         P4_4         TRCIOR TRCIAG         SEG37           54         55         77         42         31         26         P4_3         TRCIAG         SEG36           55         577         42         31         26         P4_2         CLK1         SEG35           58         60         45         34         29         P4_0         TXD1         SEG32           59         61         46         35         P3_7         INT7         TRCTRG         XD1         SEG32           60         62         47         36         P3_6         INT6         ZD1         SEG32           61         63         48         37         P3_5         INT5         ZD1         SEG32           61         61         31         P3_2         INT2         ZD1 <td></td>													
51       38       27       22       P4_6       TRCIOB       C       SE339         52       40       29       24       P4_6       TRCIOB       C       SE339         54       56       41       30       25       P4_4       TRCIOB       C       SE339         54       56       41       30       25       P4_4       TRCIOB       C       SE339         55       57       42       31       26       P4_4       TRCIOB       C       SE339         56       56       33       32       27       P4_2       CLK1       SE334         57       57       44       33       28       P4_1       RXCING       SE334         59       61       46       35       P3_7       INT7       TRCTRG       M       ADTRG       SE33         60       62       47       36       P3_7       INT6       RCTRG       M       ADTRG       SE33         61631       48       37       C       P3_6       INT6       C       ADTRG       SE33         61631       49       38       C       P3_1       INT4       C       C       SE33	50 [52]					P5_0		TRAIAR					SEG40
b2 (sh)         33         28         23         P4_5         TRCIOB         Composition         SEG37           53 (s6)         40         29         24         P4_5         TRCIOB         Composition         SEG37           54 (s6)         41         30         25         P4_4         TRCIOM         Composition         SEG36           55 (s7)         42         31         26         P4_2         TRCTRG         CLK1         SEG33           65 (s1)         43         32         27         P4_2         CLK1         SEG33           58 (s0)         45         34         29         P4_0         TRCTRG         RXD1         SEG33           59 (s1)         46         35         C         P3_7         INT7         TRCTRG         ADTRG         SEG31           60 (s2)         47         36         C         P3_6         INT6         C         ADTRG         SEG31           61 (s1)         48         37         C         P3_5         INT5         C         C         ADTRG         SEG32           62 (s4)         49         38         C         P3_4         INT4         C         C         SEG22	51 [53]	38	27	22		P4_7		TRCIOB					SEG39
53 [56]       40       29       24       P4_5       TRCIOB       Image: Constraint of the	52 [54]	39	28	23		P4_6							SEG38
54 [56]         41         30         25         P4_4         TRCION TRCING         M         SEG36           55 [57]         42         31         26         P4_3         TRCCLK/ TRCTRG          SEG35           56 [58]         43         32         27         P4_2          CLK1         SEG34           57 [59]         44         33         28         P4_1         RD1         SEG33           58 [60]         45         34         29         P4.0         TXD1         SEG33           59 [61]         46         35         P3_7         INT7         TRCTRG         ADTRG         SEG31           60 [62]         47         36         P3_7         INT5         ADTRG         SEG30           61 [63]         48         37         P3_5         INT5         ADTRG         SEG28           63 [65]         50         39         30         P3_3         INT3         ADTRG         SEG28           63 [65]         50         39         30         P3_3         INT3         ADTRG         SEG26           66 [68]         54         43         34         P2_7         Ki7         ADTRG         SEG21	53 [55]	40	29	24		P4_5						1	SEG37
55 [57]       42       31       26       P4_3       TRCLK/ TRCTRG       CLK1       SEG34         56 [58]       43       32       27       P4_2       CLK1       SEG34         57 [59]       44       33       28       P4_1       RD1       SEG33         58 [60]       45       34       29       P4_0       TXD1       SEG33         58 [61]       46       35       P3_7       INT7       TRCTRG       ADTRG       SEG31         60 [62]       47       36       P3_6       INT6       ADTRG       SEG31         61 [63]       48       37       P3_5       INT5       A       ADTRG       SEG32         62 [64]       49       38       P3_4       INT4       A       A       SEG26         63 [65]       50       39       30       P3_3       INT3       A       SEG26         64 [66]       51       40       31       P3_2       INT2       A       A       SEG26         65 [67]       52       41       32       P3_1       INT7       A       A       SEG26         66 [68]       53       42       33       P2_6       Ki6		41	30	25				TRCIOA/					SEG36
66 [58]       43       32       27       P4_2       CLK1       SEG34 $57$ [59]       44       33       28       P4_1       RXD1       SEG33         58 [60]       45       34       29       P4_0       TXD1       SEG33         59 [61]       46       35       P3_7       INT7       TRCTRG       IXD1       SEG32         59 [61]       46       35       P3_6       INT6       IXD1       SEG33         60 [62]       47       36       P3_6       INT6       IXD1       SEG33         61 [63]       48       37       P3_5       INT5       IXD1       SEG29         62 [64]       49       38       P3_4       INT4       IXD1       SEG26         63 [65]       50       39       30       P3_3       INT3       IXD1       SEG26         64 [66]       51       40       31       P3_2       INT2       IXD1       SEG26         65 [67]       52       41       32       P3_1       INT1       IXD1       SEG22         66 [68]       53       42       33       P2_7       Ki7       IXD       SEG20         67 [69]	55 [57]	42	31	26	<u> </u>	P4_3		TRCCLK/					SEG35
57 [59]       44       33       28 $P4_{-1}^{-1}$ RXD1       SEG33         58 [60]       45       34       29 $P4_{-0}^{-1}$ TXCTRG       ADTRG       SEG32         59 [61]       46       35       P3_6       INT7       TRCTRG       INT6       SEG30         60 [62]       47       36       P3_6       INT6       SEG30       SEG30         61 [63]       48       37       P3_6       INT6       SEG30       SEG30         62 [64]       49       38       P3_3       INT3       SEG20       SEG27         62 [64]       51       40       31       P3_2       INT4       SEG26       SEG27         64 [66]       51       40       31       P3_2       INT3       SEG26       SEG26         66 [67]       52       41       32       P3_1       INT1       SEG26       SEG24         67 [69]       54       43       34       P2_7       Ki7       SEG27       SEG29         68 [70]       55       44       35       P2_6       Ki6       SEG27       SEG27         70 [72]       57       46       37       P2_2       Ki2	56 [58]	43	32	27		P4_2			CLK1				SEG34
58 [60]         45         34         29         P4_0         TXD1         SEG32           59 [61]         46         35         P3_7         INT7         TRCTRG         INT6         INT6         SEG31           60 [62]         47         36         P3_6         INT6         INT6         SEG30           61 [63]         48         37         P3_5         INT5         INT6         SEG29           62 [64]         49         38         P3_4         INT6         INT6         SEG29           63 [65]         50         39         30         P3_3         INT3         INT6         INT6         SEG27           64 [66]         51         40         31         P3_2         INT2         INT6         SEG26           65 [67]         52         41         32         P3_1         INT6         SEG26           66 [68]         53         42         33         P3_0         INT6         SEG23           66 [70]         55         44         35         P2_6         Kif6         SEG20           69 [71]         56         45         36         P2_2.6         Kif6         SEG20         SEG20           <													
59 [61]       46       35       P3_7       INT7       TRCTRG       ADTRG       SEG31         60 [62]       47       36       P3_6       INT6        SEG30       SEG30         61 [63]       48       37       P3_5       INT6        SEG30       SEG30         62 [64]       49       38       P3_4       INT4        SEG28       SEG28         63 [65]       50       39       30       P3_3       INT3        SEG27         64 [66]       51       40       31       P3_2       INT2        SEG26         65 [67]       52       41       32       P3_1       INT1         SEG25         66 [68]       53       42       33       P3_0       INT0        SEG23         68 [70]       55       44       35       P2_6       Ki6        SEG20         70 [72]       57       46       37       P2_4       Ki4         SEG30         71 [73]       58        P2_2       Ki2        SEG40       SEG41         71 [73]       58        P2_2,0<		45	34			P4_0			TXD1				
61 [63]       48       37       Image: constraint of the second secon		46	35				INT7	TRCTRG				ADTRG	
61 [63]       48       37       L       P3_5 $\overline{INT5}$ L       L       SEG29         62 [64]       49       38       P3_4 $\overline{INT4}$ L       L       SEG28         63 [65]       50       39       30       P3_3 $\overline{INT3}$ L       L       SEG27         64 [66]       51       40       31       P3_2 $\overline{INT2}$ L       L       SEG26         65 [67]       52       41       32       P3_1 $\overline{INT1}$ L       L       SEG26         66 [68]       53       42       33       P3_0 $\overline{INT0}$ L       L       SEG26         66 [69]       54       43       34       P2_7 $\overline{Ki7}$ L       L       SEG26         66 [69]       54       43       34       P2_7 $\overline{Ki7}$ L       L       SEG27         68 [70]       55       44       35       P2_6 $\overline{Ki6}$ L       L       SEG29         69 [71]       56       45       36       P2_5 $\overline{Ki5}$ L       L       SEG29         71 [73]       58       Z       2       P2	60 [62]	47	36			P3_6	INT6						SEG30
63 [65]       50       39       30       P3_3 $\overline{INT3}$ Image: Market Ma	61 [63]	48	37			P3_5							SEG29
64 [66]       51       40       31 $P3_2$ $\overline{INT2}$ $INT2$ $INT0$ $IINT0$	62 [64]	49	38			P3_4	INT4						SEG28
65 [67]       52       41       32       P3_1       INT1       Image: constraint of the second seco	63 [65]	50	39	30		P3_3	INT3						
66 [68]       53       42       33       P3_0       INTO       INTO       SEG24         67 [69]       54       43       34       P2_7       KI7       INTO       SEG23         68 [70]       55       44       35       P2_6       KI6       Into       SEG22         69 [71]       56       45       36       P2_5       KI5       Into       Into       SEG21         70 [72]       57       46       37       P2_4       KI4       Into       Into       SEG20         71 [73]       58       Into       P2_3       KI3       Into       Into       SEG10         72 [74]       59       Into       P2_2       KI2       Into       Into       SEG18         73 [75]       60       Into       P2_0       KI0       Into       Into       SEG18         74 [76]       61       Into       P1_6       Into       Into       SEG18         76 [77]       Into       P1_6       Into       Into       SEG18         76 [78]       Into       P1_6       Into       Into       SEG13         78 [80]       Into       P1_4       Into       Into       Into	64 [66]	51	40	31		P3_2	INT2						SEG26
$67$ [69]544334 $P2_{-7}$ $\overline{K17}$ $\overline{K10}$ $K1$		52	41	32			INT1						
68 [70]       55       44       35       P2_6       Kin       Kin       Kin       Kin       Kin         69 [71]       56       45       36       P2_5       Kis       Kis       SEG21         70 [72]       57       46       37       P2_4       Kis       Kis       SEG20         71 [73]       58       Image: Constraint of the second se		53	42	33			<b>INTO</b>						
69 [71]       56       45       36       P2_5       KI5       Image: constraint of the second secon							KI7						
70 [72]       57       46       37       P2_4       Kla       All       SEG20         71 [73]       58       Image: Constraint of the stress of		55					KI6						
71 [73]       58       P2_3       KI3       SEG19         72 [74]       59       P2_2       KI2       SEG18         73 [75]       60       P2_1       KI1       SEG17         74 [76]       61       P2_0       KI0       SEG16         75 [77]       P2_0       KI0       SEG16         75 [77]       P1_7       SEG16       SEG14         77 [79]       P1_6       SEG12         78 [80]       P1_4       SEG1         80 [82]       63       P1_1         81 [83]       64       P1_0         91_0       P1_0       AN13         82 [84]       65       P1_07													
$72 [74]$ $59$ $P2_2$ $\overline{Kl2}$ $Rectar Rectar Rect$			46	37		_							
$73 [75]$ $60$ $P2_{-1}$ $\overline{Kl1}$ SEG17 $74 [76]$ $61$ $P2_{-0}$ $\overline{Kl0}$ SEG16 $75 [77]$ $P1_{-7}$ $P1_{-7}$ SEG16 $76 [78]$ $P1_{-6}$ $P1_{-6}$ $SEG14$ $77 [79]$ $P1_{-5}$ $P1_{-6}$ $SEG13$ $78 [80]$ $P1_{-4}$ $SEG12$ $SEG12$ $79 [81]$ $62$ $P1_{-13}$ $AN15$ $SEG11$ $80 [82]$ $63$ $P1_{-1}$ $AN14$ $SEG10$ $81 [83]$ $64$ $P1_{-1}$ $AN13$ $SEG9$ $82 [84]$ $65$ $P1_{-0}$ $AN11$ $AN11$ $SEG1$													
74 [76]       61       P2_0       KI0       SEG16         75 [77]       P1_7       SEG15         76 [78]       P1_6       SEG14         77 [79]       P1_5       SEG13         78 [80]       P1_4       SEG12         79 [81]       62       P1_2       AN15         80 [82]       63       P1_2       AN14         81 [83]       64       P1_0       AN12         83 [85]       66       47       38       P0_7													
75 [77]       P1_7       SEG15         76 [78]       P1_6       SEG14         77 [79]       P1_5       SEG13         78 [80]       P1_4       SEG12         79 [81]       62       P1_3       AN15         80 [82]       63       P1_1       AN14         81 [83]       64       P1_0       AN13         82 [84]       65       P1_0       AN11 (3)													
76 [78]       P1_6       SEG14         77 [79]       P1_5       SEG13         78 [80]       P1_4       SEG12         79 [81]       62       P1_3       AN15         80 [82]       63       P1_2       AN14         81 [83]       64       P1_0       AN13         82 [84]       65       P1_0       AN12         83 [85]       66       47       38       P0_7		61					KI0						
77 [79]         P1_5         SEG13           78 [80]         P1_4         SEG12           79 [81]         62         P1_3         AN15         SEG11           80 [82]         63         P1_2         AN14         SEG10           81 [83]         64         P1_1         AN13         SEG9           82 [84]         65         P1_0         AN12         SEG8           83 [85]         66         47         38         P0_7         AN11 (3)         SEG7						_							
78 [80]         P1_4         SEG12           79 [81]         62         P1_3         AN15         SEG11           80 [82]         63         P1_2         AN14         SEG10           81 [83]         64         P1_1         AN13         SEG9           82 [84]         65         P1_0         AN12         SEG8           83 [85]         66         47         38         P0_7         AN11 (3)         SEG7						_							
79 [81]         62         P1_3         AN15         SEG11           80 [82]         63         P1_2         AN14         SEG10           81 [83]         64         P1_1         AN13         SEG9           82 [84]         65         P1_0         AN12         SEG8           83 [85]         66         47         38         P0_7         AN11 (3)         SEG7						_							
80 [82]         63         P1_2         AN14         SEG10           81 [83]         64         P1_1         AN13         SEG9           82 [84]         65         P1_0         AN12         SEG8           83 [85]         66         47         38         P0_7         AN11 (3)         SEG7		62				_				+		AN15	
81 [83]         64         P1_1         AN13         SEG9           82 [84]         65         P1_0         AN12         SEG8           83 [85]         66         47         38         P0_7         AN11 <sup>(3)</sup> SEG7													
82 [84]         65         P1_0         AN12         SEG8           83 [85]         66         47         38         P0_7         AN11 <sup>(3)</sup> SEG7						_			<u> </u>				
83 [85] 66 47 38 P0_7 AN11 <sup>(3)</sup> SEG7						_							
		66	47	38		_							
84 [86] 67 48 39 P0_6 AN10 <sup>(3)</sup> SEG6	84 [86]	67	48	39		 P0_6						AN10 <sup>(3)</sup>	SEG6

Table 1.12Pin Name Information by Pin Number (2)

Notes:

1. The pin in parentheses can be assigned by a program.

2. The number in brackets indicates the pin number for the 100P6F package.

3. Pins AN10 and AN11 are not available in the R8C/L35C, and R8C/L36C Groups.



Pin Number						I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C	Control Pin	Port	Interrupt	Timer	Serial Interface	SSU	I <sup>2</sup> C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
85 [87]	68	49	40		P0_5						AN9	SEG5
86 [88]	69	50	41		P0_4						AN8	SEG4
87 [89]	70	51	42		P0_3						AN7	SEG3
88 [90]	71	52	43		P0_2						AN6	SEG2
89 [91]	72	53	44		P0_1						AN5	SEG1
90 [92]	73	54	45		P0_0						AN4	SEG0
91 [93]	74	55	46									VL1
92 [94]	75	56	47									VL2
93 [95]	76	57										VL3
94 [96]	77	58	48		P12_3							CL2
95 [97]	78	59	49		P12_2							CL1
96 [98]	79	60	50									VL4
97 [99]					P13_7		TRGCLKB				AN19	
98 [100]					P13_6		TRGIOB				AN18	
99 [1]					P13_5		TRGCLKA				AN17	
100 [2]					P13_4		TRGIOA				AN16	

Pin Name Information by Pin Number (3) Table 1.13

Notes:

The pin in parentheses can be assigned by a program.
 The number in brackets indicates the pin number for the 100P6F package.



### 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

### 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

### 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

#### 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

### 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

### 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

#### 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

### 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



Address	Register	Symbol	After Reset
02C0h	rogiotor	Cymbol	71101 110001
02C1h			
02C2h			
02C3h			
02C4h			
02C5h			
02C6h			
02C7h			
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D0h			
02D1h			
02D2h 02D3h			
02D3h 02D4h			
02D411 02D5h			
02D5h 02D6h			
02D6n 02D7h			
02D7h 02D8h			
02D8h			
02D9h 02DAh			
02DAn 02DBh			
02DBh 02DCh			
02DDh			
02DDh 02DEh			
02DEn 02DFh			
02DFn 02E0h			
02E1h			
02E2h 02E3h			
02E31			
02E411 02E5h			
02E5h			
02E011			
02E7h			
02E8h 02E9h			
02E90			
02EAh			
02EBh 02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			

Table 4.12 SF	R Information (12) <sup>(1)</sup>
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X: Undefined Note: 1. Blank spaces are reserved. No access is allowed.



			16 D .
Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h	1		XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h	-		XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
		516516	
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
		D700/0	
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
	-		
2CC3h			XXh
2CC4h			XXh
2CC5h	7		XXh
2CC6h	1		XXh
	-		
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh	-		XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
	DTC CONTO Data To	DICDI6	
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h	-		XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh	1		XXh
	4		
2CDBh			XXh
2CDCh			XXh
2CDDh	1		XXh
	-		
2CDEh	4		XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
	4		
2CE2h			XXh
2CE3h			XXh
2CE4h	1		XXh
	4		
2CE5h			XXh
2CE6h			XXh
2CE7h	1		XXh
	DTO Occuted Data 04	DTODO1	
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh	1		XXh
2CEBh	-		
			XXh
2CECh			XXh
2CEDh	1		XXh
2CEEh	1		XXh
	-		
2CEFh			XXh
X: Undefined	J	I	1.0

SFR Information (15)<sup>(1)</sup> Table 4.15

X: Undefined Note: 1. Blank spaces are reserved. No access is allowed.



#### 5.2 **Recommended Operating Conditions**

Recommended Operating Conditions (VCC = 1.8 to 5.5 V and Topr = -20 to  $85^{\circ}$ C (N version) / -40 to  $85^{\circ}$ C (D version), unless Table 5.2 otherwise specified.)

Symbol		D	arameter		Conditions		Standard		Unit
Symbol		F	arameter		Conditions	Min.	Тур.	Max.	Unit
Vcc/AVcc	Supply voltage					1.8		5.5	V
Vss/AVss						—	0	—	V
Viн	Input "H" voltage	Other th	nan CMOS ii	nput	$4.0~V \leq Vcc \leq 5.5~V$	0.8 Vcc		Vcc	V
					$2.7~V \leq Vcc < 4.0~V$	0.8 Vcc		Vcc	V
					$1.8 \text{ V} \leq \text{Vcc} < 2.7 \text{ V}$	0.9 Vcc		Vcc	V
		CMOS	Input level	Input level selection	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0.5 Vcc	_	Vcc	V
		input	switching	: 0.35 Vcc	$2.7~V \leq Vcc < 4.0~V$	0.55 Vcc	_	Vcc	V
			function		$1.8~V \leq Vcc < 2.7~V$	0.65 Vcc		Vcc	V
			(I/O port)	Input level selection	$4.0~V \leq Vcc \leq 5.5~V$	0.65 Vcc		Vcc	V
				: 0.5 Vcc	$2.7~V \leq Vcc < 4.0~V$	0.7 Vcc	_	Vcc	V
					$1.8 \text{ V} \leq \text{Vcc} < 2.7 \text{ V}$	0.8 Vcc	_	Vcc	V
				Input level selection	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0.85 Vcc	_	Vcc	V
				: 0.7 Vcc	$2.7~V \leq Vcc < 4.0~V$	0.85 Vcc	_	Vcc	V
					$1.8 \text{ V} \leq \text{Vcc} < 2.7 \text{ V}$	0.85 Vcc	_	Vcc	V
VIL	Input "L" voltage	Other th	nan CMOS ii	nput	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0	_	0.2 Vcc	V
					$2.7~V \leq Vcc < 4.0~V$	0	_	0.2 Vcc	V
					$1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$	0	_	0.05 Vcc	V
		CMOS	Input level	Input level selection	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0		0.2 Vcc	V
		input	switching	: 0.35 Vcc	$2.7~V \leq Vcc < 4.0~V$	0	_	0.2 Vcc	V
			function		$1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$	0	_	0.2 Vcc	V
			(I/O port)	Input level selection	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0		0.4 Vcc	V
				: 0.5 Vcc	$2.7~V \leq Vcc < 4.0~V$	0		0.3 Vcc	V
					$1.8~V \leq Vcc < 2.7~V$	0	_	0.2 Vcc	V
				Input level selection	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0		0.55 Vcc	V
				: 0.7 Vcc	$2.7~V \leq Vcc < 4.0~V$	0	_	0.45 Vcc	V
					$1.8~V \leq Vcc < 2.7~V$	0	_	0.35 Vcc	V
IOH(sum)	Peak sum output "H" current	Sum of	all pins IOH(p	beak)		_		-160	mA
IOH(sum)	Average sum output "H" current	Sum of	all pins IOH(a	avg)		_		-80	mA
IOH(peak)	Peak output "H"	Port P1	0, P11 <sup>(2)</sup>			_	_	-40	mA
	current	Other p				_	_	-10	mA
IOH(avg)	Average output		0, P11 <sup>(2)</sup>			_		-20	mA
	"H" current <sup>(1)</sup>	Other p				_		-5	mA
IOL(sum)	Peak sum output		all pins IOL(p	eak)		_		160	mA
	"L" current								
IOL(sum)	Average sum output "L" current		all pins IOL(a	ivg)			_	80	mA
IOL(peak)	Peak output "L"		0, P11 <sup>(2)</sup>				—	40	mA
	current	Other p				—		10	mA
IOL(avg)	Average output		0, P11 <sup>(2)</sup>			—	—	20	mA
	"L" current (1)	Other p	ins			—	_	5	mA
f(XIN)	XIN clock input of	scillation	frequency		$2.7 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	_	_	20	MHz
					$1.8~V \leq Vcc < 2.7~V$	—		5	MHz
f(XCIN)	XCIN clock input	oscillatio	n frequency		$1.8 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	—	32.768	50	kHz
fOCO40M	When used as the timer RG <sup>(3)</sup>	e count s	ource for tim	ner RC, timer RD, or	$2.7 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	32		40	MHz
fOCO-F	fOCO-F frequenc	у			2.7 V ≤ Vcc ≤ 5.5 V	_	_	20	MHz
-		•			$1.8 \text{ V} \leq \text{Vcc} < 2.7 \text{ V}$	_	_	5	MHz
_	System clock free	uencv			$2.7 V \le Vcc \le 5.5 V$	_		20	MHz
	_,				$1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$	_	_	5	MHz
f(BCLK)	CPU clock freque	ncv			$2.7 V \le Vcc \le 5.5 V$			20	MHz
	2. 2 5.0000 10900				$1.8 V \le Vcc < 2.7 V$	_		5	MHz

Notes:

The average output current indicates the average value of current measured during 100 ms. 1.

This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive 2. capacity is set to Low, the value of any other pin applies. fOCO40M can be used as the count source for timer RC, timer RD, or timer RG in the range of Vcc = 2.7 V to 5.5V.

3.

Cumbal	Parameter	Conditions		Unit			
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
—	Program/erase endurance (1)		1,000 (2)		—	times	
—	Byte program time		—	80	500	μS	
—	Block erase time		—	0.3	—	S	
td(SR-SUS)	Time delay from suspend request until suspend		_	—	5 + CPU clock × 3 cycles	ms	
—	Interval from erase start/restart until following suspend request		0	—	—	ms	
—	Time from suspend until erase restart		_	—	30+CPU clock × 1 cycle	μS	
td(CMDRST- READY)	Time from when command is forcibly terminated until reading is enabled		_	—	30+CPU clock × 1 cycle	μS	
—	Program, erase voltage		2.7		5.5	V	
—	Read voltage		1.8	—	5.5	V	
—	Program, erase temperature		0	—	60	°C	
—	Data hold time <sup>(6)</sup>	Ambient temperature = 55°C	20	—	—	year	

## Table 5.6Flash Memory (Program ROM) Characteristics<br/>(Vcc = 2.7 to 5.5 V and Topr = 0 to 60°C, unless otherwise specified.)

Notes:

1. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).

3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

6. The data hold time includes time that the power supply is off or the clock is not supplied.



# Table 5.8Voltage Detection 0 Circuit Characteristics<br/>(Vcc = 1.8 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless<br/>otherwise specified.)

Cumbal	Parameter	Condition		Unit		
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
Vdet0	Voltage detection level Vdet0_0 <sup>(1)</sup>		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)		3.55	3.80	4.05	V
_	Voltage detection 0 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V		1.5		μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts <sup>(2)</sup>		—	—	100	μS

Notes:

1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

3. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

#### Table 5.9 Voltage Detection 1 Circuit Characteristics

(Vcc = 1.8 to 5.5 V and Topr = $-20$ to $85^{\circ}$ C (N version) / $-40$ to $85^{\circ}$ C (D version), unless
otherwise specified.)

Cumhol	Parameter	Condition		Unit		
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
Vdet1	Voltage detection level Vdet1_0 <sup>(1)</sup>	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 <sup>(1)</sup>	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 <sup>(1)</sup>	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 <sup>(1)</sup>	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 <sup>(1)</sup>	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 <sup>(1)</sup>	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 <sup>(1)</sup>	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 <sup>(1)</sup>	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A <sup>(1)</sup>	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B <sup>(1)</sup>	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C <sup>(1)</sup>	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E <sup>(1)</sup>	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	At the falling of Vcc	4.20	4.45	4.75	V
_	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	_	0.07	_	V
		Vdet1_6 to Vdet1_F selected	_	0.10	—	V
—	Voltage detection 1 circuit response time <sup>(2)</sup>	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	—	60	150	μS
_	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts $^{\rm (3)}$		—	—	100	μS

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.

2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.

3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

# Table 5.10Voltage Detection 2 Circuit Characteristics<br/>(Vcc = 1.8 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless<br/>otherwise specified.)

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Unit
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time <sup>(1)</sup>	At the falling of Vcc from $5 \text{ V to } (\text{Vdet2}_0 - 0.1) \text{ V}$		20	150	μS
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	_	1.7		μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts <sup>(2)</sup>		_	—	100	μS

Notes:

1. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.

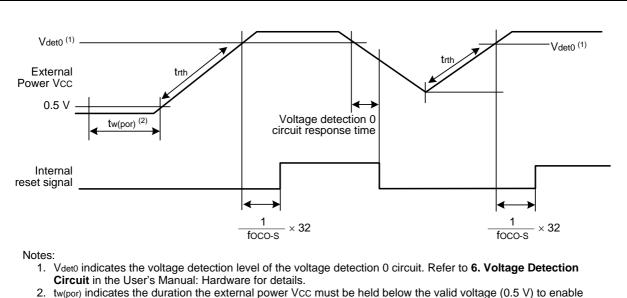
2. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

# Table 5.11 Power-on Reset Circuit Characteristics <sup>(1)</sup> (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Unit		
	Falanielei	Condition	Min.	Тур.	Max.	Offic
trth	External power Vcc rise gradient		0		50000	mV/msec

Note:

1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



 tw(por) indicates the duration the external power VCC must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain tw(por) for 1 ms or more.

Figure 5.3

**Power-on Reset Circuit Characteristics** 



# Table 5.12High-speed On-Chip Oscillator Circuit Characteristics<br/>(Vcc = 1.8 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless<br/>otherwise specified.)

Symbol	Parameter	Condition		Unit		
	Falameter	Condition	Min.	Max.		
—	High-speed on-chip oscillator frequency after reset	$\label{eq:VCC} \begin{array}{l} Vcc = 1.8 \ V \ to \ 5.5 \ V \\ -20^{\circ}C \leq T_{opr} \leq 85^{\circ}C \end{array}$	38.4	40	41.6	MHz
		Vcc = 1.8 V to 5.5 V −40°C ≤ Topr ≤ 85°C	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into	$\label{eq:Vcc} \begin{array}{l} Vcc = 1.8 \ V \ to \ 5.5 \ V \\ -20^{\circ}C \leq T_{opr} \leq 85^{\circ}C \end{array}$	35.389	36.864	38.338	MHz
	the FRA1 register and the FRA5 register correction value into the FRA3 register <sup>(1)</sup>	$\label{eq:VCC} \begin{array}{l} Vcc = 1.8 \ V \ to \ 5.5 \ V \\ -40^{\circ}C \leq T_{opr} \leq 85^{\circ}C \end{array}$	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	30.72	32	33.28	MHz
	the FRA1 register and the FRA7 register correction value into the FRA3 register	$\label{eq:Vcc} \begin{array}{l} Vcc = 1.8 \ V \ to \ 5.5 \ V \\ -40^{\circ}C \leq T_{opr} \leq 85^{\circ}C \end{array}$	30.40	32	33.60	MHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	0.5	3	ms
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	_	400	—	μΑ

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

# Table 5.13Low-speed On-Chip Oscillator Circuit Characteristics<br/>(Vcc = 1.8 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless<br/>otherwise specified.)

Symbol	Parameter	Condition		Unit			
Symbol	Falditietei	Condition	Min.	Тур.	Max.	Onit	
fOCO-S	Low-speed on-chip oscillator frequency		112.5	125	137.5	kHz	
—	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	—	30	100	μS	
	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	_	3	—	μΑ	
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz	
	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	30	100	μs	
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	2	—	μΑ	

## Table 5.14 Power Supply Circuit Characteristics

#### (Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = $25^{\circ}$ C, unless otherwise specified.)

Symbol	Parameter	Condition		Unit		
Symbol	Falanelei	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during		_	—	2000	μS
	power-on <sup>(1)</sup>					

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.



		•			•		-							-		
			0		00	le lue		Condition			S	tanda	rd			
Symbol Parameter			Ci	illation rcuit	On-C Oscilla	ator	CPU Clock	Low-Power- Consumption	(	Other	Min.	Тур.	Max.	Unit		
			(2)	XCIN	High-Speed (fOCO-F)	Speed		Setting				(3)				
lcc	Power supply	High- speed	20 MHz	Off	Off	125 kHz	No division	—			—	7.0	15	mΑ		
	current (1)	clock	16	Off	Off	125	No	—			-	5.6	12.5	mA		
		mode	MHz 10	Off	Off	kHz 125	division No	_			_	3.6	_	mA		
			MHz			kHz	division									
			20 MHz	Off	Off	125 kHz	Divide- by-8	—			-	3.0	_	mA		
			16 MHz	Off	Off	125 kHz	Divide- by-8	—			-	2.2	—	mA		
			10	Off	Off	125	Divide-	_			-	1.5	—	mA		
		High-	MHz Off	Off	20 MHz	kHz 125	by-8 No	_			_	7.0	15	mA		
		speed				kHz	division						10			
		on-chip oscillator	Off	Off	20 MHz	125 kHz	Divide- by-8	—			-	3.0	_	mA		
		mode	Off	Off	4 MHz	125 kHz	Divide-	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			_	1	-	mA		
		Low- speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide- by-8	FMR27 = 1 VCA20 = 0			-	90	400	μΑ		
		Low- speed	Off	32 kHz	Off	Off	No	FMR27 = 1 VCA20 = 0			-	100	400	μA		
		clock	Off	32	Off	Off	No	FMSTP = 1	Flash memory off		—	55	-	μA		
		mode Wait	Off	kHz Off	Off	125	division	VCA20 = 0 VCA27 = 0	Program operation of While a WAIT instru-		_	15	100	μA		
		mode				kHz		VCA26 = 0 VCA25 = 0 VCA20 = 1	Peripheral clock ope	eration				-		
			Off	Off	Off	125 kHz	_	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instru Peripheral clock off	ction is executed	_	4	90	μA		
			Off	32 kHz	Off	Off	-	VCA27 = 0 VCA26 = 0	While a WAIT instruction is executed	LCD drive control circuit <sup>(4)</sup>	-	7	—	μA		
				1412				VCA25 = 0 VCA20 = 1	Peripheral clock off	When external division						
								CM02 = 1	Timer RE operation in real-time clock mode	resistors are used LCD drive control	_	12	_	μA		
			I							CM01 = 0		circuit <sup>(5)</sup> When the internal voltage multiplier is used				
			Off	32 kHz	Off	Off	_	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instru Peripheral clock off Timer RE operation	ction is executed in real-time clock mode	—	3.5	1	μA		
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2.0	5.0	μA		
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0	Topr = 85°C Peripheral clock off		—	15		μA		
		Power-	Off	Off	Off	Off		CM10 = 1	Topr = 25°C		<u> </u>	0.02	0.2			
		off mode	Off	Off	Off	Off	_	_	Topr = $85^{\circ}C$		=	0.02	- 0.2	μA μA		

#### **Table 5.18** DC Characteristics (2) [4.0 V $\leq$ Vcc $\leq$ 5.5 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Notes:

1. 2. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.

XIN is set to square wave input.

Vcc = 5.0 V 3.

VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment 4.

and common output pins are open. The standard value does not include the current that flows through external division resistors. 5. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55

are selected, and segment and common output pins are open.



Symbol	Pa	rameter	Condition	St	andard		Unit
Symbol	га	lameter	Condition	Min.	Тур.	Max.	Onit
Vон	Output "H" voltage	Port P10, P11 (1)	Юн = -2 mA	Vcc - 0.5	_	Vcc	V
		Other pins	Iон = -1 mA	Vcc - 0.5	_	Vcc	V
		XOUT	Іон = -200 μА	1.0	_	_	V
Vol	Output "L" voltage	Port P10, P11 <sup>(1)</sup>	IOL = 2 mA			0.5	V
		Other pins	IOL = 1 mA	_	_	0.5	V
		XOUT	ΙΟL = 200 μΑ	_	_	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT2, INT3, INT4, INT5, INT6, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOC1, TRDIOD1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRGCLKA, TRGCLKB, TRGIOA, TRGIOB, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO RESET, WKUP0		0.05	0.4	1	V 
Ін	Input "H" current		VI = 1.8 V, Vcc = 1.8 V	_	_	4.0	μA
IIL	Input "L" current		VI = 0 V, Vcc = 1.8 V			-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, VCC = 1.8 V	60	160	420	μA kΩ
Rfxin	Feedback resistance	XIN		_	0.3	_	MΩ
Rfxcin	Feedback resistance	XCIN		—	14	—	MΩ
Vram	RAM hold voltage		During stop mode	1.8	_	_	V

## Table 5.21DC Characteristics (5) [1.8 V $\leq$ Vcc < 2.7 V]<br/>(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.



l		Condition									Standa			
Symbol	Parameter		Cir	llation cuit	On-C Oscilla	ator	CPU	Low-Power- Consumption	(	Other	Min.	Тур.	Max.	Unit
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low- Speed	Clock	Setting				(3)		
lcc	Power supply	High- speed	5 MHz	Off	Off	125 kHz	No division	—				2.2		mA
	current (1)	clock mode	5	Off	Off	125	Divide-	—			—	0.8	_	mA
		High-	MHz Off	Off	5 MHz	kHz 125	by-8 No	_			-	2.5	10	mA
		speed on-chip	Off	Off	5 MHz	kHz 125	division Divide-					1.7		mA
		oscillator mode		-	-	kHz	by-8							
		mode	Off	Off	4 MHz	125 kHz	Divide- by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			_	1	_	mA
		Low- speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide- by-8	FMR27 = 1 VCA20 = 0			—	90	300	μA
		Low- speed	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			-	90	400	μA
		clock mode	Off	32	Off	Off	No	FMSTP = 1	Flash memory off	DAM	—	45	_	μΑ
		Wait	Off	kHz Off	Off	125		VCA20 = 0 VCA27 = 0	Program operation of While a WAIT instru-		_	15	90	μA
	्र	mode				kHz		VCA26 = 0 VCA25 = 0 VCA20 = 1	Peripheral clock ope					
			Off	Off	Off	125 kHz	_	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instru Peripheral clock off	ction is executed	_	4	80	μΑ
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock off	LCD drive control circuit <sup>(4)</sup> When external division resistors are used	_	4		μA
								CM02 = 1 CM01 = 0	Timer RE operation in real-time clock mode	LCD drive control circuit <sup>(5)</sup> When the internal voltage multiplier is used	_	11		μA
			Off	32 kHz	Off	Off	_	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instru Peripheral clock off Timer RE operation	ction is executed in real-time clock mode	_	3.5		μA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2.0	5.0	μA
			Off	Off	Off	Off	_	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off			13	_	μΑ
		Power- off mode	Off	Off Off	Off Off	Off Off	_	—	Topr = 25°C		—	0.02	0.2	μA
		on mode	Off	Off	Off	Off	—	—	Topr = 85°C		-	0.3	—	μA

#### **Table 5.22** DC Characteristics (6) [1.8 V $\leq$ Vcc < 2.7 V] (Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.)

Notes:

Vcc = 1.8 V to 2.7 V, single chip mode, output pins are open, and other pins are Vss. 1.

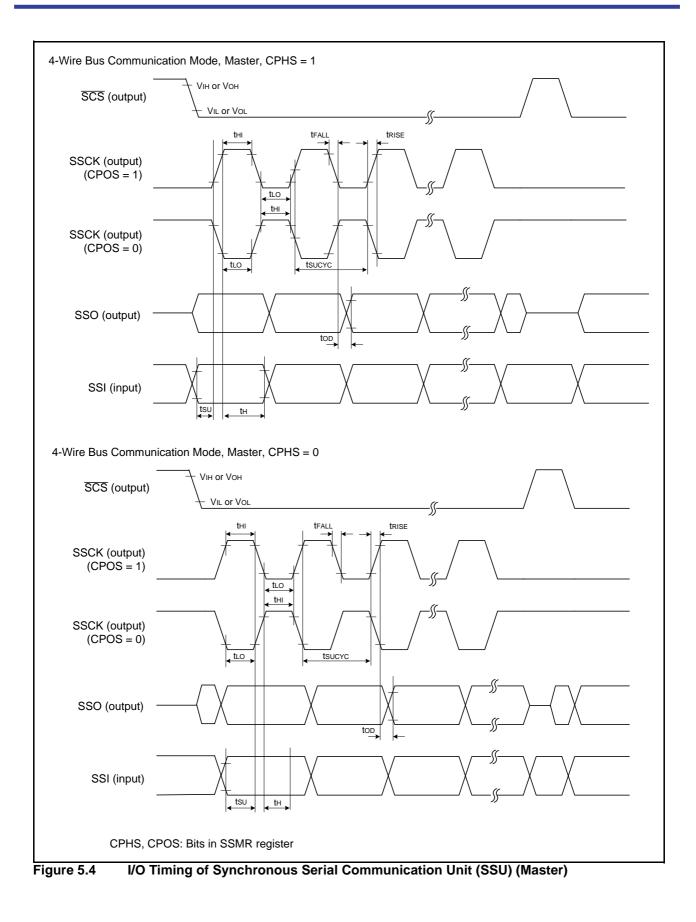
2. XIN is set to square wave input.

3. Vcc = 2.2 V

4. VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55

5. are selected, and segment and common output pins are open.





RENESAS

