Renesas Electronics America Inc - R5F2L3ACCNFA#U0 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	88
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l3accnfa-u0

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Table 1.2 lists the Programmable I/O Ports Provided for Each Group, and Table 1.3 lists the LCD Display Function Pins Provided for Each Group. Figures 1.9 to 1.13 show the Pin Assignment for Each Group, and Tables 1.7 to 1.10 list Product Information.
The explanations in the chapters which follow apply to the R8C/L3AC Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/L35C Group	R8C/L36C Group	R8C/L38C Group	R8C/L3AC Group
I/O Ports	Programmable I/O ports	41 pins	52 pins	68 pins	88 pins
	High current drive ports	5 pins	8 pins	8 pins	16 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	8 pins	8 pins	8 pins
	Key input interrupt pins	4 pins	4 pins	8 pins	8 pins
Timer RA	Timer RA output pin	None	1 pin	1 pin	1 pin
Timer RB	Timer RB output pin	None	1 pin	1 pin	1 pin
Timer RD	Timer RD I/O pin	None	None	8 pins	8 pins
Timer RE	Timer RE output pin	None	1 pin	1 pin	1 pin
Timer RG	Timer RG I/O pin	None	None	None	2 pins
	Timer RG output pin	None	None	None	2 pins
A/D Converter	Analog input pin	10 pins	10 pins	16 pins	20 pins
LCD Drive Control Circuit	LCD power supply	3 pins (VL1, VL2, VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)
	Common output pins	Max. 4 pins	Max. 8 pins	Max. 8 pins	Max. 8 pins
	Segment output pins	Max. 24 pins	Max. 32 pins	Max. 48 pins	Max. 56 pins
Packages		52-pin LQFP	64-pin LQFP	80-pin LQFP	100-pin LQFP/ 100-pin QFP

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
Refer to **Tables 1.11 to 1.13, Pin Name Information by Pin Number**, for details.

1.1.3 Specifications

Tables 1.4 to 1.6 list the Specifications.

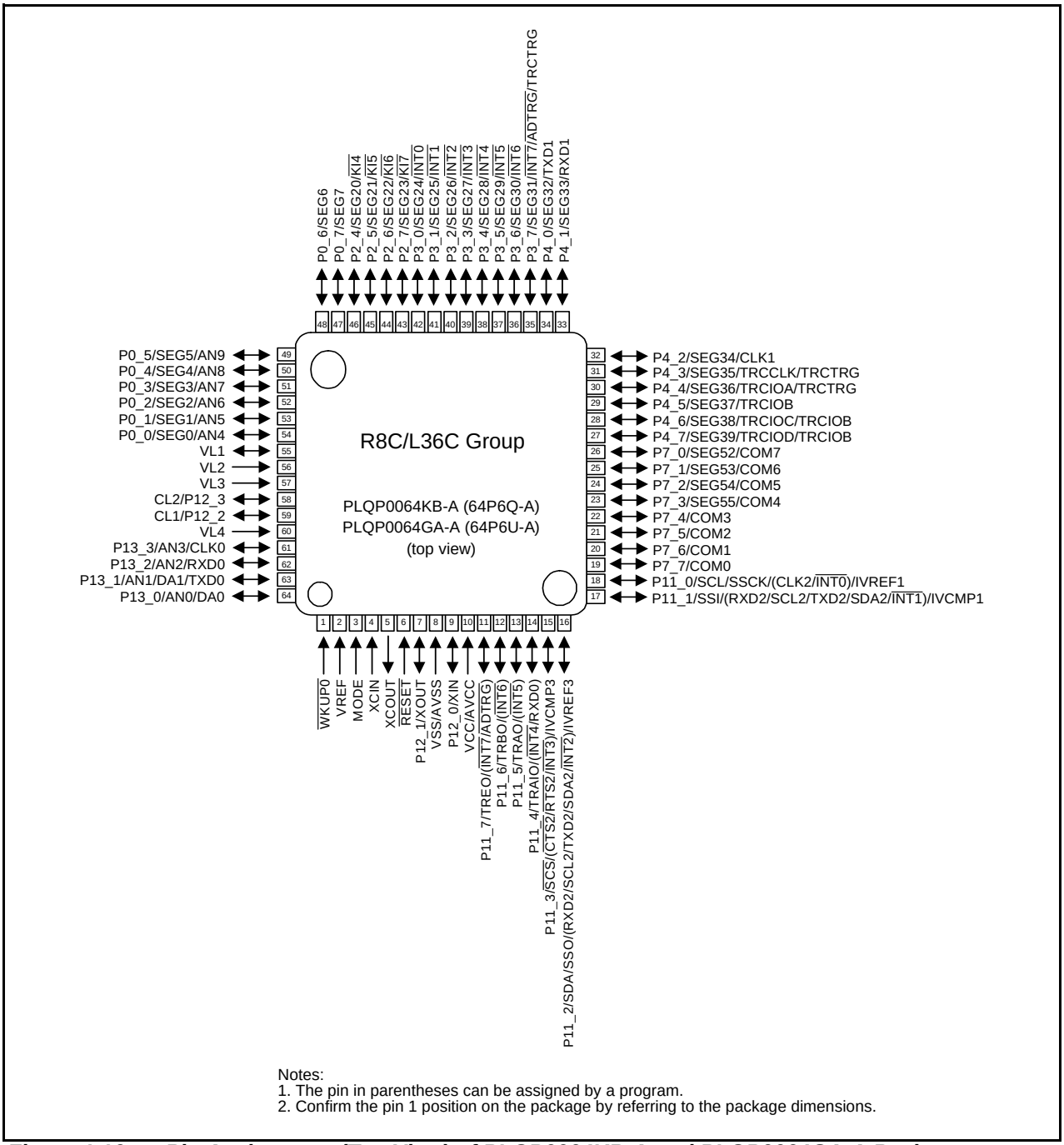
Table 1.4 Specifications (1)

Item	Function		Specification
CPU	Central processing unit		R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM/RAM Data flash		Refer to **Tables 1.7 to 1.10 Product Lists**.
Power Supply Voltage Detection	Voltage detection circuit		• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	R8C/L35C Group	• CMOS I/O ports: 41, selectable pull-up resistor • High current drive ports: 5
		R8C/L36C Group	• CMOS I/O ports: 52, selectable pull-up resistor • High current drive ports: 8
		R8C/L38C Group	• CMOS I/O ports: 68, selectable pull-up resistor • High current drive ports: 8
		R8C/L3AC Group	• CMOS I/O ports: 88, selectable pull-up resistor • High current drive ports: 16
Clock	Clock generation circuits		4 circuits: XIN clock oscillation circuit XCIN clock oscillation circuit (32 kHz) High-speed on-chip oscillator (with frequency adjustment function) Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Division ratio selectable from 1, 2, 4, 8, and 16 • Low-power-consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode
			Real-time clock (timer RE)
Interrupts		R8C/L35C Group	• Number of interrupt vectors: 69 • External Interrupt: 9 ($\overline{\text{INT}}$ × 5, key input × 4) • Priority levels: 7 levels
		R8C/L36C Group	• Number of interrupt vectors: 69 • External Interrupt: 12 ($\overline{\text{INT}}$ × 8, key input × 4) • Priority levels: 7 levels
		R8C/L38C Group	• Number of interrupt vectors: 69 • External Interrupt: 16 ($\overline{\text{INT}}$ × 8, key input × 8) • Priority levels: 7 levels
		R8C/L3AC Group	• Number of interrupt vectors: 69 • External Interrupt: 16 ($\overline{\text{INT}}$ × 8, key input × 8) • Priority levels: 7 levels
Watchdog Timer			• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for watchdog timer
DTC (Data Transfer Controller)			• 1 channel • Activation sources: 38 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.5 Specifications (2)

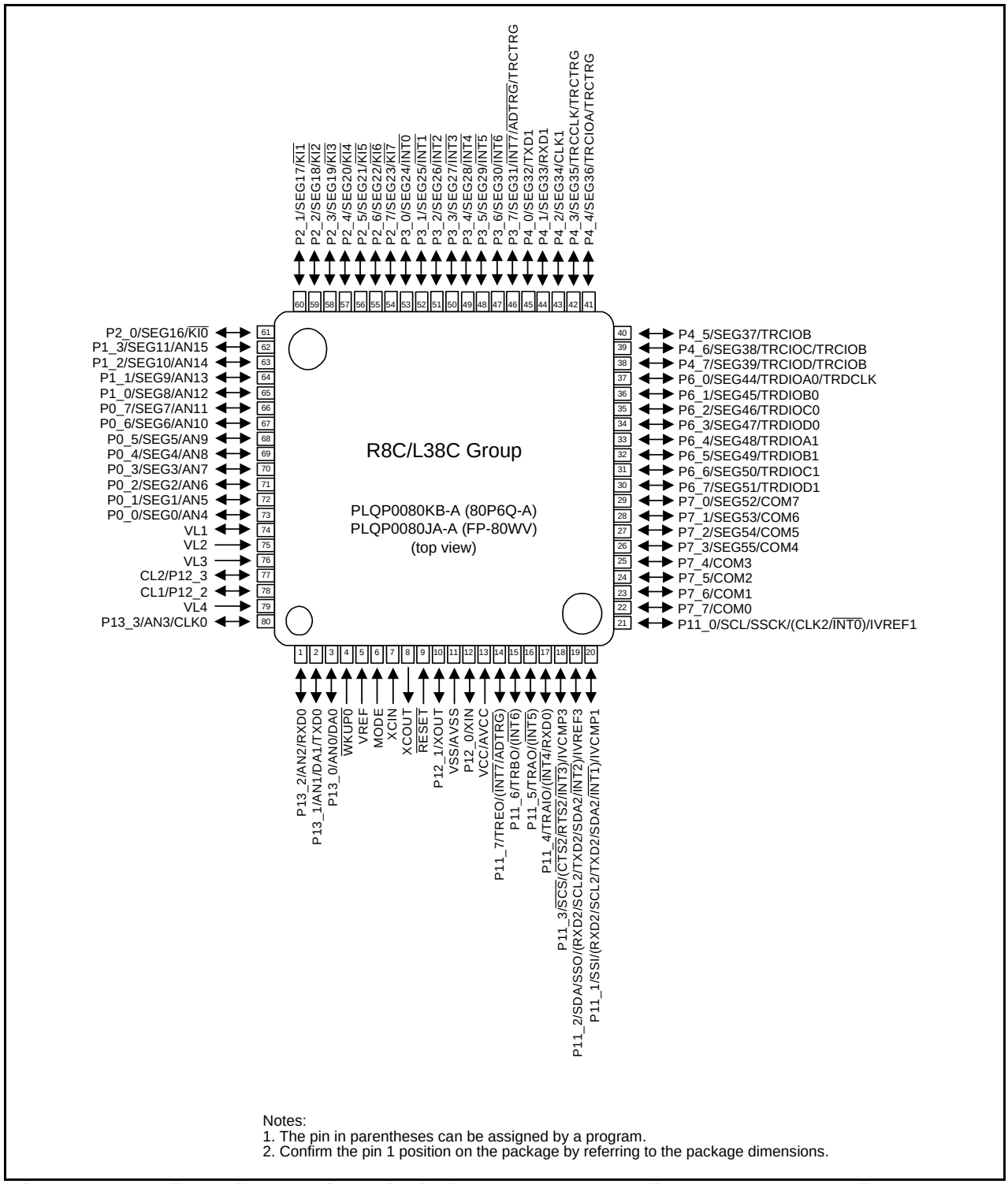
Item	Function	Specification	
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode	
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode	
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)	
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output: 6 pins, sawtooth wave modulation), complementary PWM mode (three-phase waveform output: 6 pins, triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)	
	Timer RE	8 bits × 1 Real-time clock mode (counting of seconds, minutes, hours, days of week), output compare mode	
	Timer RG	16 bits × 1 Phase-counting mode, timer mode (output compare function, input capture function), PWM mode (output: 1 pin)	
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART × 2 channels	
	UART2	Clock synchronous serial I/O/UART, I^2C mode (I^2C-bus), multiprocessor communication function	
Synchronous Serial Communication Unit (SSU)		1 (shared with I^2C-bus)	
I^2C bus		1 (shared with SSU)	
LIN Module		Hardware LIN: 1 channel (timer RA, UART0 used)	
A/D Converter	R8C/L35C Group	10-bit resolution × 10 channels, including sample and hold function, with sweep mode	
	R8C/L36C Group	10-bit resolution × 10 channels, including sample and hold function, with sweep mode	
	R8C/L38C Group	10-bit resolution × 16 channels, including sample and hold function, with sweep mode	
	R8C/L3AC Group	10-bit resolution × 20 channels, including sample and hold function, with sweep mode	
D/A Converter		8-bit resolution × 2 circuits	
Comparator B		2 circuits	
LCD Drive Control Circuit	R8C/L35C Group	Common output: Max. 4 pins Segment output: Max. 24 pins	Bias: 1/2, 1/3 Duty: static, 1/2, 1/3, 1/4
	R8C/L36C Group	Common output: Max. 8 pins Segment output: Max. 32 pins (1)	Bias: 1/2, 1/3, 1/4 Duty: static, 1/2, 1/3, 1/4, 1/8
	R8C/L38C Group	Common output: Max. 8 pins Segment output: Max. 48 pins (1)	
	R8C/L3AC Group	Common output: Max. 8 pins Segment output: Max. 56 pins (1)	
		Voltage multiplier and dedicated regulator integrated	

Note:
1. This applies when four pins are selected for common output.



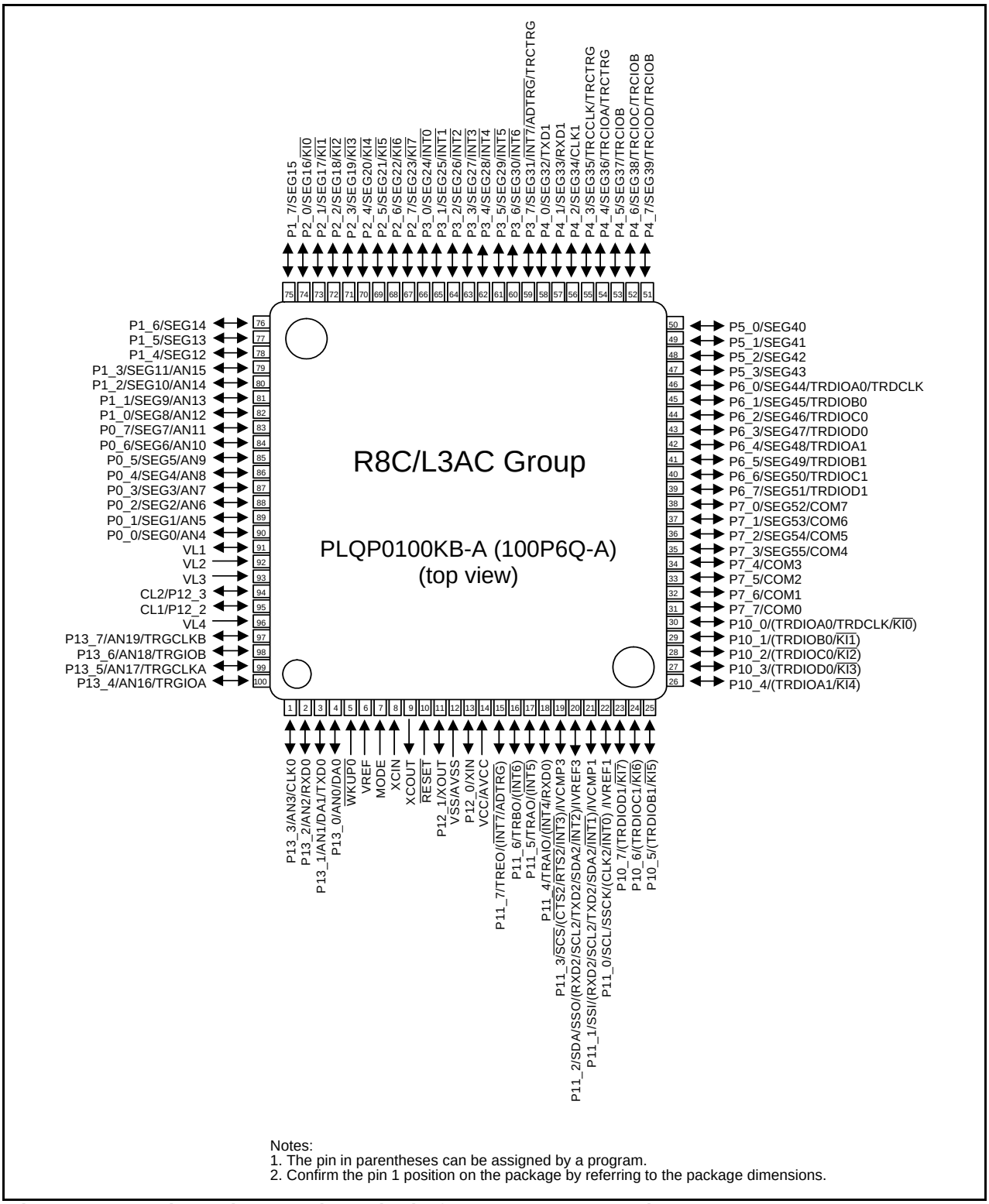
Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.10 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.11 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.12 Pin Assignment (Top View) of PLQP0100KB-A Package

Table 1.12 Pin Name Information by Pin Number (2)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
40 [42]	31				P6_6		TRDIOC1					SEG50
41 [43]	32				P6_5		TRDIOB1					SEG49
42 [44]	33				P6_4		TRDIOA1					SEG48
43 [45]	34				P6_3		TRDIOD0					SEG47
44 [46]	35				P6_2		TRDIOC0					SEG46
45 [47]	36				P6_1		TRDIOB0					SEG45
46 [48]	37				P6_0		TRDIOA0/ TRDCLK					SEG44
47 [49]					P5_3							SEG43
48 [50]					P5_2							SEG42
49 [51]					P5_1							SEG41
50 [52]					P5_0							SEG40
51 [53]	38	27	22		P4_7		TRCIOD/ TRCIOB					SEG39
52 [54]	39	28	23		P4_6		TRCIOC/ TRCIOB					SEG38
53 [55]	40	29	24		P4_5		TRCIOB					SEG37
54 [56]	41	30	25		P4_4		TRCIOA/ TRCTRG					SEG36
55 [57]	42	31	26		P4_3		TRCCLK/ TRCTRG					SEG35
56 [58]	43	32	27		P4_2			CLK1				SEG34
57 [59]	44	33	28		P4_1			RXD1				SEG33
58 [60]	45	34	29		P4_0			TXD1				SEG32
59 [61]	46	35			P3_7	$\overline{INT7}$	TRCTRG				$\overline{ADTRG}$	SEG31
60 [62]	47	36			P3_6	$\overline{INT6}$						SEG30
61 [63]	48	37			P3_5	$\overline{INT5}$						SEG29
62 [64]	49	38			P3_4	$\overline{INT4}$						SEG28
63 [65]	50	39	30		P3_3	$\overline{INT3}$						SEG27
64 [66]	51	40	31		P3_2	$\overline{INT2}$						SEG26
65 [67]	52	41	32		P3_1	$\overline{INT1}$						SEG25
66 [68]	53	42	33		P3_0	$\overline{INT0}$						SEG24
67 [69]	54	43	34		P2_7	$\overline{KI7}$						SEG23
68 [70]	55	44	35		P2_6	$\overline{KI6}$						SEG22
69 [71]	56	45	36		P2_5	$\overline{KI5}$						SEG21
70 [72]	57	46	37		P2_4	$\overline{KI4}$						SEG20
71 [73]	58				P2_3	$\overline{KI3}$						SEG19
72 [74]	59				P2_2	$\overline{KI2}$						SEG18
73 [75]	60				P2_1	$\overline{KI1}$						SEG17
74 [76]	61				P2_0	$\overline{KI0}$						SEG16
75 [77]					P1_7							SEG15
76 [78]					P1_6							SEG14
77 [79]					P1_5							SEG13
78 [80]					P1_4							SEG12
79 [81]	62				P1_3						AN15	SEG11
80 [82]	63				P1_2						AN14	SEG10
81 [83]	64				P1_1						AN13	SEG9
82 [84]	65				P1_0						AN12	SEG8
83 [85]	66	47	38		P0_7						AN11 (3)	SEG7
84 [86]	67	48	39		P0_6						AN10 (3)	SEG6

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.
3. Pins AN10 and AN11 are not available in the R8C/L35C, and R8C/L36C Groups.

1.5 Pin Functions

Tables 1.14 and 1.15 list Pin Functions for R8C/L3AC Group.

Table 1.14 Pin Functions for R8C/L3AC Group (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off mode exit input	$\overline{\text{WKUP0}}$	I	This pin is provided for input to exit the mode used in power-off mode. Connect to VSS when not using power-off mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Timer RG	TRGCLKA, TRGCLKB	I	Timer RG input pins
	TRGIOA, TRGIOB	I/O	Timer RG I/O pins
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin

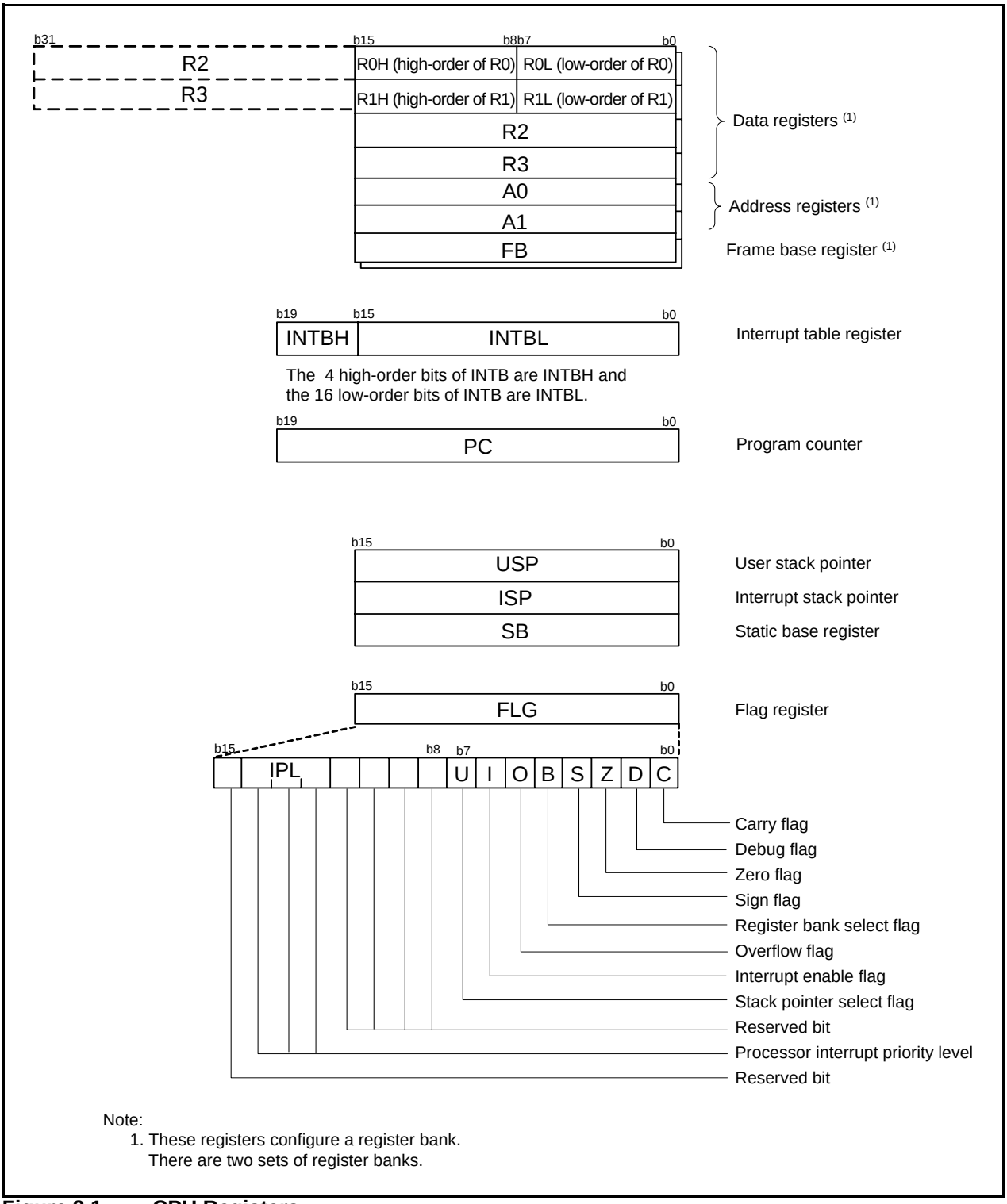
I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register banks.



Note:
1. These registers configure a register bank.
There are two sets of register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A 0 Register	DA0	00h
00D9h	D/A 1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P10 Register	P10	XXh
00F5h	Port P11 Register	P11	XXh
00F6h	Port P10 Direction Register	PD10	00h
00F7h	Port P11 Direction Register	PD11	00h
00F8h	Port P12 Register	P12	XXh
00F9h	Port P13 Register	P13	XXh
00FAh	Port P12 Direction Register	PD12	00h
00FBh	Port P13 Direction Register	PD13	00h
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Timer RE Counter Data Register	TRESEC	XXh
0119h	Timer RE Minute Data Register / Timer RE Compare Data Register	TREMIN	XXh
011Ah	Timer RE Hour Data Register	TREHR	XXh
011Bh	Timer RE Day of Week Data Register	TREWK	XXh
011Ch	Timer RE Control Register 1	TRECR1	XXXXX0XXb
011Dh	Timer RE Control Register 2	TRECR2	XXh
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h	Timer RD Control Expansion Register	TRDECR	00h
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h	LCD Bias Control Register	LCR1	00h
0202h	LCD Display Control Register	LCR2	X0000000b
0203h	LCD Clock Control Register	LCR3	00h
0204h			
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h	LCD Port Select Register 3	LSE3	00h
020Ah	LCD Port Select Register 4	LSE4	00h
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch	LCD Port Select Register 6	LSE6	00h
020Dh	LCD Port Select Register 7	LSE7	00h
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh		LRA27L	XXh
022Ch		LRA28L	XXh
022Dh		LRA29L	XXh
022Eh		LRA30L	XXh
022Fh		LRA31L	XXh
0230h		LRA32L	XXh
0231h		LRA33L	XXh
0232h		LRA34L	XXh
0233h		LRA35L	XXh
0234h		LRA36L	XXh
0235h		LRA37L	XXh
0236h		LRA38L	XXh
0237h		LRA39L	XXh
0238h		LRA40L	XXh
0239h		LRA41L	XXh
023Ah		LRA42L	XXh
023Bh		LRA43L	XXh
023Ch		LRA44L	XXh
023Dh		LRA45L	XXh
023Eh		LRA46L	XXh
023Fh		LRA47L	XXh

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.17 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

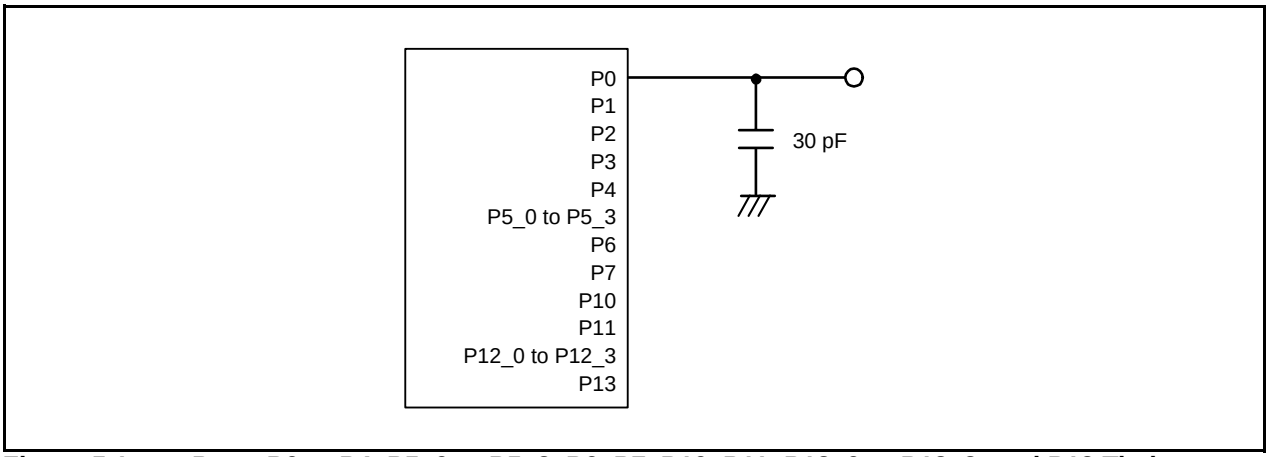


Figure 5.1 Ports P0 to P4, P5_0 to P5_3, P6, P7, P10, P11, P12_0 to P12_3, and P13 Timing Measurement Circuit

Table 5.22 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed								
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	Off	125 kHz	No division	—			—	2.2	—	mA
			5 MHz	Off	Off	125 kHz	Divide-by-8	—			—	0.8	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	—			—	2.5	10	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	—			—	1.7	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	90	300	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	90	400	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM		—	45	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	4	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	4	—	µA
										LCD drive control circuit (5) When the internal voltage multiplier is used	—	11	—	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2.0	5.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off		—	13	—	µA
		Power-off mode	Off	Off	Off	Off	—	—	Topr = 25°C		—	0.02	0.2	µA
			Off	Off	Off	Off	—	—	Topr = 85°C		—	0.3	—	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 2.2 V
4. VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.The standard value does not include the current that flows through external division resistors.
5. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

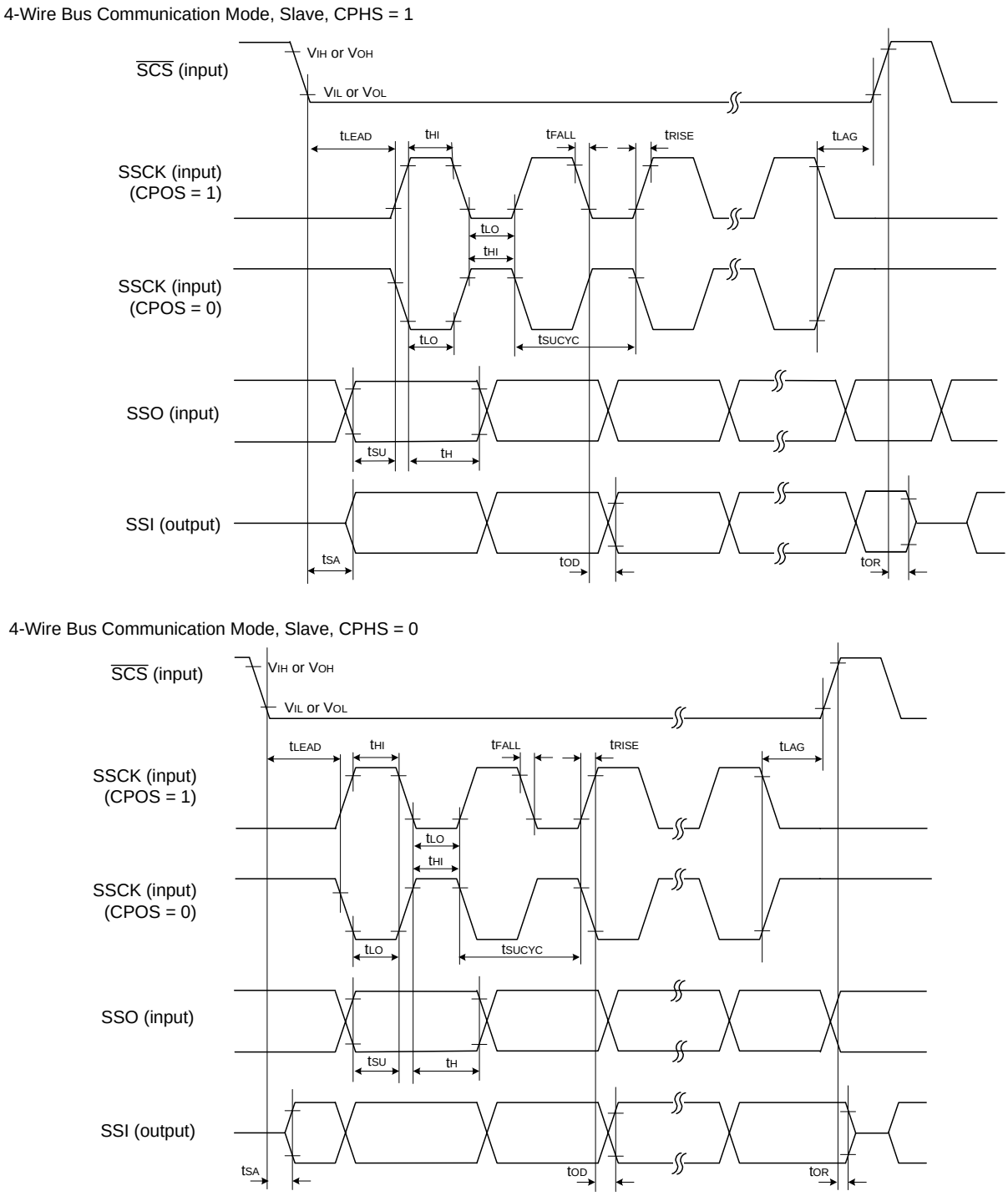
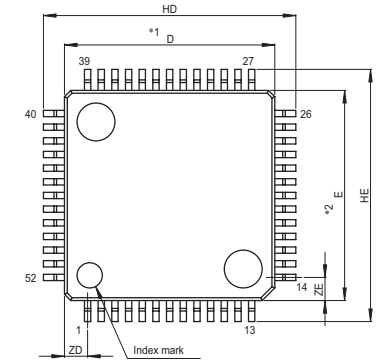


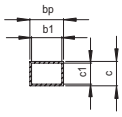
Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Package Dimensions

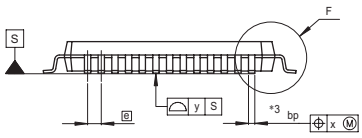
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

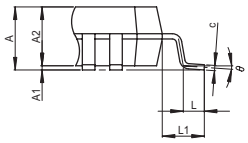
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g





Terminal cross section



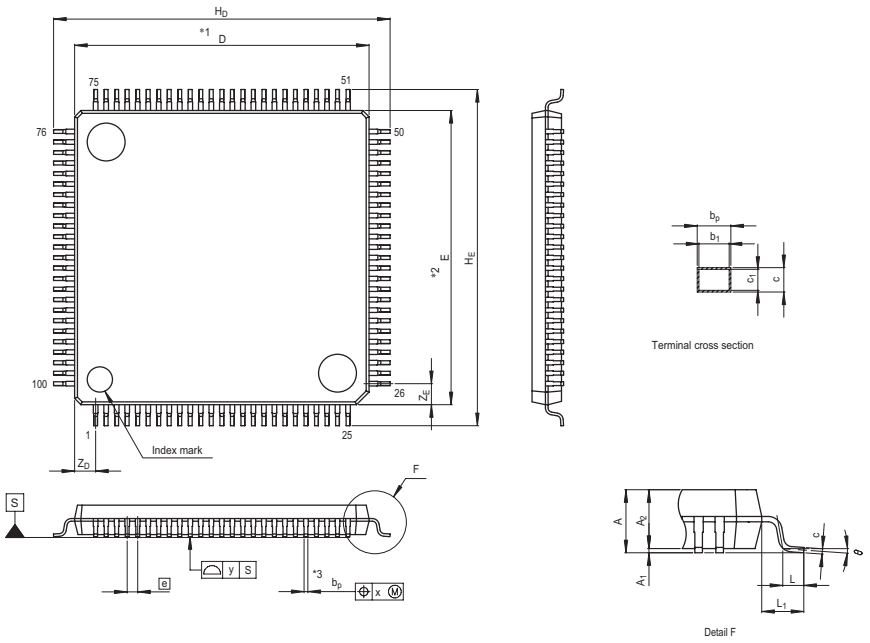


Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

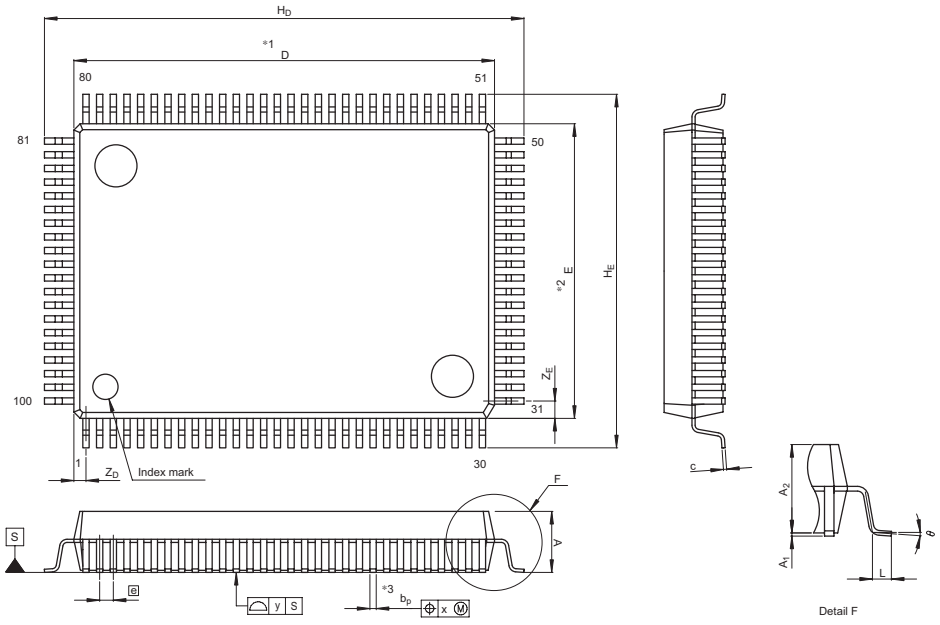
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8