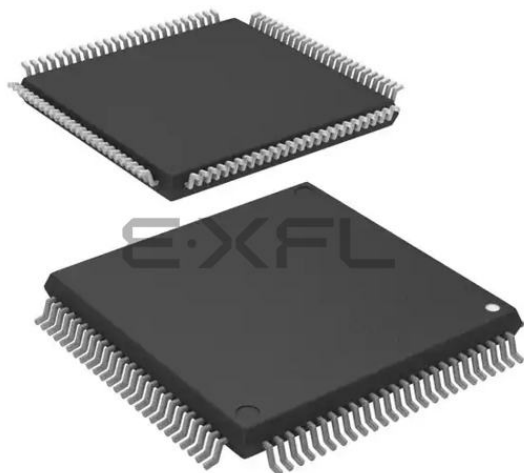




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Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	88
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l3accnfp-31

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Table 1.2 lists the Programmable I/O Ports Provided for Each Group, and Table 1.3 lists the LCD Display Function Pins Provided for Each Group. Figures 1.9 to 1.13 show the Pin Assignment for Each Group, and Tables 1.7 to 1.10 list Product Information.

The explanations in the chapters which follow apply to the R8C/L3AC Group only. Note the differences shown below.

Table 1.1 Differences between Groups

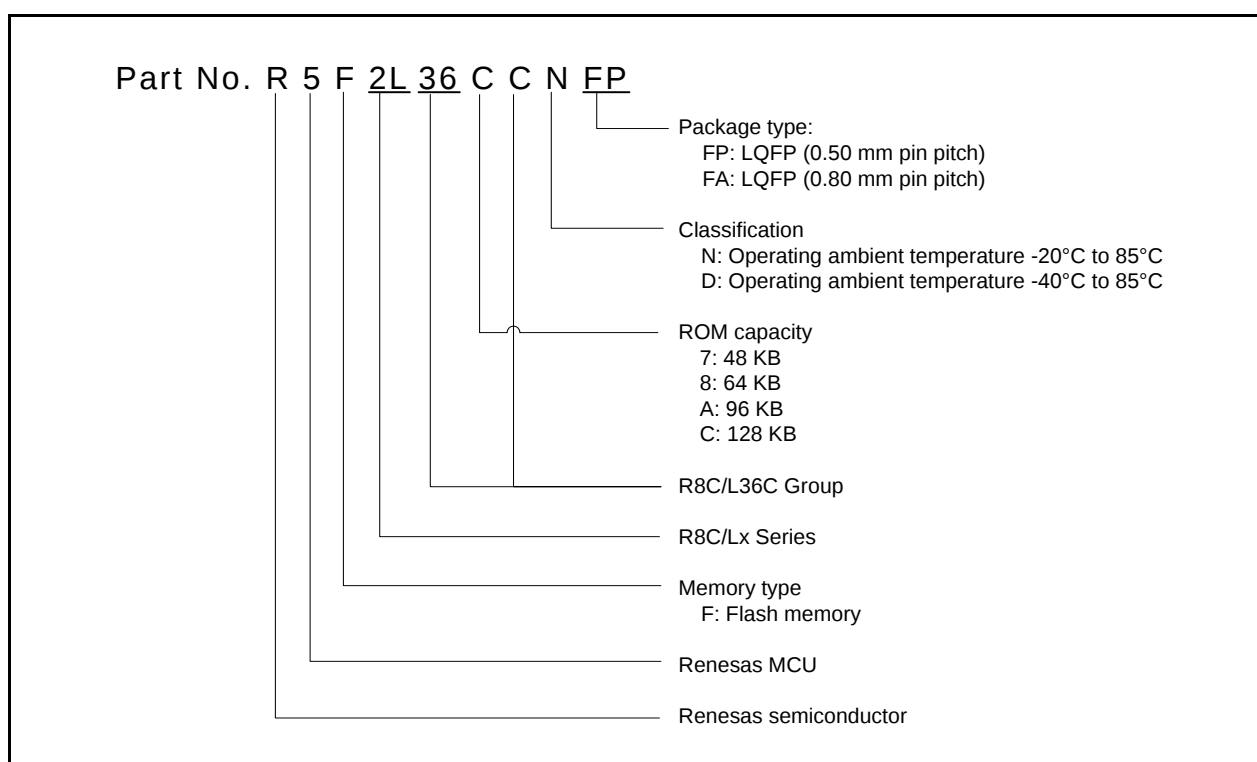
Item	Function	R8C/L35C Group	R8C/L36C Group	R8C/L38C Group	R8C/L3AC Group
I/O Ports	Programmable I/O ports	41 pins	52 pins	68 pins	88 pins
	High current drive ports	5 pins	8 pins	8 pins	16 pins
Interrupts	INT interrupt pins	5 pins	8 pins	8 pins	8 pins
	Key input interrupt pins	4 pins	4 pins	8 pins	8 pins
Timer RA	Timer RA output pin	None	1 pin	1 pin	1 pin
Timer RB	Timer RB output pin	None	1 pin	1 pin	1 pin
Timer RD	Timer RD I/O pin	None	None	8 pins	8 pins
Timer RE	Timer RE output pin	None	1 pin	1 pin	1 pin
Timer RG	Timer RG I/O pin	None	None	None	2 pins
	Timer RG output pin	None	None	None	2 pins
A/D Converter	Analog input pin	10 pins	10 pins	16 pins	20 pins
LCD Drive Control Circuit	LCD power supply	3 pins (VL1, VL2, VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)
	Common output pins	Max. 4 pins	Max. 8 pins	Max. 8 pins	Max. 8 pins
	Segment output pins	Max. 24 pins	Max. 32 pins	Max. 48 pins	Max. 56 pins
Packages		52-pin LQFP	64-pin LQFP	80-pin LQFP	100-pin LQFP/ 100-pin QFP

Note:

1. I/O ports are shared with I/O functions, such as interrupts or timers.
Refer to **Tables 1.11 to 1.13, Pin Name Information by Pin Number**, for details.

Table 1.8 Product List for R8C/L36C Group**Current of Apr 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L367CNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	N Version
R5F2L367CNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368CNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368CNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36ACNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36ACNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L367CDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	D Version
R5F2L367CDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368CDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368CDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36ACDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36ACDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	

**Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/L36C Group**

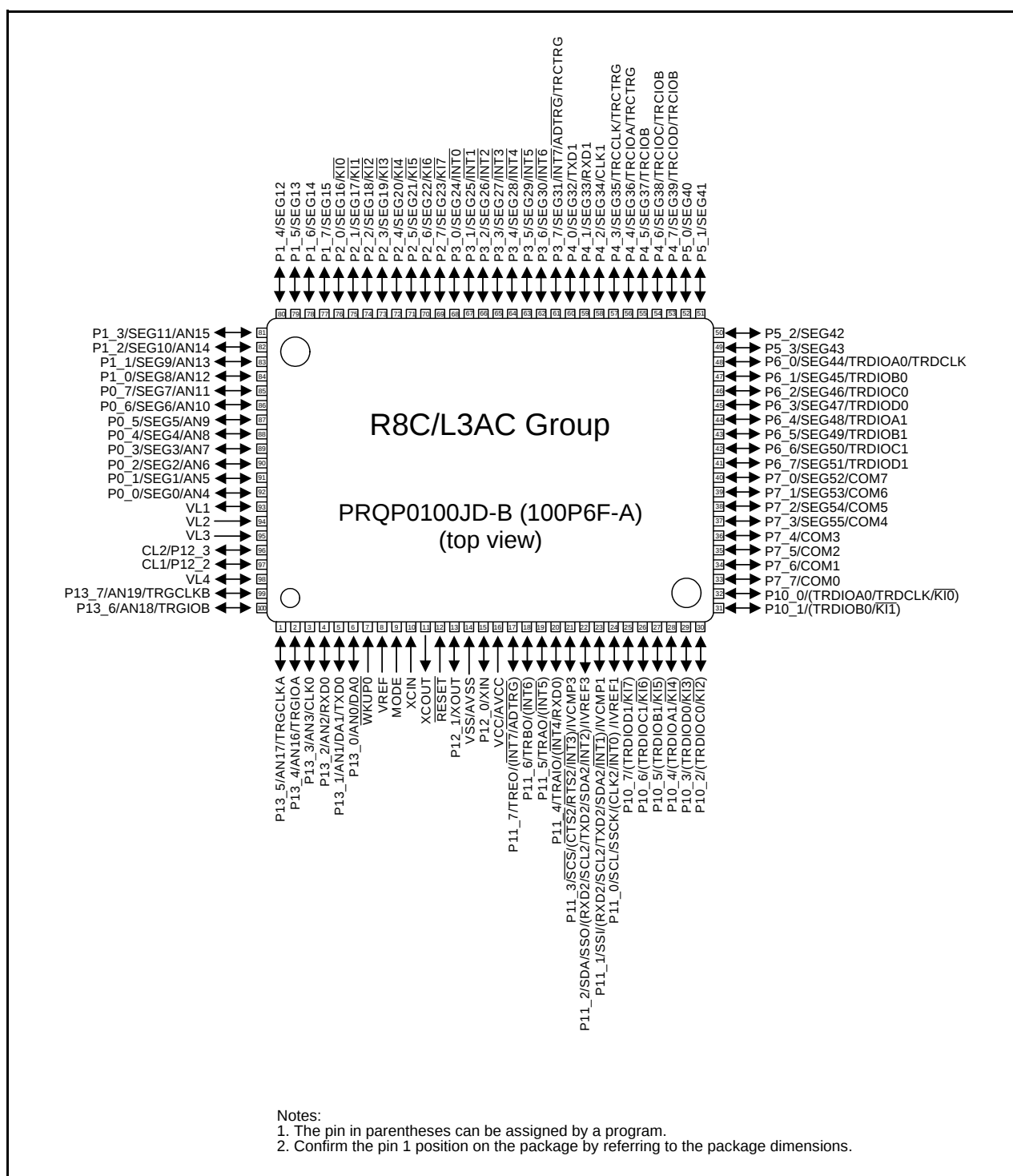


Figure 1.13 Pin Assignment (Top View) of PRQP0100JD-B Package

Table 1.11 Pin Name Information by Pin Number (1)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AC (Note 2)	L38C	L36C	L35C			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B	LCD drive control circuit
1 [3]	80	61	51		P13_3			CLK0			AN3	
2 [4]	1	62	52		P13_2			RXD0			AN2	
3 [5]	2	63	1		P13_1			TXD0			AN1/DA1	
4 [6]	3	64	2		P13_0						AN0/DA0	
5 [7]	4	1	3	WKUP0								
6 [8]	5	2	4	VREF								
7 [9]	6	3	5	MODE								
8 [10]	7	4	6	XCIN								
9 [11]	8	5	7	XCOUT								
10 [12]	9	6	8	RESET								
11 [13]	10	7	9	XOUT	P12_1							
12 [14]	11	8	10	VSS/AVSS								
13 [15]	12	9	11	XIN	P12_0							
14 [16]	13	10	12	VCC/AVCC								
15 [17]	14	11			P11_7	(INT7)	TREO				(ADTRG)	
16 [18]	15	12			P11_6	(INT6)	TRBO					
17 [19]	16	13			P11_5	(INT5)	TRA0					
18 [20]	17	14	13		P11_4	(INT4)	TRAIO	(RXD0)				
19 [21]	18	15	14		P11_3	(INT3)		(CTS2/RTS2)	SCS		IVCMP3	
20 [22]	19	16	15		P11_2	(INT2)		(RXD2/SCL2/TXD2/SDA2)	SSO	SDA	IVREF3	
21 [23]	20	17	16		P11_1	(INT1)		(RXD2/SCL2/TXD2/SDA2)	SSI		IVCMP1	
22 [24]	21	18	17		P11_0	(INT0)		(CLK2)	SSCK	SCL	IVREF1	
23 [25]					P10_7	(KI7)	(TRDIOD1)					
24 [26]					P10_6	(KI6)	(TRDIOD1)					
25 [27]					P10_5	(KI5)	(TRDIOD1)					
26 [28]					P10_4	(KI4)	(TRDIOA1)					
27 [29]					P10_3	(KI3)	(TRDIOD0)					
28 [30]					P10_2	(KI2)	(TRDIOD0)					
29 [31]					P10_1	(KI1)	(TRDIOD0)					
30 [32]					P10_0	(KI0)	(TRDIOA0/TRDCLK)					
31 [33]	22	19	18		P7_7							COM0
32 [34]	23	20	19		P7_6							COM1
33 [35]	24	21	20		P7_5							COM2
34 [36]	25	22	21		P7_4							COM3
35 [37]	26	23			P7_3							SEG55/COM4
36 [38]	27	24			P7_2							SEG54/COM5
37 [39]	28	25			P7_1							SEG53/COM6
38 [40]	29	26			P7_0							SEG52/COM7
39 [41]	30				P6_7		TRDIOD1					SEG51

Notes:

1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register banks.

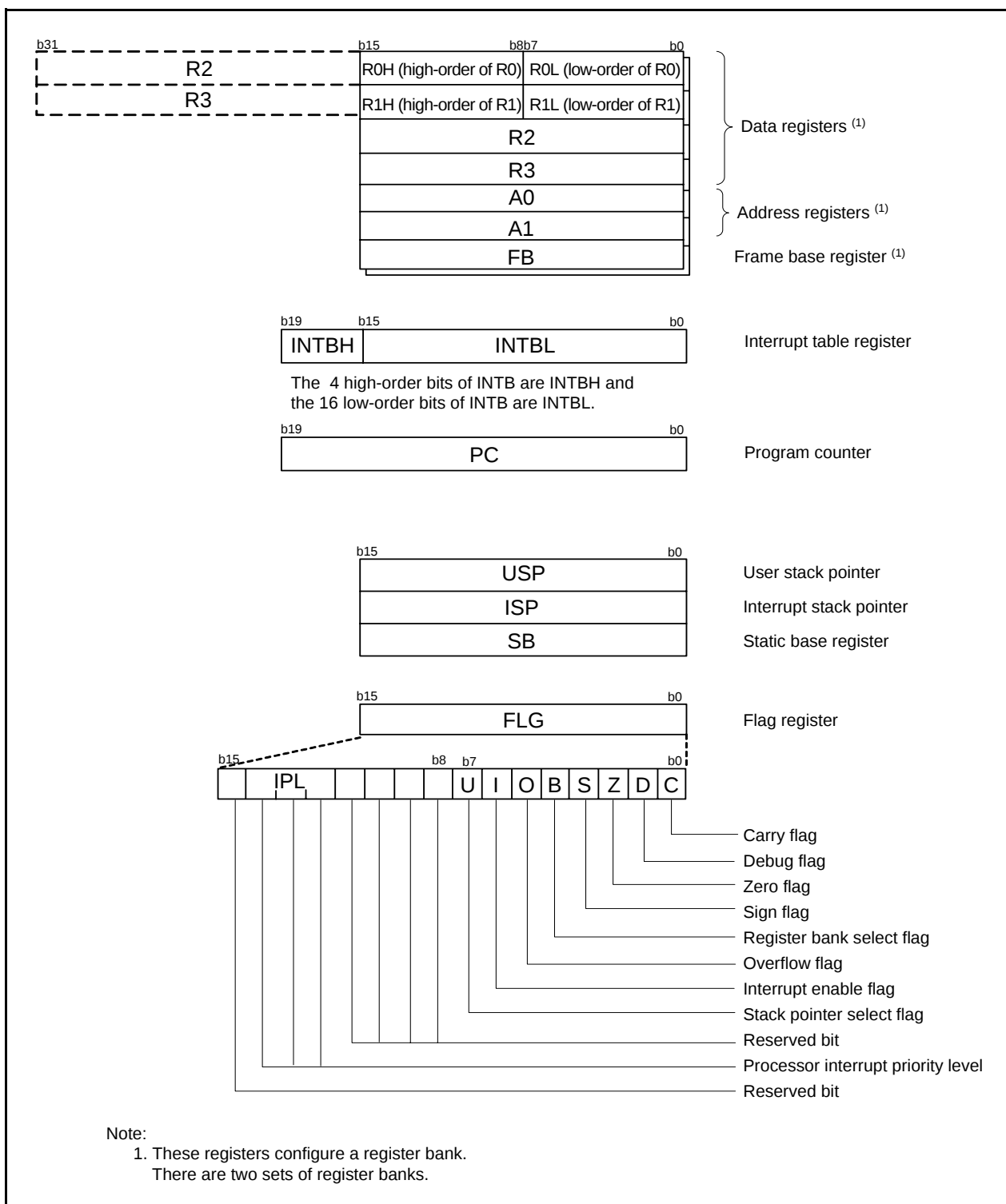


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.10 SFR Information (10) ⁽¹⁾

Address	Register	Symbol	After Reset
0240h	LCD Display Data Register	LRA48L	XXh
0241h		LRA49L	XXh
0242h		LRA50L	XXh
0243h		LRA51L	XXh
0244h		LRA52L	XXh
0245h		LRA53L	XXh
0246h		LRA54L	XXh
0247h		LRA55L	XXh
0248h			
0249h			
024Ah			
024Bh			
024Ch			
024Dh			
024Eh			
024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h			
0261h			
0262h			
0263h			
0264h			
0265h			
0266h			
0267h			
0268h			
0269h			
026Ah			
026Bh			
026Ch			
026Dh			
026Eh			
026Fh			
0270h	LCD Display Control Data Register	LRA0H	XXh
0271h		LRA1H	XXh
0272h		LRA2H	XXh
0273h		LRA3H	XXh
0274h		LRA4H	XXh
0275h		LRA5H	XXh
0276h		LRA6H	XXh
0277h		LRA7H	XXh
0278h		LRA8H	XXh
0279h		LRA9H	XXh
027Ah		LRA10H	XXh
027Bh		LRA11H	XXh
027Ch		LRA12H	XXh
027Dh		LRA13H	XXh
027Eh		LRA14H	XXh
027Fh		LRA15H	XXh

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.11 SFR Information (11) ⁽¹⁾

Address	Register	Symbol	After Reset
0280h	LCD Display Control Data Register	LRA16H	XXh
0281h		LRA17H	XXh
0282h		LRA18H	XXh
0283h		LRA19H	XXh
0284h		LRA20H	XXh
0285h		LRA21H	XXh
0286h		LRA22H	XXh
0287h		LRA23H	XXh
0288h		LRA24H	XXh
0289h		LRA25H	XXh
028Ah		LRA26H	XXh
028Bh		LRA27H	XXh
028Ch		LRA28H	XXh
028Dh		LRA29H	XXh
028Eh		LRA30H	XXh
028Fh		LRA31H	XXh
0290h		LRA32H	XXh
0291h		LRA33H	XXh
0292h		LRA34H	XXh
0293h		LRA35H	XXh
0294h		LRA36H	XXh
0295h		LRA37H	XXh
0296h		LRA38H	XXh
0297h		LRA39H	XXh
0298h		LRA40H	XXh
0299h		LRA41H	XXh
029Ah		LRA42H	XXh
029Bh		LRA43H	XXh
029Ch		LRA44H	XXh
029Dh		LRA45H	XXh
029Eh		LRA46H	XXh
029Fh		LRA47H	XXh
02A0h		LRA48H	XXh
02A1h		LRA49H	XXh
02A2h		LRA50H	XXh
02A3h		LRA51H	XXh
02A4h		LRA52H	XXh
02A5h		LRA53H	XXh
02A6h		LRA54H	XXh
02A7h		LRA55H	XXh
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.12 SFR Information (12) ⁽¹⁾

Address	Register	Symbol	After Reset
02C0h			
02C1h			
02C2h			
02C3h			
02C4h			
02C5h			
02C6h			
02C7h			
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h			
02E1h			
02E2h			
02E3h			
02E4h			
02E5h			
02E6h			
02E7h			
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh			
02FFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.13 SFR Information (13) ⁽¹⁾

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.15 SFR Information (15) ⁽¹⁾

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions
(VCC = 1.8 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter			Conditions	Standard			Unit	
					Min.	Typ.	Max.		
Vcc/AVcc	Supply voltage				1.8	—	5.5	V	
Vss/AVss	Supply voltage				—	0	—	V	
VIH	Input “H” voltage	Other than CMOS input		4.0 V ≤ Vcc ≤ 5.5 V	0.8 Vcc	—	Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0.8 Vcc	—	Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0.9 Vcc	—	Vcc	V	
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
VIL	Input “L” voltage	Other than CMOS input		4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0	—	0.05 Vcc	V	
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)			—	—	–160	mA	
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(aveg)			—	—	–80	mA	
IOH(peak)	Peak output “H” current	Port P10, P11 (2)			—	—	–40	mA	
		Other pins			—	—	–10	mA	
IOH(aveg)	Average output “H” current (1)	Port P10, P11 (2)			—	—	–20	mA	
		Other pins			—	—	–5	mA	
IoL(sum)	Peak sum output “L” current	Sum of all pins IoL(peak)			—	—	160	mA	
IoL(sum)	Average sum output “L” current	Sum of all pins IoL(aveg)			—	—	80	mA	
IoL(peak)	Peak output “L” current	Port P10, P11 (2)			—	—	40	mA	
		Other pins			—	—	10	mA	
IoL(aveg)	Average output “L” current (1)	Port P10, P11 (2)			—	—	20	mA	
		Other pins			—	—	5	mA	
f(XIN)	XIN clock input ossillation frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
f(XCIN)	XCIN clock input ossillation frequency			1.8 V ≤ Vcc ≤ 5.5 V	—	32.768	50	kHz	
fOCO40M	When used as the count source for timer RC, timer RD, or timer RG (3)			2.7 V ≤ Vcc ≤ 5.5 V	32	—	40	MHz	
fOCO-F	fOCO-F frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
—	System clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
f(BCLK)	CPU clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	

Notes:

1. The average output current indicates the average value of current measured during 100 ms.
2. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.
3. fOCO40M can be used as the count source for timer RC, timer RD, or timer RG in the range of VCC = 2.7 V to 5.5V.

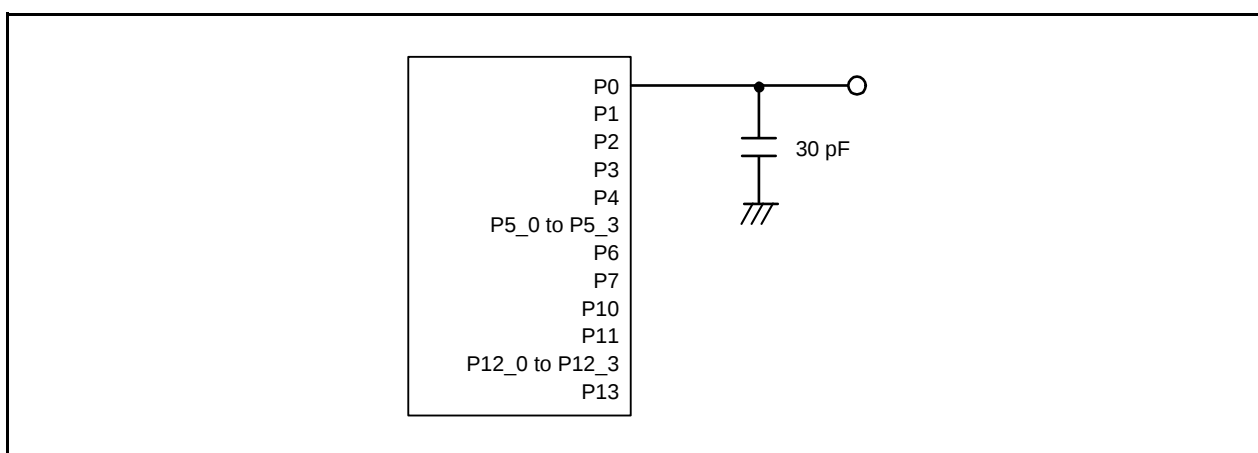


Figure 5.1 Ports P0 to P4, P5_0 to P5_3, P6, P7, P10, P11, P12_0 to P12_3, and P13 Timing Measurement Circuit

5.3 Peripheral Function Characteristics

Table 5.3 A/D Converter Characteristics
($V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version) /
 -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVCC		—	—	10	Bit
—	Absolute accuracy ⁽²⁾	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN19 input	—	—	±3	LSB
			Vref = AVCC = 3.3 V	AN0 to AN19 input	—	—	±5	LSB
			Vref = AVCC = 3.0 V	AN0 to AN19 input	—	—	±5	LSB
			Vref = AVCC = 2.2 V	AN0 to AN19 input	—	—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN19 input	—	—	±2	LSB
			Vref = AVCC = 3.3 V	AN0 to AN19 input	—	—	±2	LSB
			Vref = AVCC = 3.0 V	AN0 to AN19 input	—	—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN19 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		2	—	20	MHz
			3.2 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		2	—	16	MHz
			2.7 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		2	—	10	MHz
			2.2 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				2.2	—	AVCC	V
VIa	Analog input voltage ⁽³⁾				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.20 DC Characteristics (4) [2.7 V ≤ V_{CC} < 4.0 V]
(T_{OP} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition								Standard			Unit	
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)	Max.		
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed									
I _{CC}	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—			—	7.0	14.5	mA	
			10 MHz	Off	Off	125 kHz	No division	—			—	3.6	10	mA	
			20 MHz	Off	Off	125 kHz	Divide-by-8	—			—	3.0	—	mA	
			10 MHz	Off	Off	125 kHz	Divide-by-8	—			—	1.5	—	mA	
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—			—	7.0	14.5	mA	
			Off	Off	20 MHz	125 kHz	Divide-by-8	—			—	3.0	—	mA	
			Off	Off	10 MHz	125 kHz	No division	—			—	4.0	—	mA	
			Off	Off	10 MHz	125 kHz	Divide-by-8	—			—	1.7	—	mA	
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			—	1	—	mA	
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	85	390	μA	
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	90	400	μA	
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM			—	50	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	15	90	μA	
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	5	80	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	5	—	μA	
									LCD drive control circuit (5) When the internal voltage multiplier is used			—	11	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	μA	
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	T _{OP} = 25°C Peripheral clock off		—	2	5.0	μA	
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	T _{OP} = 85°C Peripheral clock off		—	13.0	—	μA	
		Power-off mode	Off	Off	Off	Off	—	—		T _{OP} = 25°C		—	0.02	0.2	μA
			Off	Off	Off	Off	—	—		T _{OP} = 85°C		—	0.3	—	μA

Notes:

- V_{CC} = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are V_{SS}.
- XIN is set to square wave input.
- V_{CC} = 3.0 V
- V_{LCD} = V_{CC}, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
- The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

Table 5.21 DC Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output "H" voltage	Port P10, P11 (1)	$I_{OH} = -2\text{ mA}$	$V_{CC} - 0.5$	—	V_{CC}	V
		Other pins	$I_{OH} = -1\text{ mA}$	$V_{CC} - 0.5$	—	V_{CC}	V
		XOUT	$I_{OH} = -200\text{ }\mu\text{A}$	1.0	—	—	V
VOL	Output "L" voltage	Port P10, P11 (1)	$I_{OL} = 2\text{ mA}$	—	—	0.5	V
		Other pins	$I_{OL} = 1\text{ mA}$	—	—	0.5	V
		XOUT	$I_{OL} = 200\text{ }\mu\text{A}$	—	—	0.5	V
VT+-VT-	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}},$ $\overline{\text{INT3}}, \overline{\text{INT4}}, \overline{\text{INT5}},$ $\overline{\text{INT6}}, \overline{\text{INT7}},$ $\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}}, \overline{\text{KI4}},$ $\overline{\text{KI5}}, \overline{\text{KI6}}, \overline{\text{KI7}},$ $\overline{\text{TRAI0}},$ $\overline{\text{TRCIOA}}, \overline{\text{TRCIOB}},$ $\overline{\text{TRCIOC}}, \overline{\text{TRCIOD}},$ $\overline{\text{TRDIOA0}}, \overline{\text{TRDIOB0}},$ $\overline{\text{TRDIOC0}}, \overline{\text{TRDIOD0}},$ $\overline{\text{TRDIOA1}}, \overline{\text{TRDIOB1}},$ $\overline{\text{TRDIOC1}}, \overline{\text{TRDIOD1}},$ $\overline{\text{TRCTRG}}, \overline{\text{TRCCLK}},$ $\overline{\text{TRGCLKA}}, \overline{\text{TRGCLKB}},$ $\overline{\text{TRGIOA}}, \overline{\text{TRGIOB}},$ $\overline{\text{ADTRG}},$ $\overline{\text{RXD0}}, \overline{\text{RXD1}}, \overline{\text{RXD2}},$ $\overline{\text{CLK0}}, \overline{\text{CLK1}}, \overline{\text{CLK2}},$ $\overline{\text{SSI}}, \overline{\text{SCL}}, \overline{\text{SDA}}, \overline{\text{SSO}}$		0.05	0.4	—	V
		RESET, WKUP0		0.1	0.8	—	V
I _{IH}	Input "H" current		$V_I = 1.8\text{ V}, V_{CC} = 1.8\text{ V}$	—	—	4.0	μA
I _{IL}	Input "L" current		$V_I = 0\text{ V}, V_{CC} = 1.8\text{ V}$	—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		$V_I = 0\text{ V}, V_{CC} = 1.8\text{ V}$	60	160	420	k Ω
R _{IXIN}	Feedback resistance	XIN		—	0.3	—	M Ω
R _{IXCIN}	Feedback resistance	XCIN		—	14	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.22 DC Characteristics (6) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed								
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	Off	125 kHz	No division	—			—	2.2	—	mA
			5 MHz	Off	Off	125 kHz	Divide-by-8	—			—	0.8	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	—			—	2.5	10	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	—			—	1.7	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	90	300	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	90	400	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	—	45	—	μA	
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	15	90	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	4	80	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	4	—	μA
									LCD drive control circuit (5) When the internal voltage multiplier is used	—	11	—	μA	
		Stop mode	Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	μA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2.0	5.0	μA
									Topr = 85°C Peripheral clock off		—	13	—	μA
			Power-off mode	Off	Off	Off	Off	—	—	Topr = 25°C		—	0.02	0.2
		Off		Off	Off	Off	—	—	Topr = 85°C		—	0.3	—	μA

Notes:

1. $V_{CC} = 1.8\text{ V}$ to 2.7 V , single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. $V_{CC} = 2.2\text{ V}$
4. VLCD = V_{CC}, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
5. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

