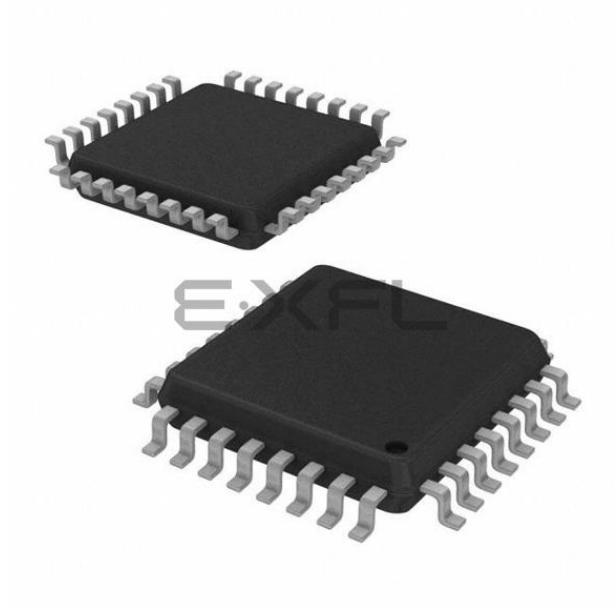

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	75MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv10z16vlc7

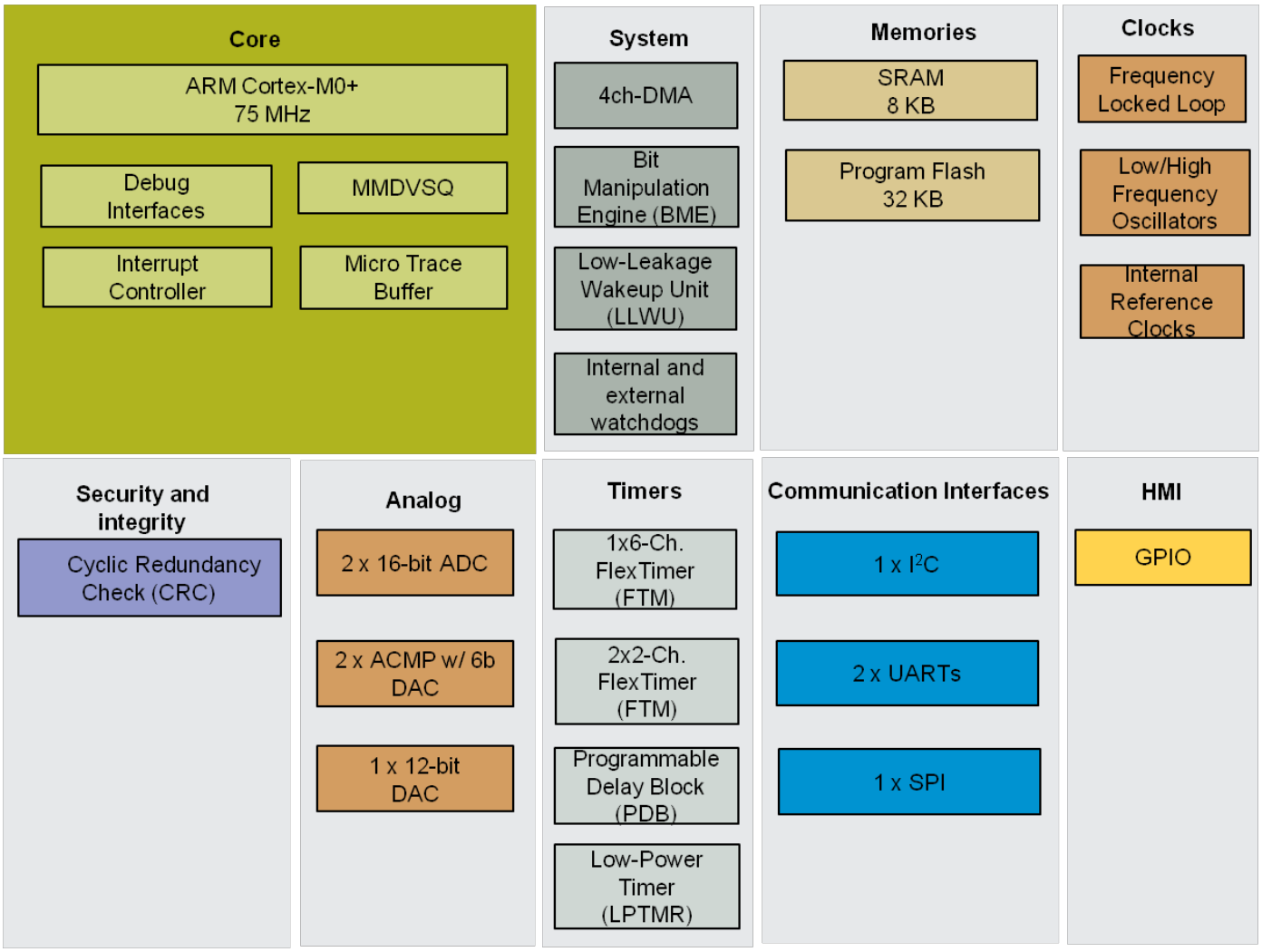

Figure 1. KV10 block diagram

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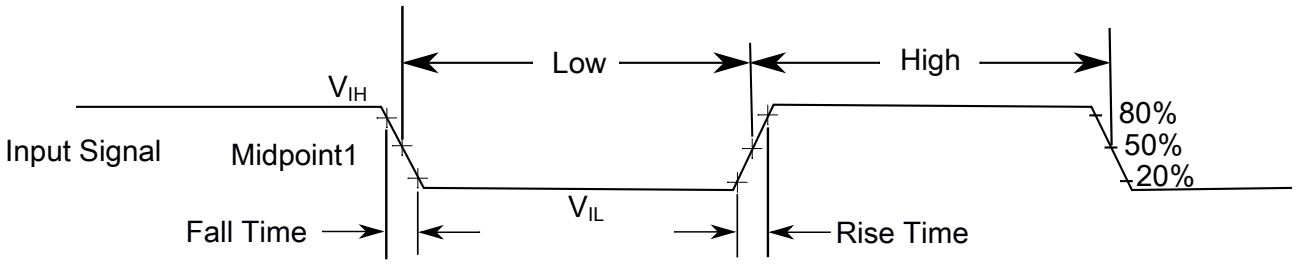


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume:

1. output pins
   - have C_L=30pF loads,
   - are slew rate disabled, and
   - are normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	Pin negative DC injection current—single pin • V_{IN} < V_{SS}–0.3V	-5	—	mA	1

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 3.0 V 50 MHz (25 MHz Bus)	—	5	6.3	mA	
	• at 1.8 V 75 MHz (25 MHz Bus)	—	6.5	7.8	mA	
	• at 3.0 V 75 MHz (25 MHz Bus)	—	6.5	7.5	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					Target IDD
	• at 1.8 V 50 MHz	—	7.1	8.2	mA	
	• at 3.0 V 50 MHz	—	7.1	8	mA	
	• at 1.8 V 75 MHz	—	9.4	10.9	mA	
	• at 3.0 V 75 MHz	—	9.4	10.6	mA	
I_{DD_WAIT}	Wait mode high frequency 75 MHz current at 3.0 V — all peripheral clocks disabled	—	4	5.2	mA	—
I_{DD_WAIT}	Wait mode reduced frequency 50 MHz current at 3.0 V — all peripheral clocks disabled	—	3.4	4.7	mA	—
I_{DD_VLPR}	Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks disabled	—	215	437	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPR}	Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks enabled	—	313	570	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPW}	Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks disabled	—	149	303	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPW}	Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks enabled	—	244	347	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_STOP}	Stop mode current at 3.0 V					—
	• -40 °C to 25 °C	—	248	280	µA	
	• at 50 °C	—	261	315		
	• at 70 °C	—	278	333		
	• at 85 °C	—	307	435		
	• at 105 °C	—	381	510		
I_{DD_VLPS}	Very-Low-Power Stop mode current at 3.0 V					—
	• -40 °C to 25 °C	—	2.2	4.3		
	• at 50 °C	—	4.2	9.9		

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 70 °C	—	8.8	24	µA	
	• at 85 °C	—	16.2	59		
	• at 105 °C	—	36.7	82		
I_{DD_VLLS3}	Very-Low-Leakage Stop mode 3 current at 3.0 V • -40 °C to 25 °C				µA	—
	• at 50 °C	—	1.3	5.7		
	• at 70 °C	—	1.9	6.1		
	• at 85 °C	—	3.3	7.4		
	• at 105 °C	—	5.8	11.2		
		—	13	18		
I_{DD_VLLS1}	Very-Low-Leakage Stop mode 1 current at 3.0 V • -40°C to 25°C				µA	—
	• at 50°C	—	0.8	3.0		
	• at 70°C	—	1.2	4.9		
	• at 85°C	—	2.2	7.0		
	• at 105°C	—	4	12.5		
		—	9.4	29.0		
I_{DD_VLLS0}	Very-Low-Leakage Stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V • -40 °C to 25 °C				µA	—
	• at 50 °C	—	0.279	0.7		
	• at 70 °C	—	0.638	1.2		
	• at 85 °C	—	1.63	2.5		
	• at 105 °C	—	3.4	4.5		
		—	8.9	12.0		
I_{DD_VLLS0}	Very-Low-Leakage Stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V • -40 °C to 25 °C				µA	2
	• at 50 °C	—	0.098	0.485		
	• at 70 °C	—	0.448	0.788		
	• at 85 °C	—	1.4	2.29		
	• at 105 °C	—	3.19	4.14		
		—	8.47	11.8		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. No brownout

The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 75 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	48	MHz	
f_{BUS}	Bus clock	—	24	MHz	
f_{FLASH}	Flash clock	—	24	MHz	
f_{LPTMR}	LPTMR clock	—	24	MHz	
High Speed run mode					
f_{SYS}	System and core clock	—	75	MHz	
f_{BUS}	Bus clock	—	25	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	

Table continues on the next page...

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{FTM}	FTM clock	—	75	MHz	
VLPR mode					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz	

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time Fast slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 8 7	 ns ns	3
	Port rise and fall time Slow slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 15 25	 ns ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (low drive) is 25pF.

Table 16. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 17. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

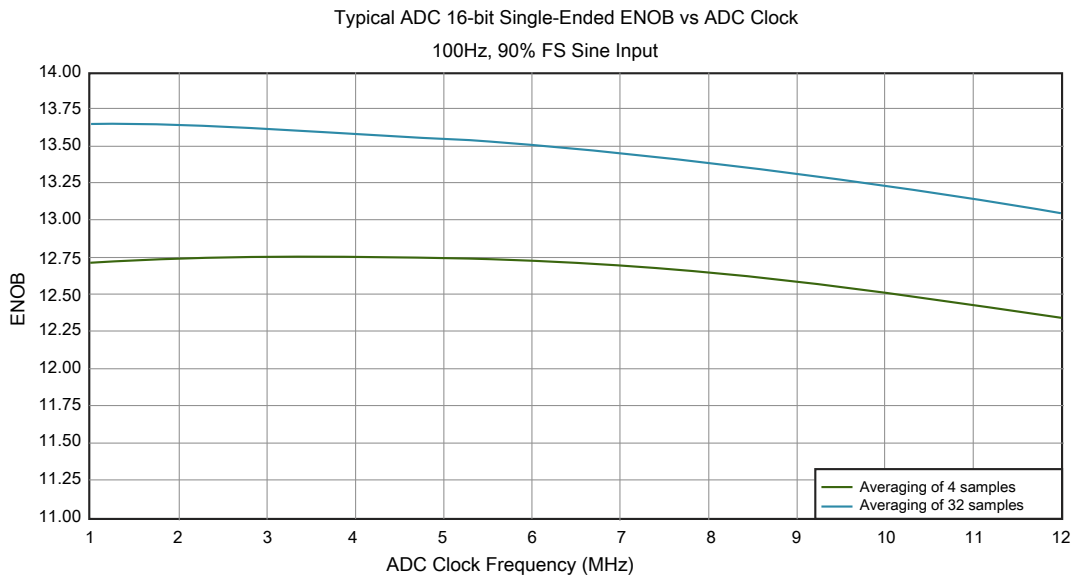


Figure 9. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 23. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	35	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	100	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs

Table continues on the next page...

Table 23. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to V_{DD} – 0.7 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

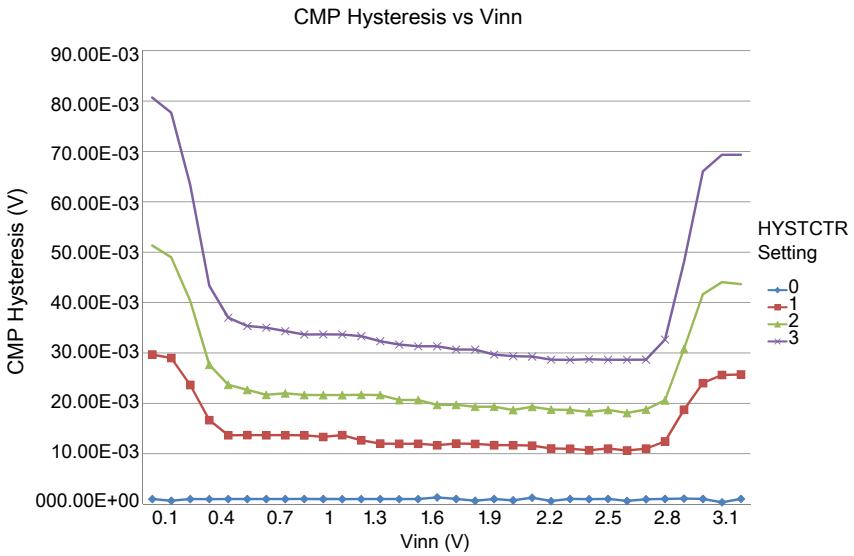


Figure 10. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

Table 25. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08)—high-speed mode	—	1	—	µs	1
	—low-power mode	—	—	5	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

3.8.1 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 26. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

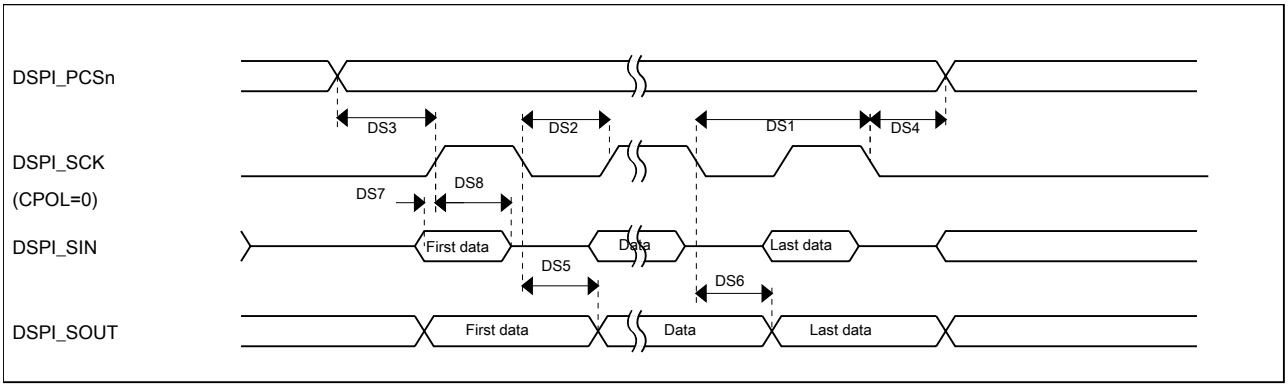


Figure 14. DSPI classic SPI timing — master mode

Table 27. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz

Table continues on the next page...

Table 27. Slave mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	21	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	15	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	15	ns

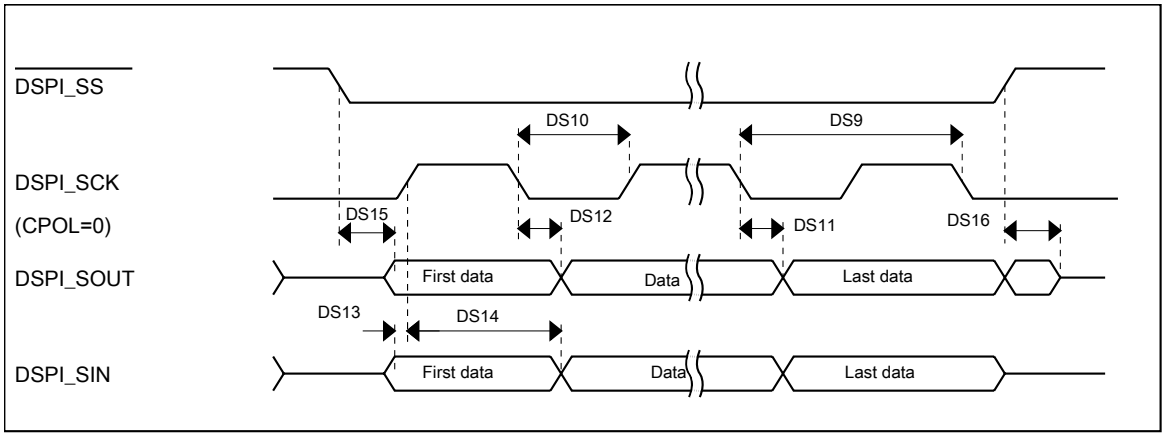


Figure 15. DSPI classic SPI timing — slave mode

3.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 28. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	

Table continues on the next page...

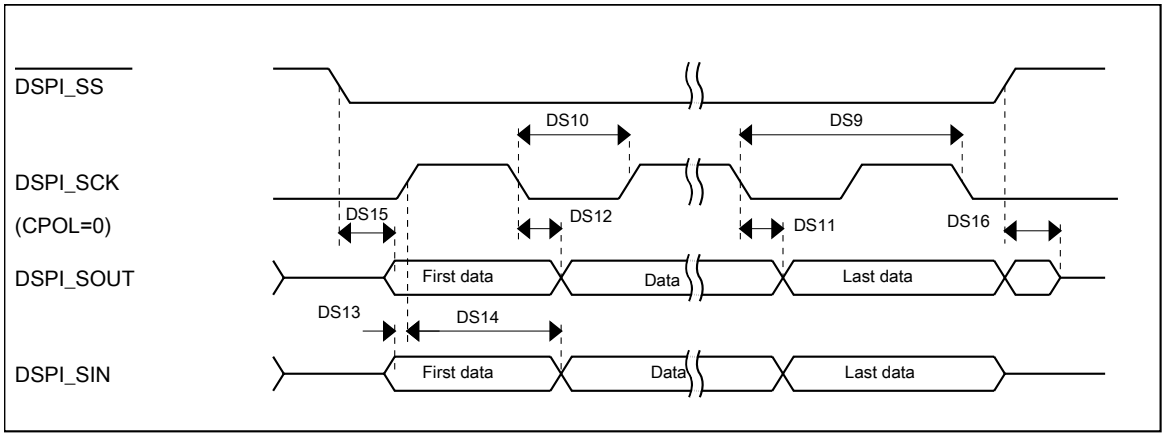


Figure 17. DSPI classic SPI timing — slave mode

3.8.3 I²C

See General switching specifications.

3.8.4 UART

See General switching specifications.

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ASA00473D
32-pin LQFP	98ASH70029A
48-pin LQFP	98ASH00962A

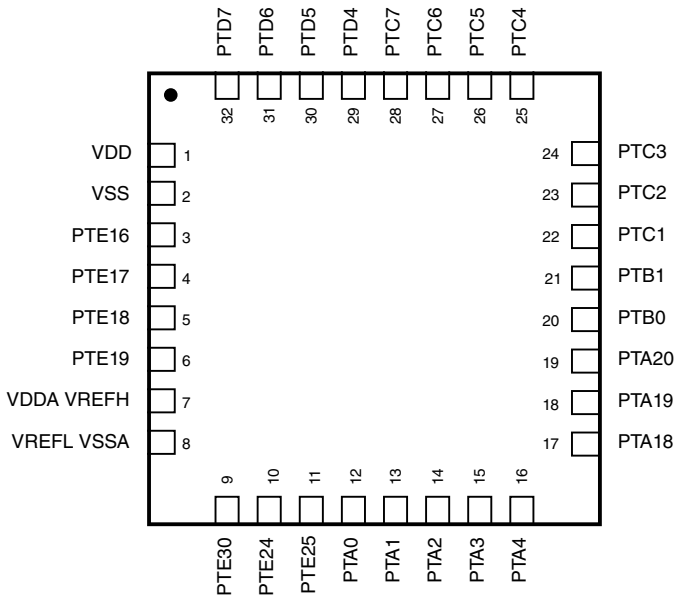


Figure 19. 32 QFN Pinout Diagram

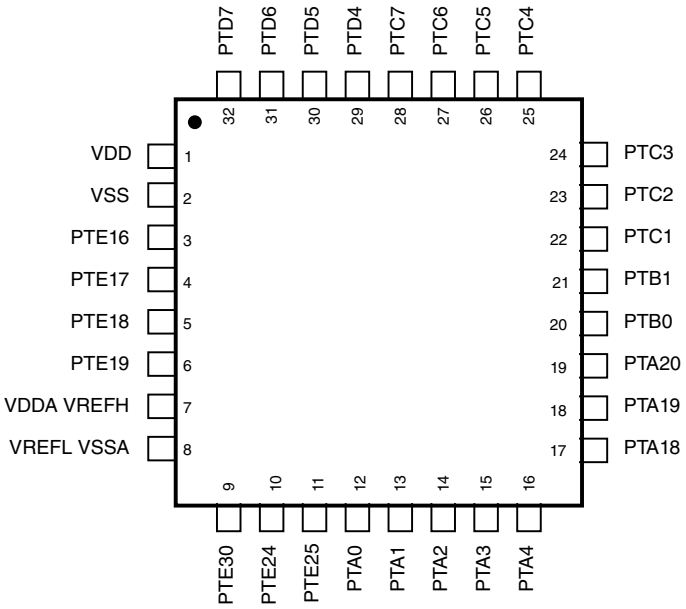


Figure 20. 32 LQFP Pinout Diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the MKV10 device numbers.

7 Part identification

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

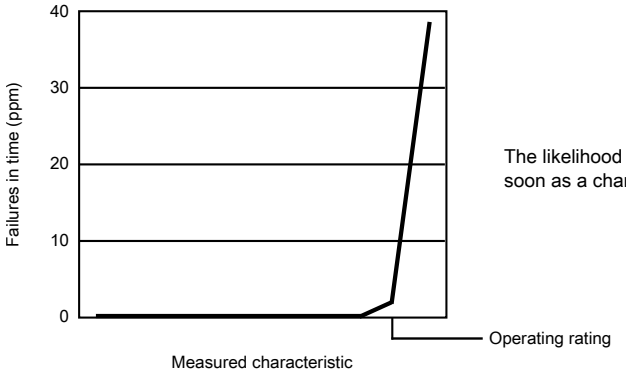
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

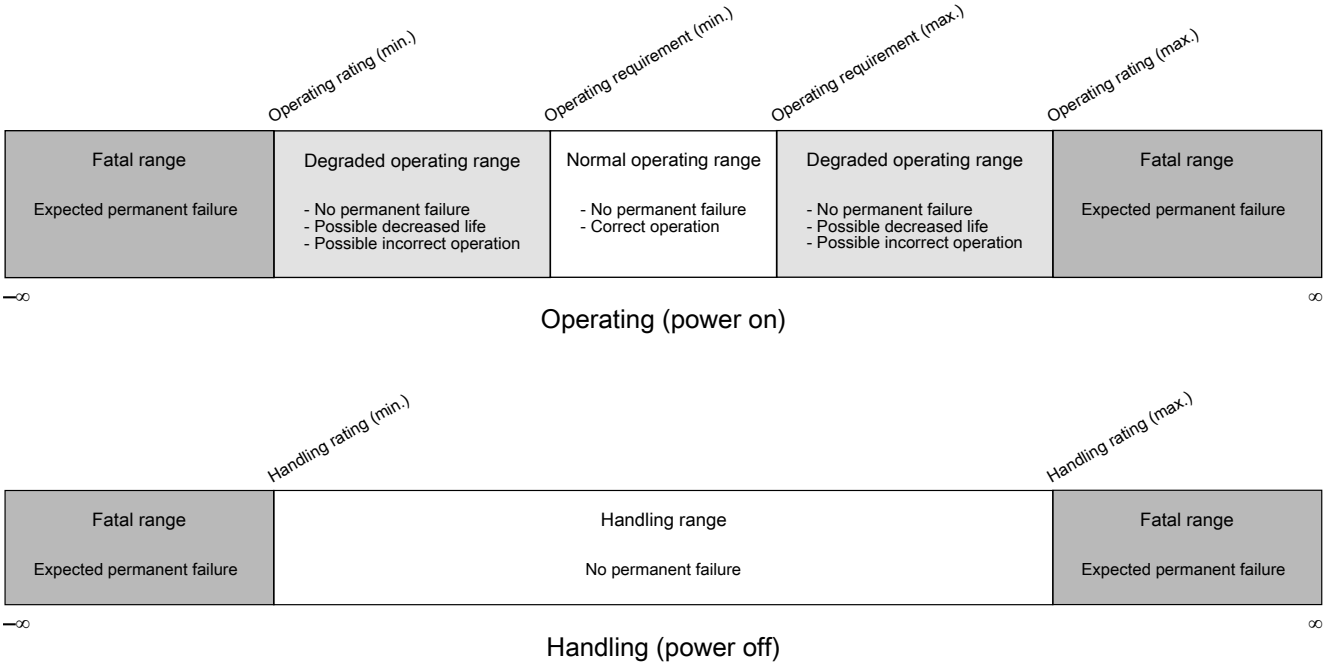
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

8.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

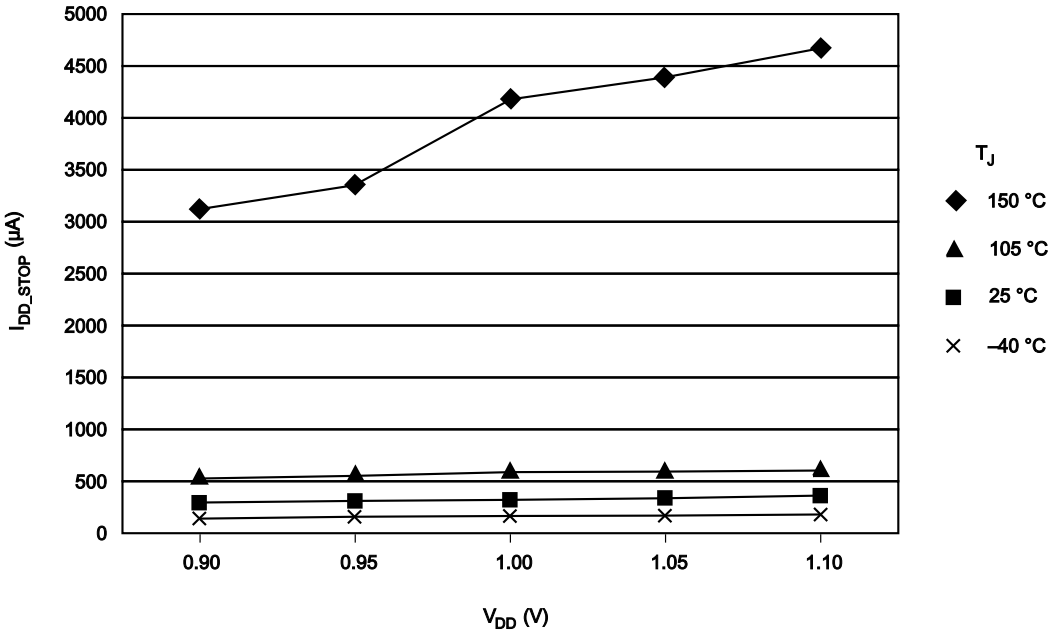
8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.



8.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 30. Revision history

Rev. No.	Date	Substantial Changes
3	02/2014	Initial public release
4	02/2015	• Updated the section "Power consumption operating behaviors" • Added a note below the "Thermal operating requirements" table.