Infineon Technologies - MB96F346RWCPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

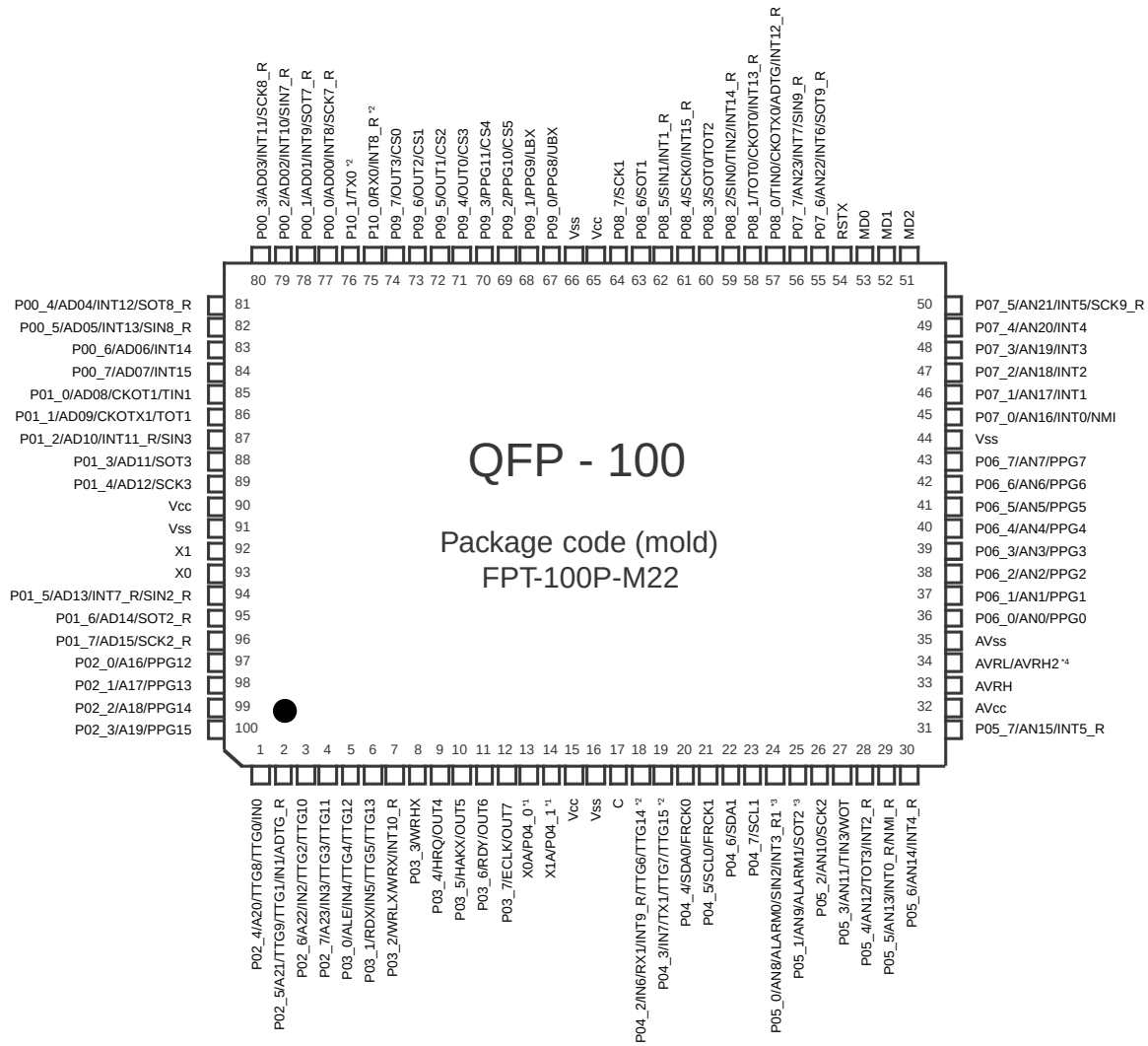
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f346rwcpmc-gse2

■ PIN ASSIGNMENTS

Pin assignment of MB96(F)34x (FPT-100P-M22)



*1: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

*2: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

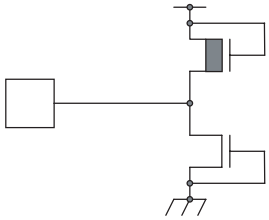
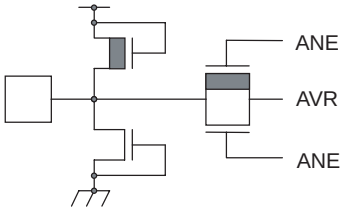
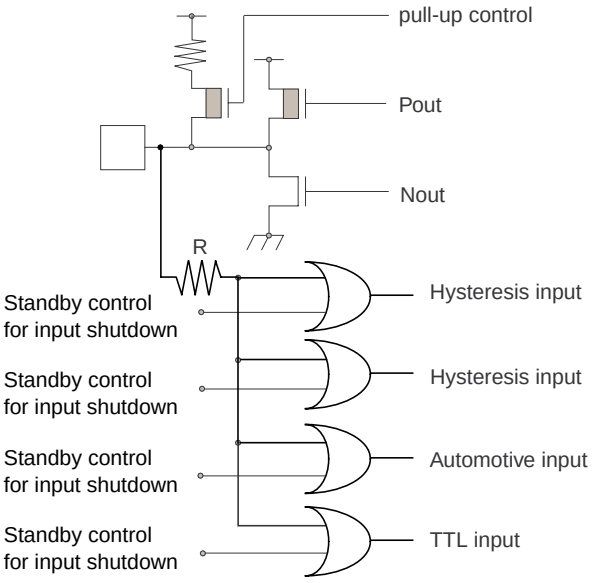
*3: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

*4: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F²MC-16LX family MB90340 series.

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 • Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function * • Automotive input with input shutdown function • TTL input with input shutdown function * • Programmable pull-up resistor: 50kΩ approx. Note: MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

■ USER ROM MEMORY MAP FOR FLASH DEVICES

MB96F345D
MB96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	External bus	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$		
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$		
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$		
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$		
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$		
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$		
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$		
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$		
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$		
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$		
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$		
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$		
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$		
E0:FFFF$_H$ E0:0000$_H$			
DF:FFFF$_H$ DF:8000$_H$		Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K *1	
DE:FFFF$_H$ DE:0000$_H$		Reserved	
0E:FFFF$_H$ 0E:FF00$_H$	(0E:FFFF$_H$) (0E:FF00$_H$)	SDA0-256 *2	Data Flash A
0E:FEFF$_H$ 0E:0000$_H$		Reserved	
0D:FFFF$_H$ 0D:C000$_H$	(0F:FFFF$_H$) (0F:C000$_H$)	SDA4-16K	Data Flash A
0D:BFFF$_H$ 0D:8000$_H$	(0F:BFFF$_H$) (0F:8000$_H$)	SDA3-16K	
0D:7FFF$_H$ 0D:4000$_H$	(0F:7FFF$_H$) (0F:4000$_H$)	SDA2-16K	
0D:3FFF$_H$ 0D:0000$_H$	(0F:3FFF$_H$) (0F:0000$_H$)	SDA1-16K	
0C:FFFF$_H$ 0C:0000$_H$		Reserved	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

*2: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address DE:FF00$_H$ - DE:FF2F$_H$

I/O map MB96(F)34x (9 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000E3H	USART3 - Ext. Status Register	ESCR3		R/W
0000E4H	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
0000E5H	USART3 - Baud Rate Generator Register High	BGRH3		R/W
0000E6H	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
0000E7H-0000EFH	Reserved			-
0000F0H-0000FFH	External Bus area	EXTBUS0		R/W
000100H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103H	DMA0 - DMA control register	DMACS0		R/W
000104H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107H	DMA0 - Data counter high byte	DCTH0		R/W
000108H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010AH	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010BH	DMA1 - DMA control register	DMACS1		R/W
00010CH	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
00010DH	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010EH	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010FH	DMA1 - Data counter high byte	DCTH1		R/W
000110H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113H	DMA2 - DMA control register	DMACS2		R/W
000114H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W

I/O map MB96(F)34x (17 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000483H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485H	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487H	I/O Port P07 - Port Output Drive Register	PODR07		R/W
000488H	I/O Port P08 - Port Output Drive Register	PODR08		R/W
000489H	I/O Port P09 - Port Output Drive Register	PODR09		R/W
00048AH	I/O Port P10 - Port Output Drive Register	PODR10		R/W
00048BH-0004A7H	Reserved			-
0004A8H	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
0004A9H	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
0004AAH	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
0004ABH	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
0004ACH	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
0004ADH	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
0004AEH	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
0004AFH	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
0004B0H	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		R/W
0004B1H	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		R/W
0004B2H	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		R/W
0004B3H-0004BBH	Reserved			-
0004BCH	I/O Port P00 - External Pin State Register	EPSR00		R
0004BDH	I/O Port P01 - External Pin State Register	EPSR01		R
0004BEH	I/O Port P02 - External Pin State Register	EPSR02		R
0004BFH	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0H	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1H	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2H	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3H	I/O Port P07 - External Pin State Register	EPSR07		R

I/O map MB96(F)34x (22 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00058B$_H$	PPG10 - Period setting register			W
00058C$_H$	PPG10 - Duty cycle register		PDUT10	W
00058D$_H$	PPG10 - Duty cycle register			W
00058E$_H$	PPG10 - Control status register Low	PCNL10	PCN10	R/W
00058F$_H$	PPG10 - Control status register High	PCNH10		R/W
000590$_H$	PPG11 - Timer register		PTMR11	R
000591$_H$	PPG11 - Timer register			R
000592$_H$	PPG11 - Period setting register		PCSR11	W
000593$_H$	PPG11 - Period setting register			W
000594$_H$	PPG11 - Duty cycle register		PDUT11	W
000595$_H$	PPG11 - Duty cycle register			W
000596$_H$	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597$_H$	PPG11 - Control status register High	PCNH11		R/W
000598$_H$	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599$_H$	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A$_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B$_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C$_H$	PPG12 - Timer register		PTMR12	R
00059D$_H$	PPG12 - Timer register			R
00059E$_H$	PPG12 - Period setting register		PCSR12	W
00059F$_H$	PPG12 - Period setting register			W
0005A0$_H$	PPG12 - Duty cycle register		PDUT12	W
0005A1$_H$	PPG12 - Duty cycle register			W
0005A2$_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3$_H$	PPG12 - Control status register High	PCNH12		R/W
0005A4$_H$	PPG13 - Timer register		PTMR13	R
0005A5$_H$	PPG13 - Timer register			R
0005A6$_H$	PPG13 - Period setting register		PCSR13	W
0005A7$_H$	PPG13 - Period setting register			W
0005A8$_H$	PPG13 - Duty cycle register		PDUT13	W

I/O map MB96(F)34x (25 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00070A$_H$	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
00070B$_H$	CAN0 - Test Register High (reserved)	TESTRH0		R
00070C$_H$	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
00070D$_H$	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
00070E$_H$-00070F$_H$	Reserved			-
000710$_H$	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711$_H$	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712$_H$	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713$_H$	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714$_H$	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W
000715$_H$	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716$_H$	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717$_H$	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718$_H$	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719$_H$	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
00071A$_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
00071B$_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
00071C$_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
00071D$_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
00071E$_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
00071F$_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720$_H$	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721$_H$	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722$_H$	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723$_H$	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724$_H$	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725$_H$	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726$_H$-00073F$_H$	Reserved			-

I/O map MB96(F)34x (27 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000790H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791H	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793H	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794H-00079FH	Reserved			-
0007A0H	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
0007A1H	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
0007A2H	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R
0007A3H	CAN0 - Interrupt Pending 2 Register High	INTPND2H0		R
0007A4H-0007AFH	Reserved			-
0007B0H	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
0007B1H	CAN0 - Message Valid 1 Register High	MSGVAL1H0		R
0007B2H	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
0007B3H	CAN0 - Message Valid 2 Register High	MSGVAL2H0		R
0007B4H-0007CDH	Reserved			-
0007CEH	CAN0 - Output enable register	COER0		R/W
0007CFH-0007FFH	Reserved			-
000800H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803H	CAN1 - Status register High (reserved)	STATRH1		R
000804H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809H	CAN1 - Interrupt Register High	INTRH1		R

I/O map MB96(F)34x (30 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000890H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894H-00089FH	Reserved			-
0008A0H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4H-0008AFH	Reserved			-
0008B0H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1H	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3H	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4H-0008CDH	Reserved			-
0008CEH	CAN1 - Output enable register	COER1		R/W
0008CFH-0009FFH	Reserved			-
000A00H	DMA - IO address block register 0	IOABK0		R/W
000A01H	DMA - IO address block register 1	IOABK1		R/W
000A02H	DMA - IO address block register 2	IOABK2		R/W
000A03H	DMA - IO address block register 3	IOABK3		R/W
000A04H	DMA - IO address block register 4	IOABK4		R/W
000A05H	DMA - IO address block register 5	IOABK5		R/W
000A06H-000BFFH	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading ‘X’.
Registers of resources which are described in this table, but which are not supported by the device, should also be handled as “Reserved”.

11. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

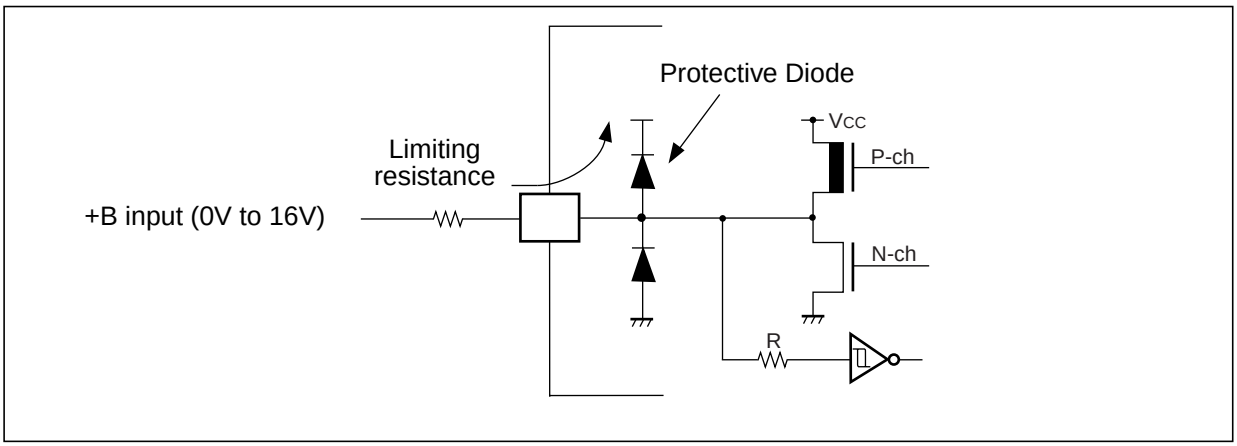
12. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13. Handling of Data Flash

The Data Flash requires different and additional control signals for parallel programming. Please check with your programming equipment maker for support of this interface.

• Sample recommended circuits:



*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \sum (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
I_A is the analog current consumption into AV_{CC}.

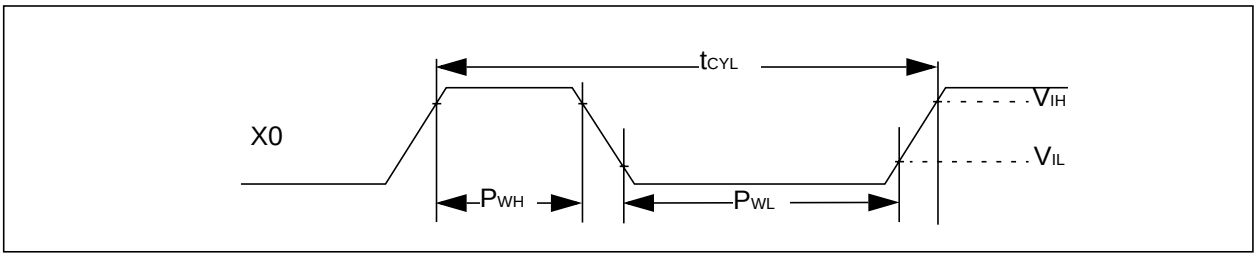
*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

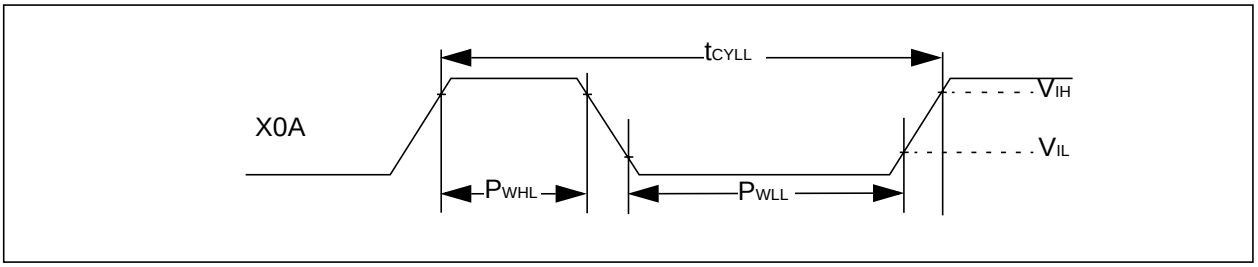
*6: Please contact Fujitsu for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes*	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.35	0.5	mA	MB96345/346
			+125˚C	0.7	2.3		
			+25˚C	0.13	0.2	mA	MB96F345
			+125˚C	0.63	2.2		
			+25˚C	0.35	0.5	mA	MB96F346/F347/F348
			+125˚C	0.85	3.3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.07	0.15	mA	MB96345/346
			+125˚C	0.46	1.9		
			+25˚C	0.07	0.15	mA	MB96F345
			+125˚C	0.6	2.1		
			+25˚C	0.07	0.15	mA	MB96F346/F347/F348
			+125˚C	0.6	2.9		
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.3	0.45	mA	MB96345/346
			+125˚C	0.65	2.2		
			+25˚C	0.08	0.15	mA	MB96F345
			+125˚C	0.58	2.1		
			+25˚C	0.3	0.45	mA	MB96F346/F347/F348
			+125˚C	0.8	3.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.03	0.1	mA	MB96345/346
			+125˚C	0.41	1.85		
			+25˚C	0.03	0.1	mA	MB96F345
			+125˚C	0.53	2.05		
			+25˚C	0.03	0.1	mA	MB96F346/F347/F348
			+125˚C	0.53	2.85		


tCYL
X0
VIH
VIL
PWH
PWL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VIL
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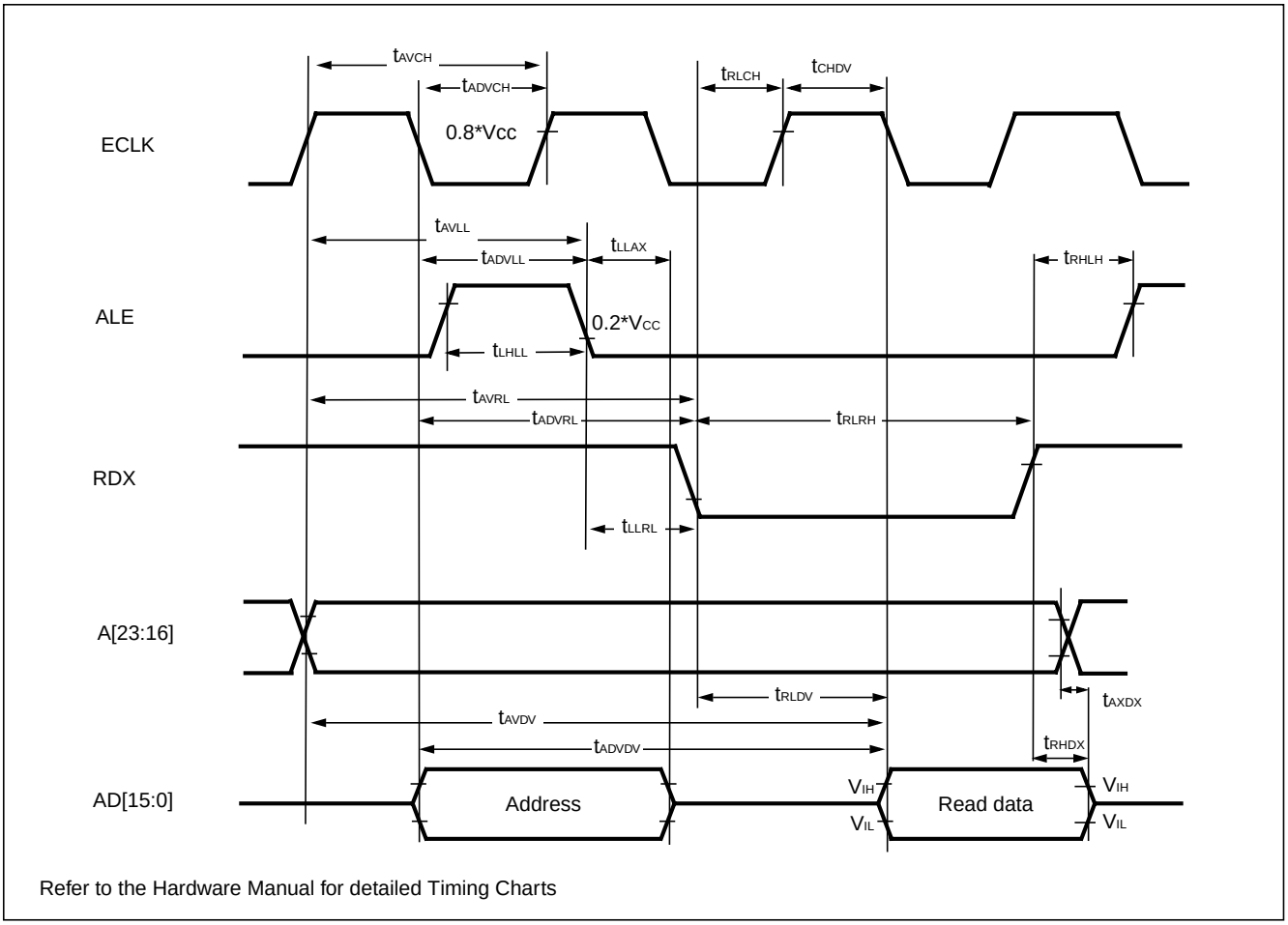


Refer to the Hardware Manual for detailed Timing Charts

Bus Timing (Write)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$ – 15	—	ns	
			EACL:ACE=1	$5t_{CYC}/2$ – 15	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC} – 15	—	ns	
			EACL:ACE=1	$2t_{CYC}$ – 15	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	t_{CYC} – 5	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	t_{CYC} – 20	—	ns	w/o cycle extension

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

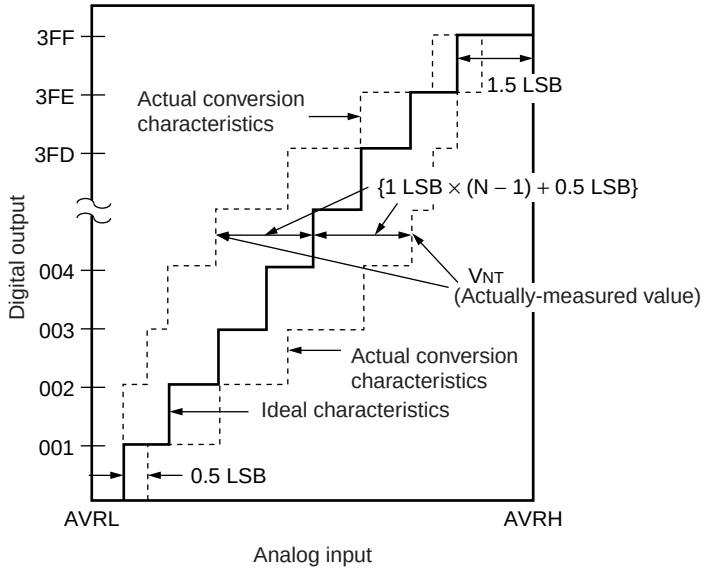
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

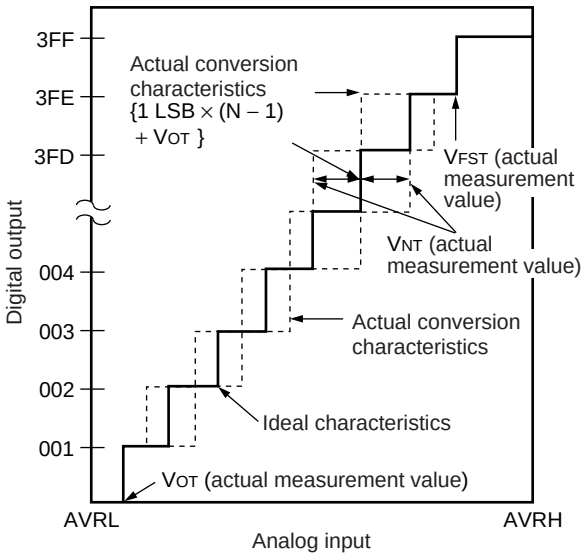
N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

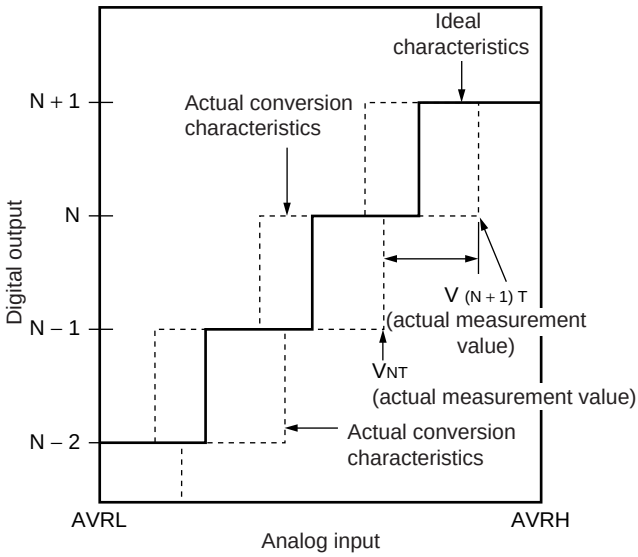
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times\ (N - 1)\ + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

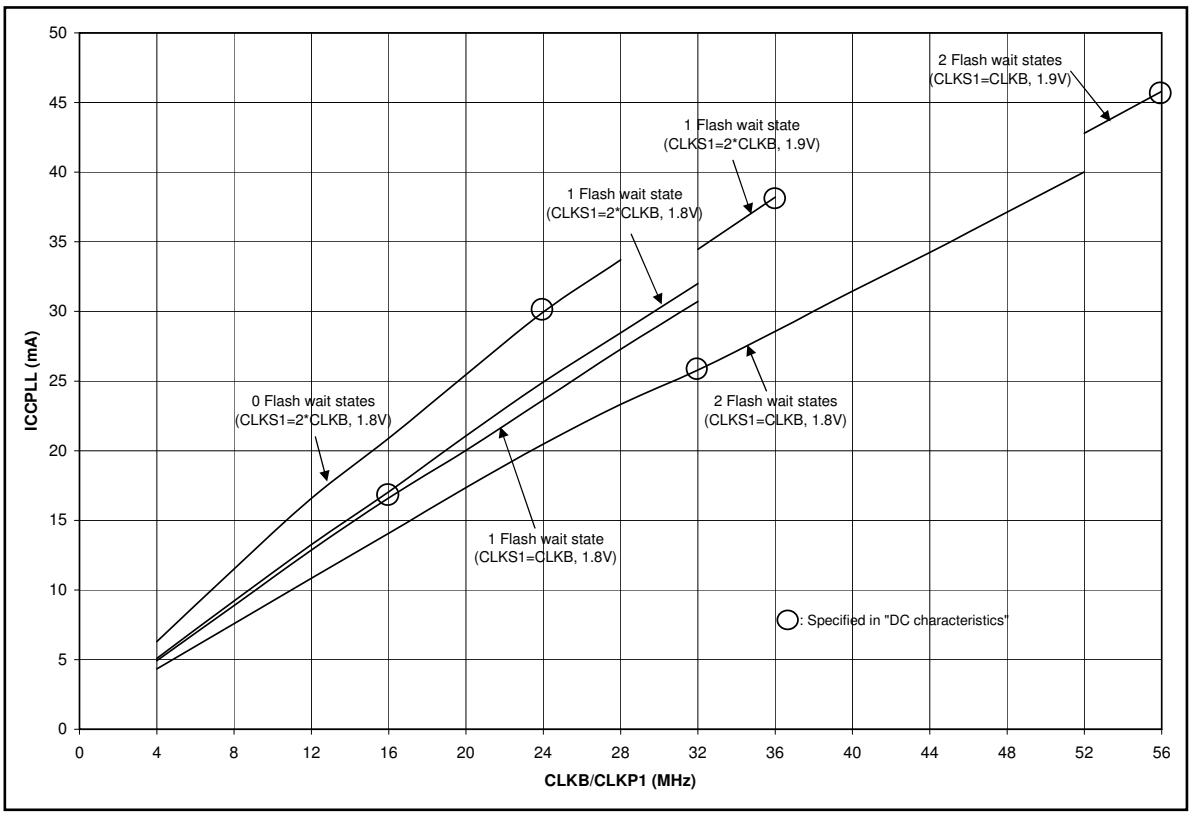
$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

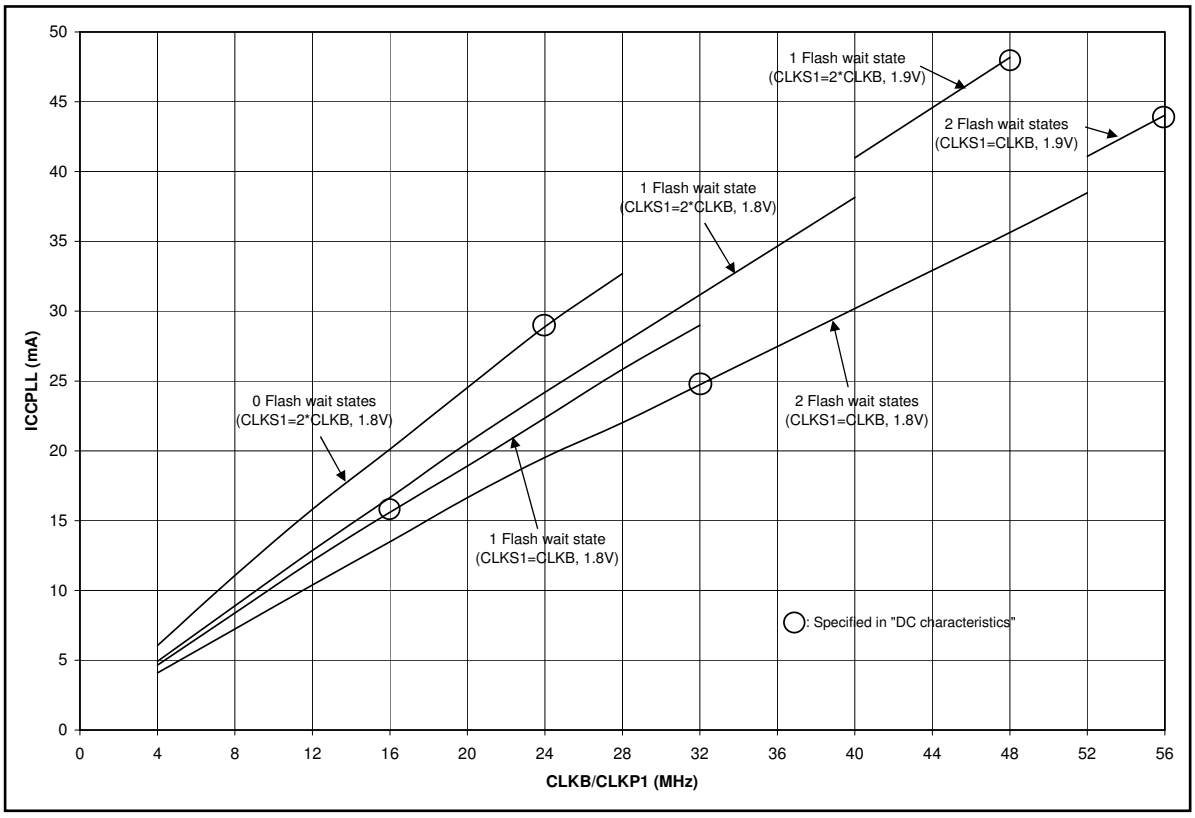
N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

Mode name	Details
PLL Sleep 48	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 96MHz$ • $f_{CLKP1} = 48MHz$ • $f_{CLKP2} = 24MHz$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 40	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 80MHz$ • $f_{CLKP1} = 40MHz$ • $f_{CLKP2} = 20MHz$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 36	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 72MHz$ • $f_{CLKP1} = 36MHz$ • $f_{CLKP2} = 18MHz$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 24	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 48MHz$ • $f_{CLKP1} = f_{CLKP2} = 24MHz$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Sleep	Main Sleep mode current $I_{CCSMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 4MHz$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, RC oscillator and Sub oscillator stopped
RC Sleep 2M	RC Sleep mode current I_{CCSRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 2MHz$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, Main oscillator and Sub oscillator stopped
RC Sleep 100k	RC Sleep mode current I_{CCSRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 100kHz$ • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped

MB96F346/F347/F348Y/R/A PLL Run mode currents



MB96F348T/H/C PLL Run mode currents



MB96F346ASA, MB96F346AWA,
MB96F347ASA, MB96F347AWA,
MB96F348ASA, MB96F348AWA,
MB96F348CSB, MB96F348CWB

Revision	Date	Modification
9	2009-01-09	• Format adjusted to official Fujitsu Microelectronics datasheet standard (mainly style changes and official notes and disclaimer added) • Numbering of Electrical Characteristics subchapters automated • Note about devices under development modified • I/O map: Note added about reserved addresses • ICCSPLL for CLKS1=96MHz mode: increased by 1mA • Serial programming interface: Note about handshaking pins improved • specified AD converter channel offset to 4LSB • package code of MB96V300 corrected in ordering information • Added voltage condition to pull-up resistance spec • Lineup: Term “Data Flash” replaced by “independent 32KB Flash” • Ordering information: column “Independent 32KB Data Flash” replaced by new column “Flash/ROM”, column “Remarks” removed • Official package dimension drawing with additional notes added • Empty pages removed • Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time and power-up stabilization time newly added • Handling devices: Notes added about Serial communication and about using ceramic resonators. • Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor • AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz • VOL3 spec improved: spec valid for 3mA load for full Vcc range • MB96F345 added • Preliminary DC spec of MB96345/346 added • Permitted power dissipation of Flash devices in QFP package improved • C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted • “Preliminary” watermark removed