Infineon Technologies - MB96F346RWCPQC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f346rwcpqc-gse2

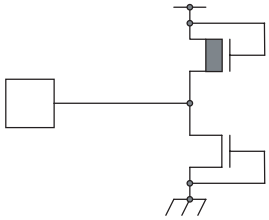
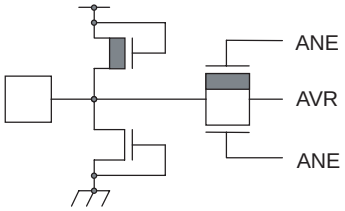
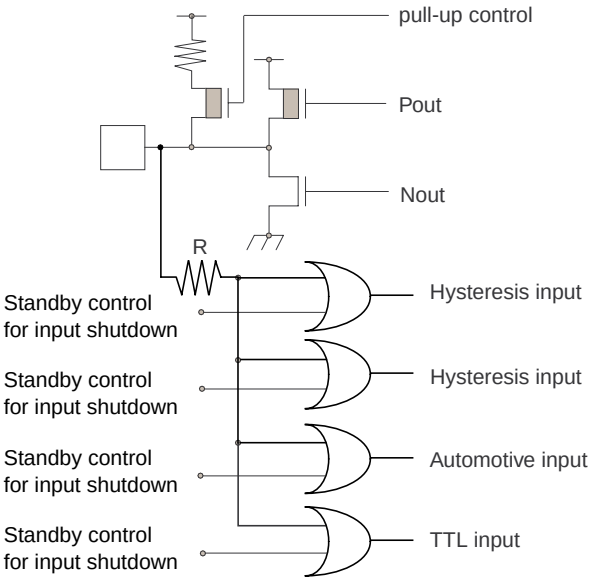
■ PIN CIRCUIT TYPE

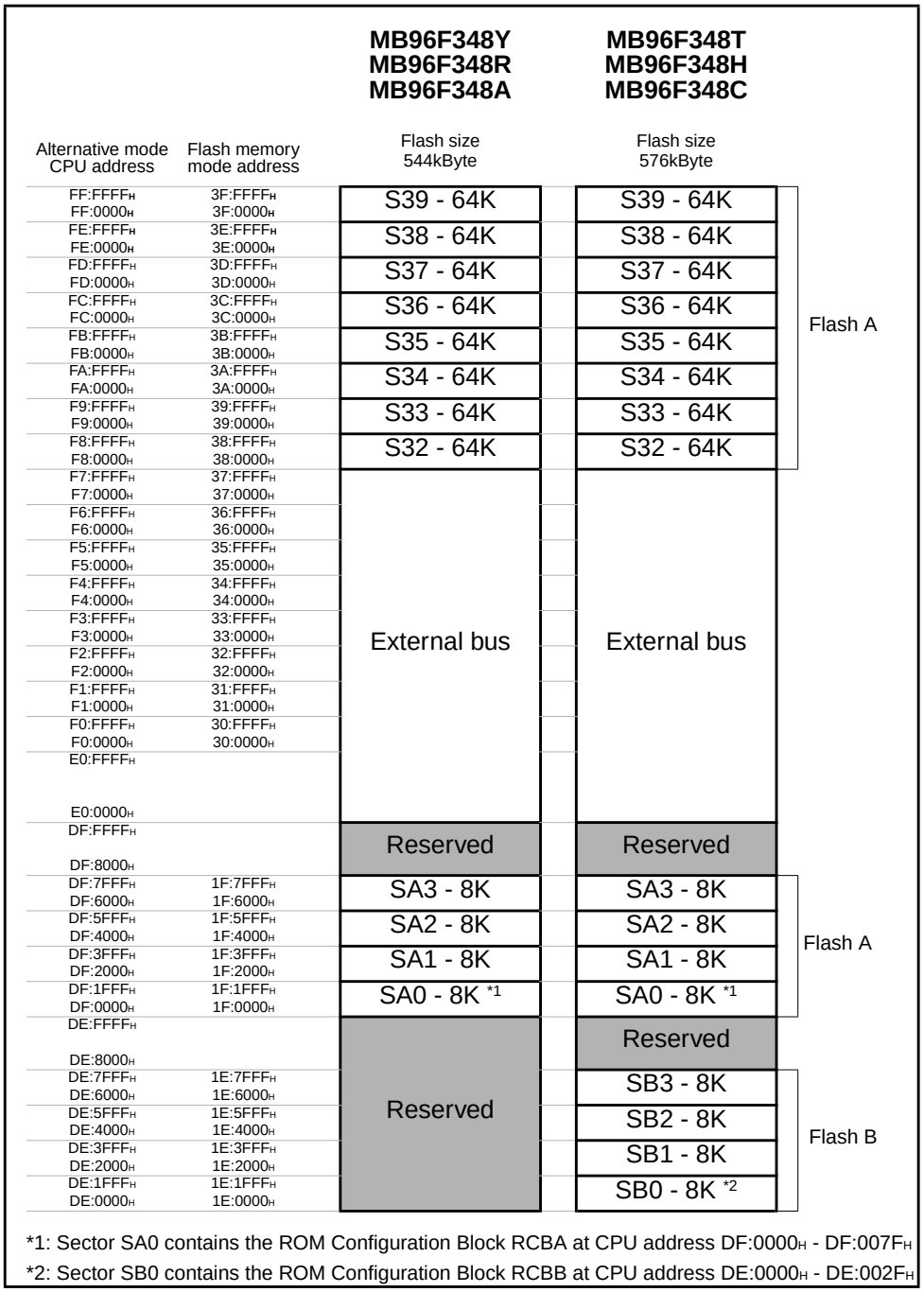
Pin circuit types

FPT-100P-M20	
Pin no.	Circuit type *1
1-10	H
11,12	B *2
11,12	H *3
13,14	Supply
15	F
16,17	H
18-21	N
22-29	I
30	Supply
31-32	G
33	Supply
34 to 41	I
42	Supply
43 to 48	I
49 to 51	C
52	E
53 to 54	I
55 to 62	H
63, 64	Supply
65 to 87	H
88,89	Supply
90, 91	A
92-100	H

FPT-100P-M22	
Pin no.	Circuit type *1
1-12	H
13, 14	B *2
13, 14	H *3
15,16	Supply
17	F
18,19	H
20-23	N
24-31	I
32	Supply
33-34	G
35	Supply
36 to 43	I
44	Supply
45 to 50	I
51 to 53	C
54	E
55 to 56	I
57 to 64	H
65, 66	Supply
67 to 89	H
90, 91	Supply
92, 93	A
94 to 100	H

*1: Please refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types
*2: Devices with suffix ”W”
*3: Devices without suffix ”W”

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 • Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function * • Automotive input with input shutdown function • TTL input with input shutdown function * • Programmable pull-up resistor: 50kΩ approx. Note: MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000H - DF:007FH

*2: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000H - DE:002FH

I/O map MB96(F)34x (18 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004C4H	I/O Port P08 - External Pin State Register	EPSR08		R
0004C5H	I/O Port P09 - External Pin State Register	EPSR09		R
0004C6H	I/O Port P10 - External Pin State Register	EPSR10		R
0004C7H-0004CFH	Reserved			-
0004D0H	ADC analog input enable register 0	ADER0		R/W
0004D1H	ADC analog input enable register 1	ADER1		R/W
0004D2H	ADC analog input enable register 2	ADER2		R/W
0004D3H	ADC analog input enable register 3	ADER3		R/W
0004D4H	ADC analog input enable register 4	ADER4		R/W
0004D5H	Reserved			-
0004D6H	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7H	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8H	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9H	Peripheral Resource Relocation Register 3	PRRR3		R/W
0004DAH	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DBH	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DCH	Peripheral Resource Relocation Register 6	PRRR6		R/W
0004DDH	Peripheral Resource Relocation Register 7	PRRR7		R/W
0004DEH	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DFH	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0H	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1H	RTC - Sub Second Register M	WTBRH0		R/W
0004E2H	RTC - Sub-Second Register H	WTBR1		R/W
0004E3H	RTC - Second Register	WTSR		R/W
0004E4H	RTC - Minutes	WTMR		R/W
0004E5H	RTC - Hour	WTHR		R/W
0004E6H	RTC - Timer Control Extended Register	WTCER		R/W
0004E7H	RTC - Clock select register	WTCKSR		R/W
0004E8H	RTC - Timer Control Register Low	WTCRL	WTCR	R/W

I/O map MB96(F)34x (28 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00080A$_H$	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
00080B$_H$	CAN1 - Test Register High (reserved)	TESTRH1		R
00080C$_H$	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
00080D$_H$	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
00080E$_H$-00080F$_H$	Reserved			-
000810$_H$	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811$_H$	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812$_H$	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813$_H$	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814$_H$	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815$_H$	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816$_H$	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817$_H$	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818$_H$	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819$_H$	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
00081A$_H$	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
00081B$_H$	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
00081C$_H$	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
00081D$_H$	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
00081E$_H$	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
00081F$_H$	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820$_H$	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821$_H$	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W
000822$_H$	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W
000823$_H$	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824$_H$	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825$_H$	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W
000826$_H$-00083F$_H$	Reserved			-

I/O map MB96(F)34x (30 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000890H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894H-00089FH	Reserved			-
0008A0H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4H-0008AFH	Reserved			-
0008B0H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1H	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3H	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4H-0008CDH	Reserved			-
0008CEH	CAN1 - Output enable register	COER1		R/W
0008CFH-0009FFH	Reserved			-
000A00H	DMA - IO address block register 0	IOABK0		R/W
000A01H	DMA - IO address block register 1	IOABK1		R/W
000A02H	DMA - IO address block register 2	IOABK2		R/W
000A03H	DMA - IO address block register 3	IOABK3		R/W
000A04H	DMA - IO address block register 4	IOABK4		R/W
000A05H	DMA - IO address block register 5	IOABK5		R/W
000A06H-000BFFH	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading ‘X’.
Registers of resources which are described in this table, but which are not supported by the device, should also be handled as “Reserved”.

Interrupt vector table MB96(F)34x (3 of 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
55	320H	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG
56	31CH	ICU0	Yes	56	Input Capture Unit 0
57	318H	ICU1	Yes	57	Input Capture Unit 1
58	314H	ICU2	Yes	58	Input Capture Unit 2
59	310H	ICU3	Yes	59	Input Capture Unit 3
60	30CH	ICU4	Yes	60	Input Capture Unit 4
61	308H	ICU5	Yes	61	Input Capture Unit 5
62	304H	ICU6	Yes	62	Input Capture Unit 6
63	300H	ICU7	Yes	63	Input Capture Unit 7
64	2FCH	OCU0	Yes	64	Output Compare Unit 0
65	2F8H	OCU1	Yes	65	Output Compare Unit 1
66	2F4H	OCU2	Yes	66	Output Compare Unit 2
67	2F0H	OCU3	Yes	67	Output Compare Unit 3
68	2ECH	OCU4	Yes	68	Output Compare Unit 4
69	2E8H	OCU5	Yes	69	Output Compare Unit 5
70	2E4H	OCU6	Yes	70	Output Compare Unit 6
71	2E0H	OCU7	Yes	71	Output Compare Unit 7
72	2DCH	FRT0	Yes	72	Free Running Timer 0
73	2D8H	FRT1	Yes	73	Free Running Timer 1
74	2D4H	IIC0	Yes	74	I2C interface
75	2D0H	IIC1	Yes	75	I2C interface
76	2CCH	ADC0	Yes	76	A/D Converter
77	2C8H	ALARM0	No	77	Alarm Comparator 0 (except MB96F345Dyy or MB96F345Fyy)
78	2C4H	ALARM1	No	78	Alarm Comparator 1 (except MB96F345Dyy or MB96F345Fyy)
79	2C0H	LINR0	Yes	79	LIN USART 0 RX
80	2BCH	LINT0	Yes	80	LIN USART 0 TX
81	2B8H	LINR1	Yes	81	LIN USART 1 RX
82	2B4H	LINT1	Yes	82	LIN USART 1 TX

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

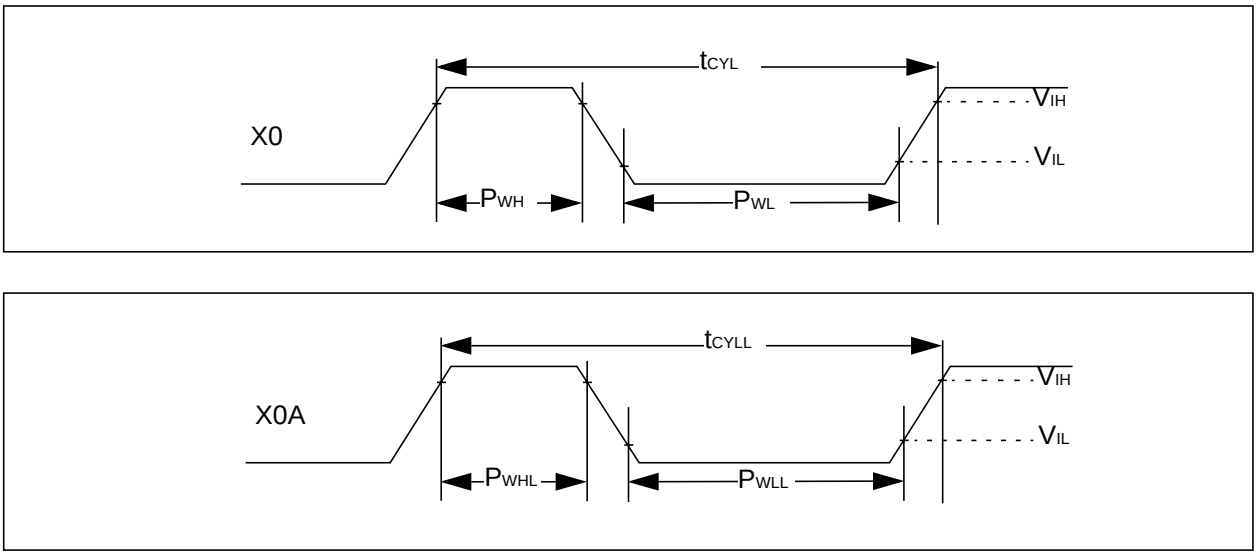
Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes*	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25˚C	0.035	0.1	mA	MB96345/346
			+125˚C	0.42	1.85		
			+25˚C	0.035	0.1	mA	MB96F345
			+125˚C	0.53	2.05		
			+25˚C	0.035	0.1	mA	MB96F346/F347/F348
			+125˚C	0.53	2.85		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25˚C	0.02	0.08	mA	MB96345/346
			+125˚C	0.4	1.8		
			+25˚C	0.02	0.08	mA	MB96F345
			+125˚C	0.52	2.0		
			+25˚C	0.02	0.08	mA	MB96F346/F347/F348
			+125˚C	0.52	2.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25˚C	0.015	0.06	mA	MB96345/346
			+125˚C	0.3	1.4		
			+25˚C	0.015	0.06	mA	MB96F345
			+125˚C	0.4	1.5		
			+25˚C	0.015	0.06	mA	MB96F346/F347/F348
			+125˚C	0.4	2.3		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	+25˚C	5	10	µA	MB96F345
			+125˚C	7	20	µA	Must be added to all current above
			+25˚C	90	140	µA	Other devices
			+125˚C	100	150		Must be added to all current above
Power supply current for active Clock modulator	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/ Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
	$I_{CCDFLASH}$	Current for one Data Flash module		10	20	mA	Must be added to all current above

4. AC Characteristics

Source Clock timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

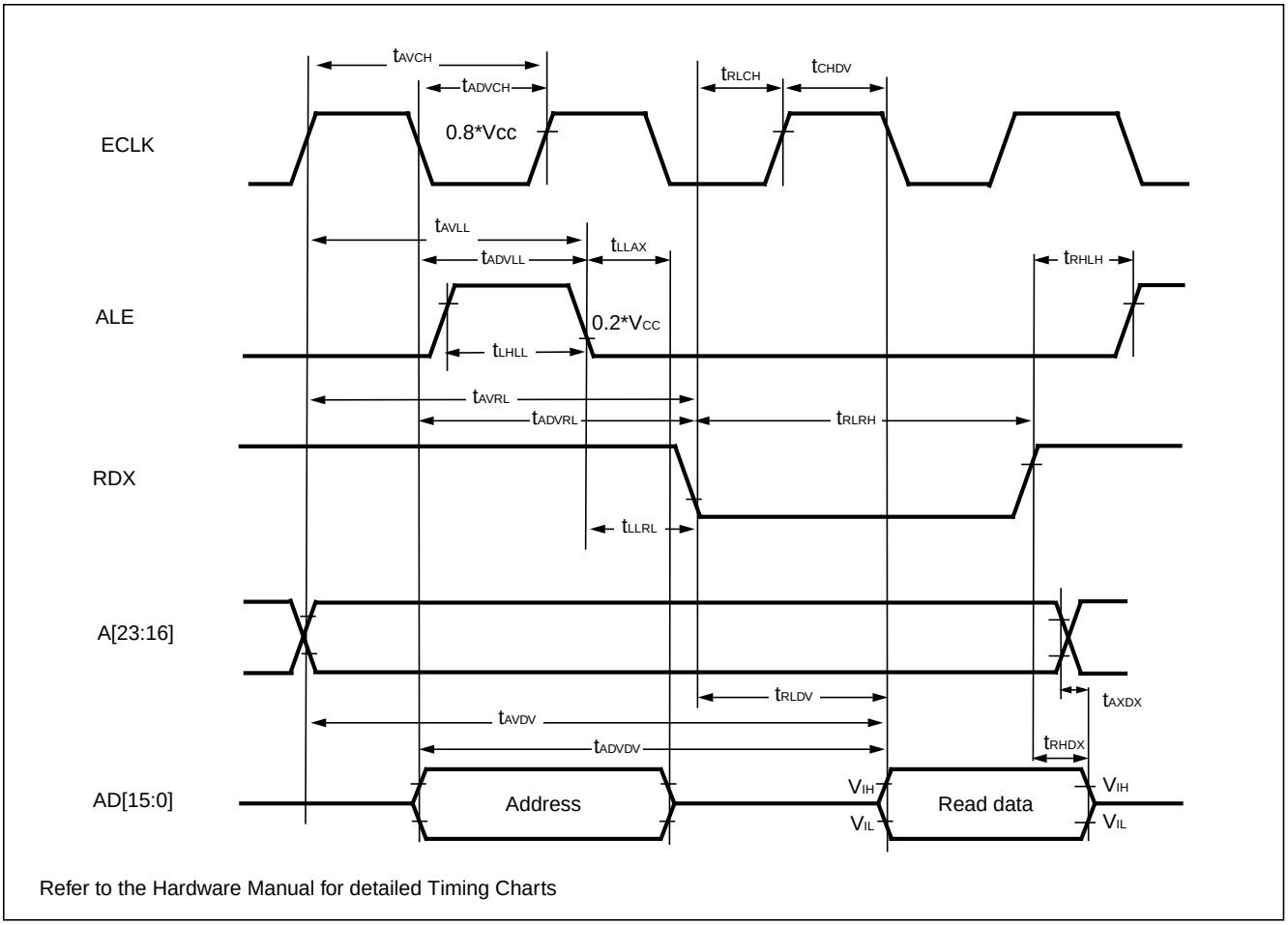
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” (not available in MB96F34xY/R/AxA), PLL off
			3.5	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” (not available in MB96F34xY/R/AxA), PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	-	64 or 256 RC clock cycles				Applied after any reset and when activating the RC oscillator. MB96F345: 256 cycles others 64 cycles
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) ≥ 4MHz, jitter coming from external oscillator, crystal or resonator is not covered
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	


tCYL
X0
VIH
VIL
PWH
PWL

tCYLL
X0A
VIH
VIL
PWHL
PWLL

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	—	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	—	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		



Refer to the Hardware Manual for detailed Timing Charts

Bus Timing (Write)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$ – 15	—	ns	
			EACL:ACE=1	$5t_{CYC}/2$ – 15	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC} – 15	—	ns	
			EACL:ACE=1	$2t_{CYC}$ – 15	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	t_{CYC} – 5	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	t_{CYC} – 20	—	ns	w/o cycle extension

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	—	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 10$	—	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 10$	—		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	—	$3t_{CYC}/2 - 15$	ns	
			EACL:ACE=1	—	$5t_{CYC}/2 - 15$		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	—	$t_{CYC}/2 - 15$	—	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	$t_{CYC} - 8$	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC} - 25$	—	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 20$	—	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	—	$t_{CYC}/2 - 20$	—	ns	

7. Low Voltage Detector characteristics

(T_A = -40 ˚C to +125 ˚C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value *1		Value *2		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.5	2.9	V	CILCR:LVL[3:0]=”0000”
Level 1	V_{DL1}	2.9	3.1	2.8	3.2	V	CILCR:LVL[3:0]=”0001”
Level 2	V_{DL2}	3.1	3.3	3	3.4	V	CILCR:LVL[3:0]=”0010”
Level 3	V_{DL3}	3.5	3.75	3.35	3.8	V	CILCR:LVL[3:0]=”0011”
Level 4	V_{DL4}	3.6	3.85	3.5	3.95	V	CILCR:LVL[3:0]=”0100”
Level 5	V_{DL5}	3.7	3.95	3.6	4.1	V	CILCR:LVL[3:0]=”0101”
Level 6	V_{DL6}	3.8	4.05	3.7	4.2	V	CILCR:LVL[3:0]=”0110”
Level 7	V_{DL7}	3.9	4.15	3.8	4.3	V	CILCR:LVL[3:0]=”0111”
Level 8	V_{DL8}	4.0	4.25	3.9	4.4	V	CILCR:LVL[3:0]=”1000”
Level 9	V_{DL9}	4.1	4.35	3.95	4.5	V	CILCR:LVL[3:0]=”1001”
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		2.6	3	V	CILCR:LVL[3:0]=”1100”
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

*1: valid for all devices except devices listed under “*2”

*2: valid for: MB96F345

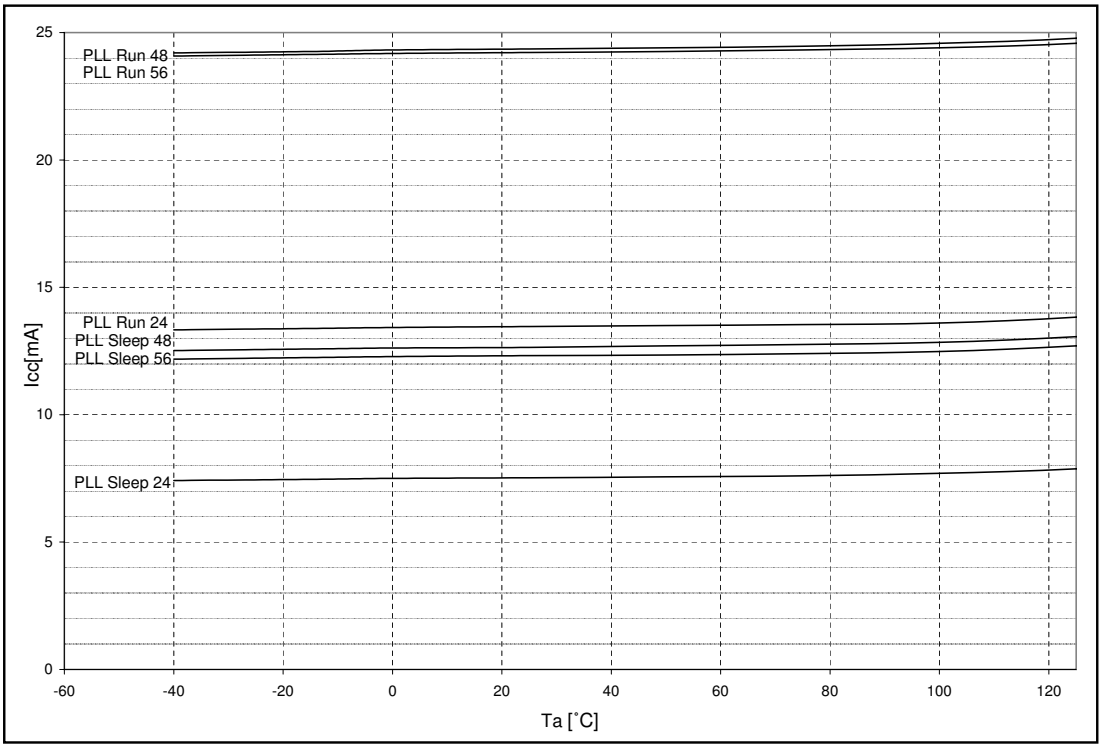
CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004\frac{V}{\mu s}$.

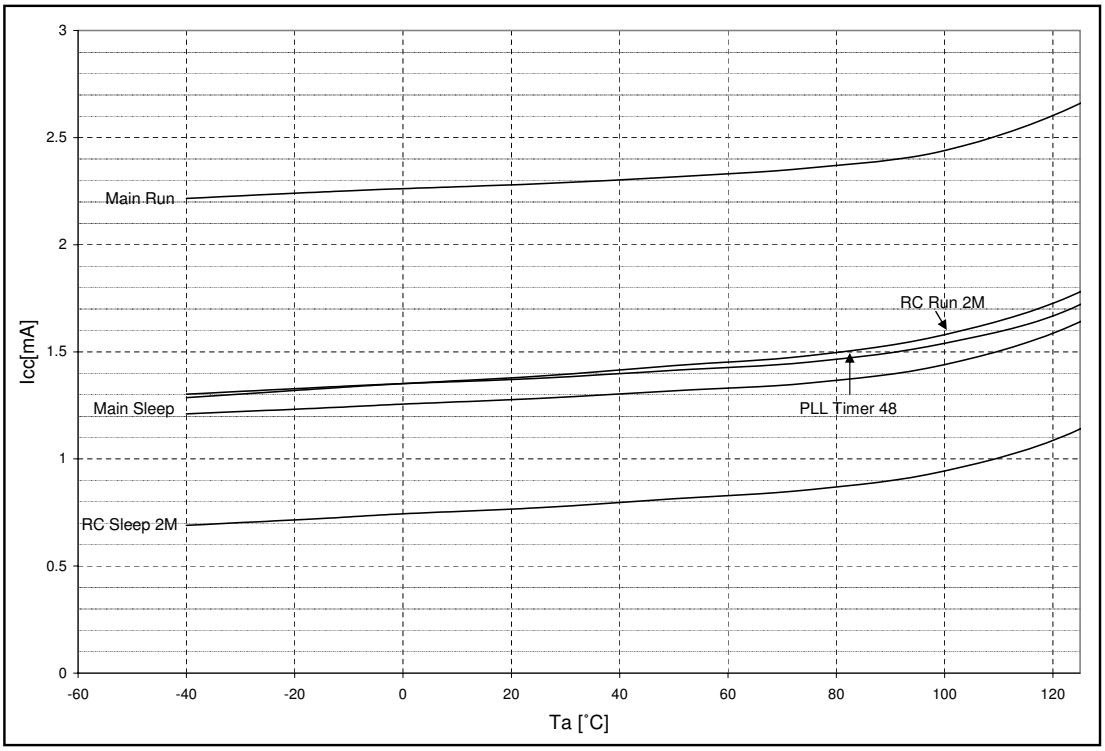
Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of “Level 0” (V_{DL0_MIN}). The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

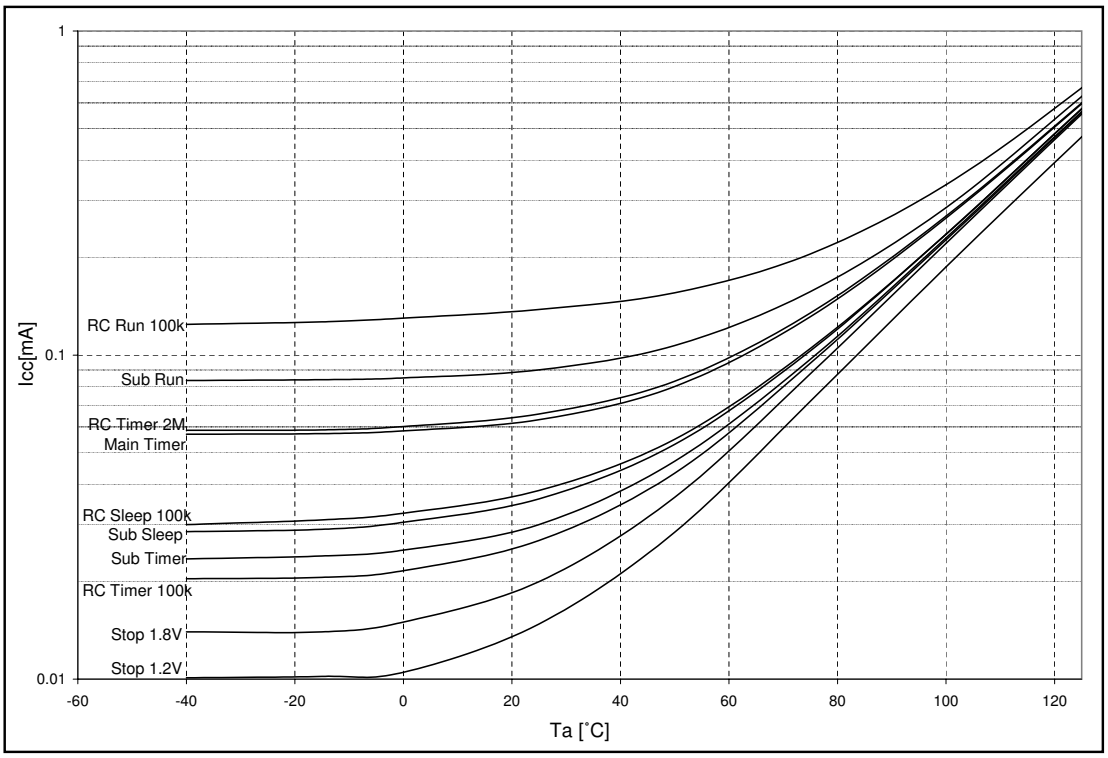
MB96345/346 PLL Run and Sleep mode currents



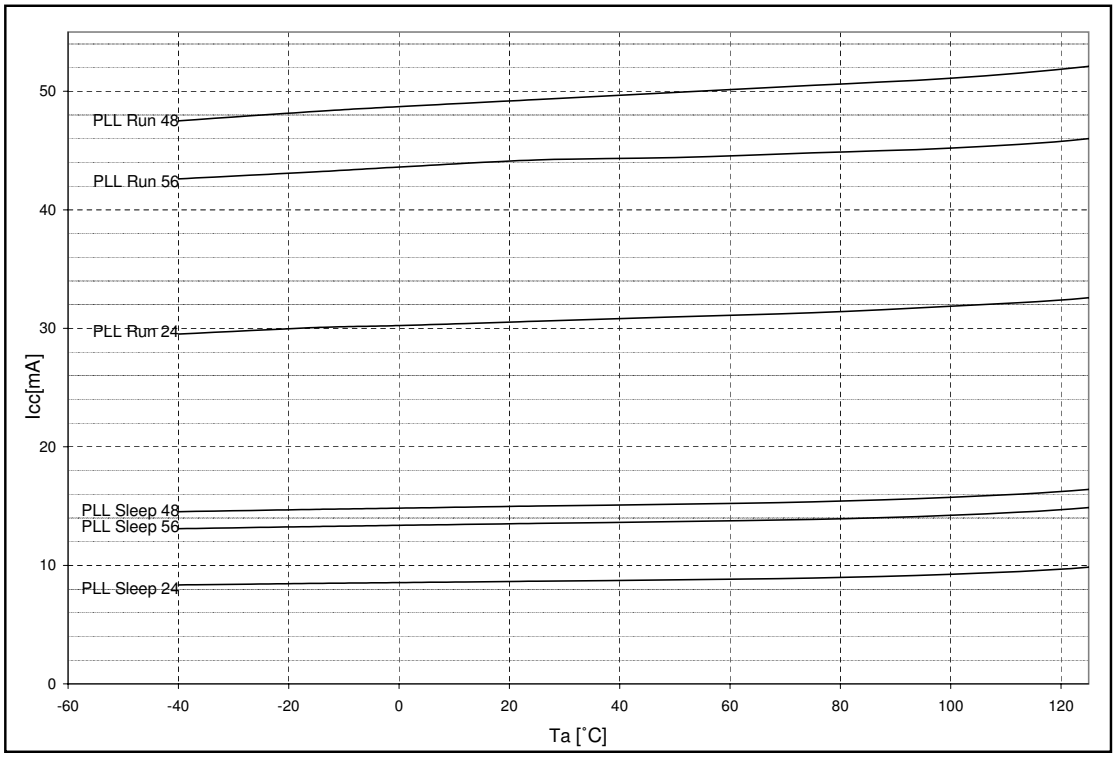
MB96345/346 operation modes with medium currents



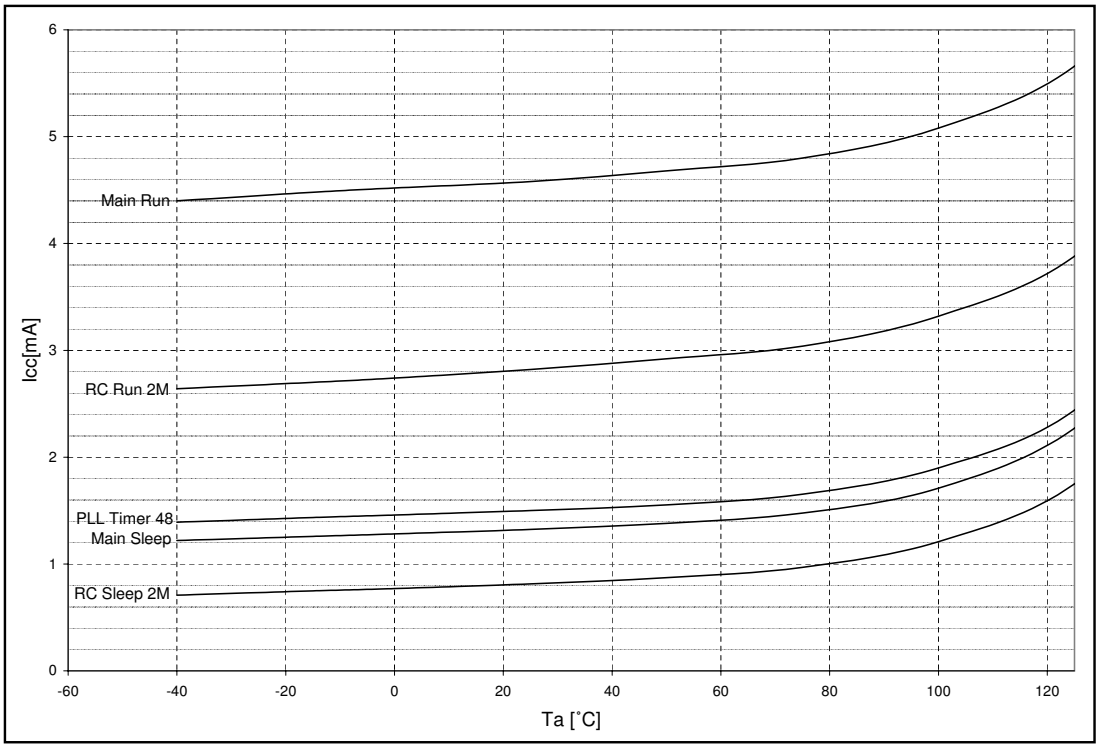
MB96F346/F347/F348Y/R/A Low power mode currents



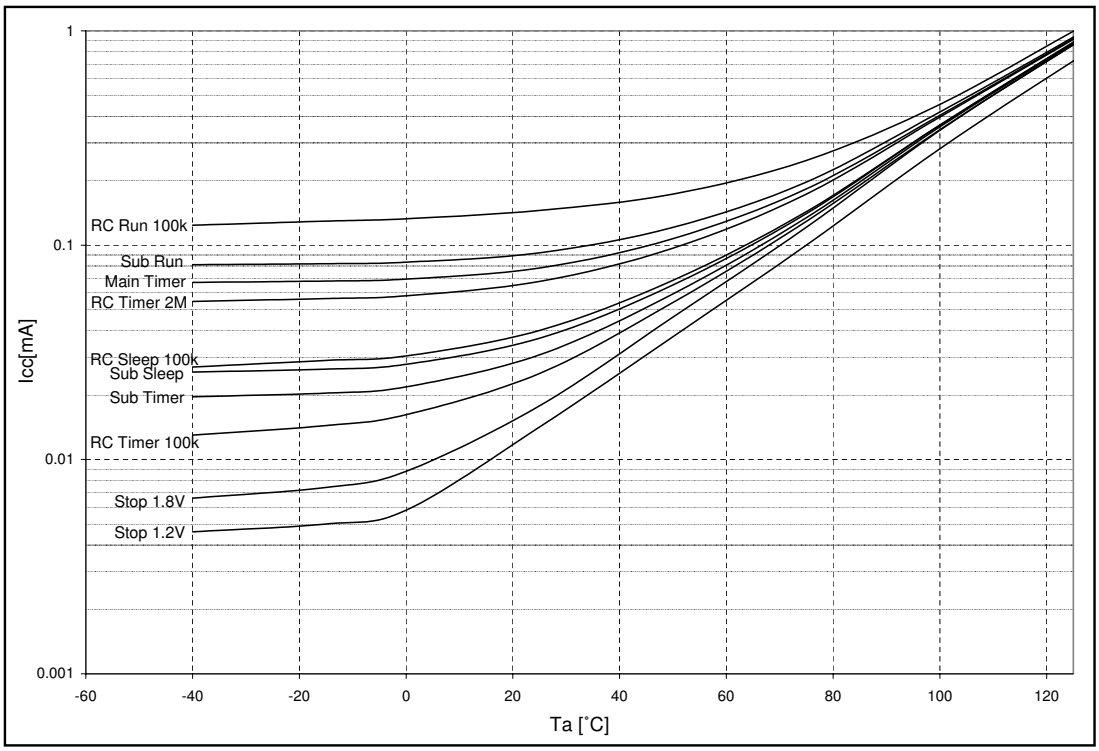
MB96F348T/H/C PLL Run and Sleep mode currents



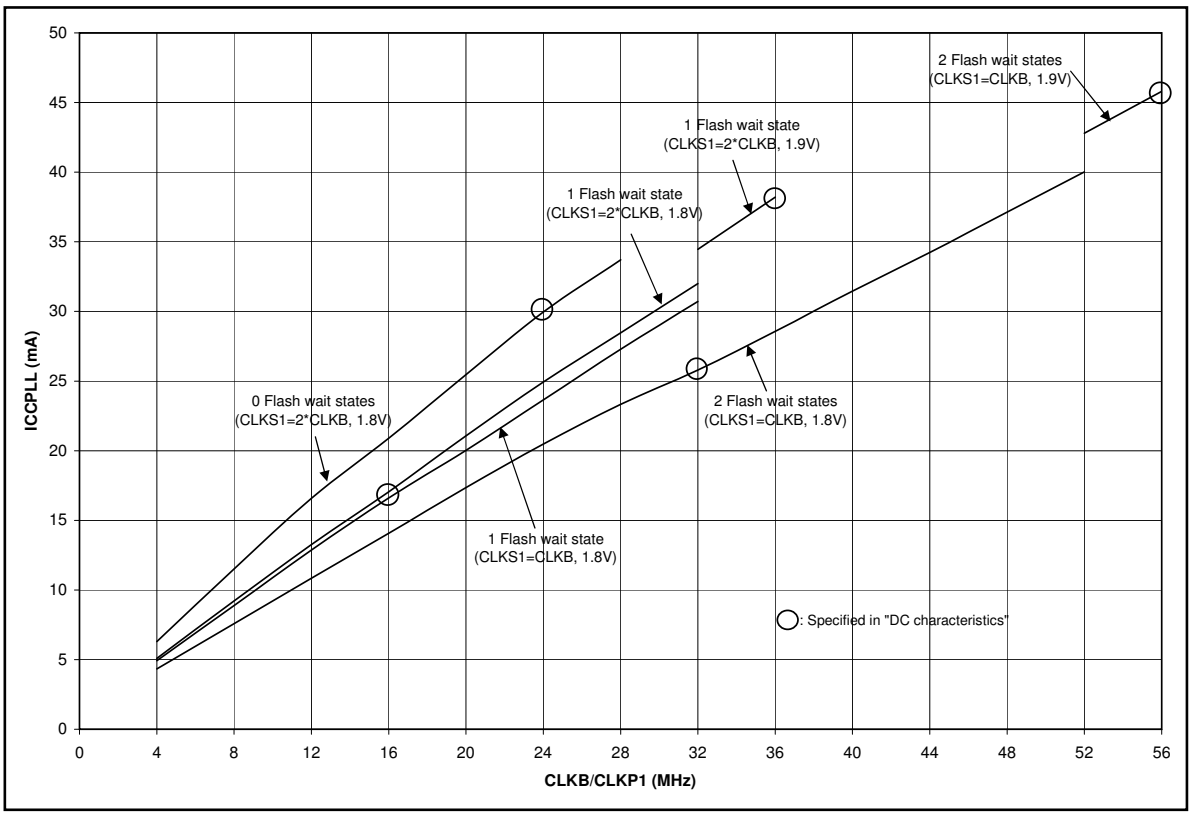
MB96F348T/H/C operation modes with medium currents



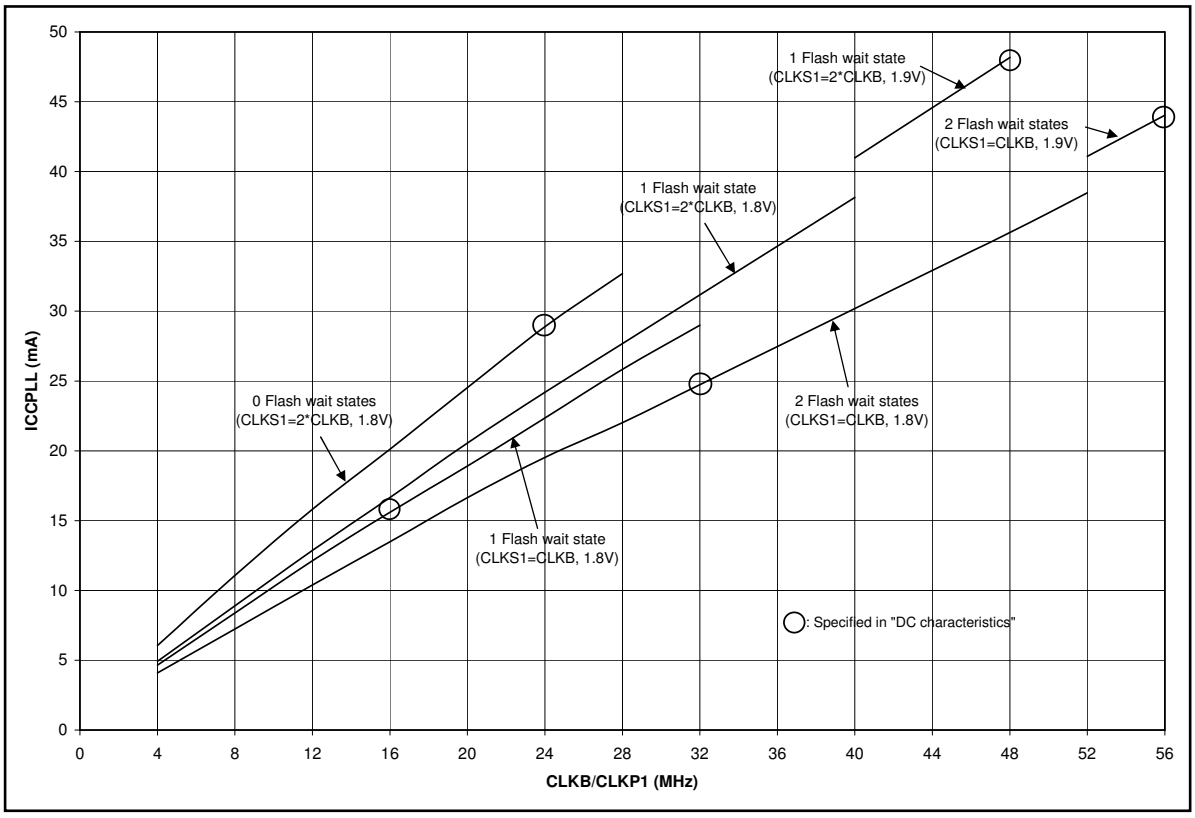
MB96F348T/H/C Low power mode currents



MB96F346/F347/F348Y/R/A PLL Run mode currents



MB96F348T/H/C PLL Run mode currents



MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F346YSB PQC-GSE2	Flash A (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F346RSB PQC-GSE2			No	
MB96F346YWB PQC-GSE2		Yes	Yes	
MB96F346RWB PQC-GSE2			No	
MB96F346YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346RSB PMC-GSE2			No	
MB96F346YWB PMC-GSE2		Yes	Yes	
MB96F346RWB PMC-GSE2			No	
MB96F346YSC PQC-GSE2*1		No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F346RSC PQC-GSE2*1			No	
MB96F346YWC PQC-GSE2*1		Yes	Yes	
MB96F346RWC PQC-GSE2*1			No	
MB96F346YSC PMC-GSE2*1		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346RSC PMC-GSE2*1			No	
MB96F346YWC PMC-GSE2*1		Yes	Yes	
MB96F346RWC PMC-GSE2*1			No	
MB96F347YSB PQC-GSE2	Flash A (416KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F347RSB PQC-GSE2			No	
MB96F347YWB PQC-GSE2		Yes	Yes	
MB96F347RWB PQC-GSE2			No	
MB96F347YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F347RSB PMC-GSE2			No	
MB96F347YWB PMC-GSE2		Yes	Yes	
MB96F347RWB PMC-GSE2			No	
MB96F347YSC PQC-GSE2*1		No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F347RSC PQC-GSE2*1			No	
MB96F347YWC PQC-GSE2*1		Yes	Yes	
MB96F347RWC PQC-GSE2*1			No	
MB96F347YSC PMC-GSE2*1		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F347RSC PMC-GSE2*1			No	
MB96F347YWC PMC-GSE2*1		Yes	Yes	
MB96F347RWC PMC-GSE2*1			No	

■ REVISION HISTORY

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.