Infineon Technologies - MB96F347RSCPMC-GSE2 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347rscpmc-gse2

■ FEATURES

Feature	Description
Technology	• 0.18µm CMOS
CPU	• F²MC-16FX CPU • Up to 56 MHz internal, 17.8 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop) • 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor). • Up to 56 MHz external clock for devices with fast clock input feature • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
DMA	• Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

Feature	Description
I/O Ports	• Virtually all external pins can be used as general purpose I/O • All push-pull outputs (except when used as I2C SDA/SCL line) • Bit-wise programmable as input/output or peripheral signal • Bit-wise programmable input enable • Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices) • Bit-wise programmable pull-up resistor • Bit-wise programmable output driving strength for EMI optimization
Packages	• 100-pin plastic QFP and LQFP
Flash Memory	• Supports automatic programming, Embedded Algorithm • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase

I/O map MB96(F)34x (2 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000026H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028H	OCU0 - Output Compare Control Status	OCS0		R/W
000029H	OCU1 - Output Compare Control Status	OCS1		R/W
00002AH	OCU0 - Compare Register		OCCP0	R/W
00002BH	OCU0 - Compare Register			R/W
00002CH	OCU1 - Compare Register		OCCP1	R/W
00002DH	OCU1 - Compare Register			R/W
00002EH	OCU2 - Output Compare Control Status	OCS2		R/W
00002FH	OCU3 - Output Compare Control Status	OCS3		R/W
000030H	OCU2 - Compare Register		OCCP2	R/W
000031H	OCU2 - Compare Register			R/W
000032H	OCU3 - Compare Register		OCCP3	R/W
000033H	OCU3 - Compare Register			R/W
000034H	OCU4 - Output Compare Control Status	OCS4		R/W
000035H	OCU5 - Output Compare Control Status	OCS5		R/W
000036H	OCU4 - Compare Register		OCCP4	R/W
000037H	OCU4 - Compare Register			R/W
000038H	OCU5 - Compare Register		OCCP5	R/W
000039H	OCU5 - Compare Register			R/W
00003AH	OCU6 - Output Compare Control Status	OCS6		R/W
00003BH	OCU7 - Output Compare Control Status	OCS7		R/W
00003CH	OCU6 - Compare Register		OCCP6	R/W
00003DH	OCU6 - Compare Register			R/W
00003EH	OCU7 - Compare Register		OCCP7	R/W
00003FH	OCU7 - Compare Register			R/W
000040H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041H	ICU0/ICU1 - Edge register	ICE01		R/W
000042H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R

I/O map MB96(F)34x (5 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000072H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075H	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077H	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078H	PPG0 - Timer register		PTMR0	R
000079H	PPG0 - Timer register			R
00007AH	PPG0 - Period setting register		PCSR0	W
00007BH	PPG0 - Period setting register			W
00007CH	PPG0 - Duty cycle register		PDUT0	W
00007DH	PPG0 - Duty cycle register			W
00007EH	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007FH	PPG0 - Control status register High	PCNH0		R/W
000080H	PPG1 - Timer register		PTMR1	R
000081H	PPG1 - Timer register			R
000082H	PPG1 - Period setting register		PCSR1	W
000083H	PPG1 - Period setting register			W
000084H	PPG1 - Duty cycle register		PDUT1	W
000085H	PPG1 - Duty cycle register			W
000086H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087H	PPG1 - Control status register High	PCNH1		R/W
000088H	PPG2 - Timer register		PTMR2	R
000089H	PPG2 - Timer register			R
00008AH	PPG2 - Period setting register		PCSR2	W
00008BH	PPG2 - Period setting register			W
00008CH	PPG2 - Duty cycle register		PDUT2	W

I/O map MB96(F)34x (21 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00056D$_H$	PPG7 - Timer register			R
00056E$_H$	PPG7 - Period setting register		PCSR7	W
00056F$_H$	PPG7 - Period setting register			W
000570$_H$	PPG7 - Duty cycle register		PDUT7	W
000571$_H$	PPG7 - Duty cycle register			W
000572$_H$	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573$_H$	PPG7 - Control status register High	PCNH7		R/W
000574$_H$	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575$_H$	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576$_H$	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577$_H$	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578$_H$	PPG8 - Timer register		PTMR8	R
000579$_H$	PPG8 - Timer register			R
00057A$_H$	PPG8 - Period setting register		PCSR8	W
00057B$_H$	PPG8 - Period setting register			W
00057C$_H$	PPG8 - Duty cycle register		PDUT8	W
00057D$_H$	PPG8 - Duty cycle register			W
00057E$_H$	PPG8 - Control status register Low	PCNL8	PCN8	R/W
00057F$_H$	PPG8 - Control status register High	PCNH8		R/W
000580$_H$	PPG9 - Timer register		PTMR9	R
000581$_H$	PPG9 - Timer register			R
000582$_H$	PPG9 - Period setting register		PCSR9	W
000583$_H$	PPG9 - Period setting register			W
000584$_H$	PPG9 - Duty cycle register		PDUT9	W
000585$_H$	PPG9 - Duty cycle register			W
000586$_H$	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587$_H$	PPG9 - Control status register High	PCNH9		R/W
000588$_H$	PPG10 - Timer register		PTMR10	R
000589$_H$	PPG10 - Timer register			R
00058A$_H$	PPG10 - Period setting register		PCSR10	W

I/O map MB96(F)34x (22 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00058B$_H$	PPG10 - Period setting register			W
00058C$_H$	PPG10 - Duty cycle register		PDUT10	W
00058D$_H$	PPG10 - Duty cycle register			W
00058E$_H$	PPG10 - Control status register Low	PCNL10	PCN10	R/W
00058F$_H$	PPG10 - Control status register High	PCNH10		R/W
000590$_H$	PPG11 - Timer register		PTMR11	R
000591$_H$	PPG11 - Timer register			R
000592$_H$	PPG11 - Period setting register		PCSR11	W
000593$_H$	PPG11 - Period setting register			W
000594$_H$	PPG11 - Duty cycle register		PDUT11	W
000595$_H$	PPG11 - Duty cycle register			W
000596$_H$	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597$_H$	PPG11 - Control status register High	PCNH11		R/W
000598$_H$	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599$_H$	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A$_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B$_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C$_H$	PPG12 - Timer register		PTMR12	R
00059D$_H$	PPG12 - Timer register			R
00059E$_H$	PPG12 - Period setting register		PCSR12	W
00059F$_H$	PPG12 - Period setting register			W
0005A0$_H$	PPG12 - Duty cycle register		PDUT12	W
0005A1$_H$	PPG12 - Duty cycle register			W
0005A2$_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3$_H$	PPG12 - Control status register High	PCNH12		R/W
0005A4$_H$	PPG13 - Timer register		PTMR13	R
0005A5$_H$	PPG13 - Timer register			R
0005A6$_H$	PPG13 - Period setting register		PCSR13	W
0005A7$_H$	PPG13 - Period setting register			W
0005A8$_H$	PPG13 - Duty cycle register		PDUT13	W

I/O map MB96(F)34x (25 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00070A$_H$	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
00070B$_H$	CAN0 - Test Register High (reserved)	TESTRH0		R
00070C$_H$	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
00070D$_H$	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
00070E$_H$-00070F$_H$	Reserved			-
000710$_H$	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711$_H$	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712$_H$	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713$_H$	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714$_H$	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W
000715$_H$	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716$_H$	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717$_H$	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718$_H$	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719$_H$	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
00071A$_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
00071B$_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
00071C$_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
00071D$_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
00071E$_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
00071F$_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720$_H$	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721$_H$	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722$_H$	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723$_H$	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724$_H$	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725$_H$	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726$_H$-00073F$_H$	Reserved			-

I/O map MB96(F)34x (26 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000740H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
00074AH	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
00074BH	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
00074CH	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
00074DH	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W
00074EH	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	R/W
00074FH	CAN0 - IF2 Data A1 High	IF2DTA1H0		R/W
000750H	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	R/W
000751H	CAN0 - IF2 Data A2 High	IF2DTA2H0		R/W
000752H	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	R/W
000753H	CAN0 - IF2 Data B1 High	IF2DTB1H0		R/W
000754H	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	R/W
000755H	CAN0 - IF2 Data B2 High	IF2DTB2H0		R/W
000756H-00077FH	Reserved			-
000780H	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781H	CAN0 - Transmission Request 1 Register High	TREQR1H0		R
000782H	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783H	CAN0 - Transmission Request 2 Register High	TREQR2H0		R
000784H-00078FH	Reserved			-

Interrupt vector table MB96(F)34x (4 of 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
83	$2B0_H$	LINR2	Yes	83	LIN USART 2 RX
84	$2AC_H$	LINT2	Yes	84	LIN USART 2 TX
85	$2A8_H$	LINR3	Yes	85	LIN USART 3 RX
86	$2A4_H$	LINT3	Yes	86	LIN USART 3 TX
87	$2A0_H$	FLASH_A	No	87	Flash memory A (only Flash devices)
88	$29C_H$	FLASH_B	No	88	Flash memory B (only MB96F348T/H/C)
89	298_H	LINR7	Yes	89	LIN USART 7 RX
90	294_H	LINT7	Yes	90	LIN USART 7 TX
91	290_H	LINR8	Yes	91	LIN USART 8 RX
92	$28C_H$	LINT8	Yes	92	LIN USART 8 TX
93	288_H	LINR9	Yes	93	LIN USART 9 RX
94	284_H	LINT9	Yes	94	LIN USART 9 TX
95	280_H	RTC0	No	95	Real Timer Clock
96	$27C_H$	CAL0	No	96	Clock Calibration Unit
97	278_H	DFLASH_A	Yes	97	Data Flash A (only MB96F345Dyy, MB96F345Fyy)

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ *1
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V *2
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V *2
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins *3
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	-	40	mA	Applicable to general purpose I/O pins *3
“L” level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
“L” level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
“L” level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
“L” level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
”H” level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
”H” level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
”H” level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
”H” level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices in QFP package) *4	P_D	-	430*5	mW	T_A=105°C
		-	750*5	mW	T_A=90°C
		-	540*5	mW	T_A=125°C, no Flash program/ erase *6
Permitted Power dissipation (MB96F346/F347/F348 in LQFP package) *4	P_D	-	375*5	mW	T_A=105°C
		-	750*5	mW	T_A=85°C
		-	470*5	mW	T_A=125°C, no Flash program/ erase *6
		-	560*5	mW	T_A=120°C, no Flash program/ erase *6

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

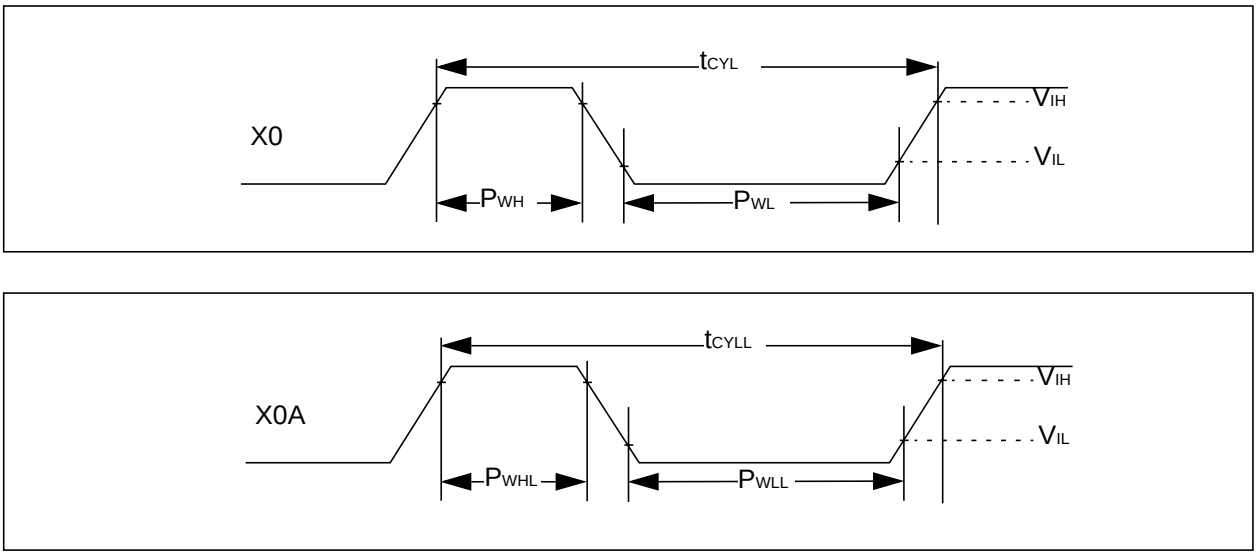
Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped)	+25˚C	1.5	2.5	mA	MB96345/346
			+125˚C	2	4.4		
			+25˚C	2.5	3.5	mA	MB96F345
			+125˚C	3.1	5.7		
			+25˚C	2.9	4	mA	MB96F346/F347/F348
			+125˚C	3.6	7		
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 0 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.35	0.55	mA	MB96345/346
			+125˚C	0.75	2.3		
			+25˚C	0.18	0.3	mA	MB96F345
			+125˚C	0.73	2.3		
			+25˚C	0.4	0.6	mA	MB96F346/F347/F348
			+125˚C	0.95	3.4		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 1 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25˚C	0.08	0.17	mA	MB96345/346
			+125˚C	0.47	1.92		
			+25˚C	0.15	0.25	mA	MB96F345
			+125˚C	0.7	2.25		
			+25˚C	0.15	0.25	mA	MB96F346/F347/F348
			+125˚C	0.7	3.05		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25˚C	0.04	0.12	mA	MB96345/346
			+125˚C	0.43	1.85		
			+25˚C	0.1	0.2	mA	MB96F345
			+125˚C	0.65	2.2		
			+25˚C	0.1	0.2	mA	MB96F346/F347/F348
			+125˚C	0.65	3		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped)	+25˚C	1.4	1.9	mA	MB96345/346
			+125˚C	1.9	3.9		
			+25˚C	1.3	1.8	mA	MB96F345
			+125˚C	1.9	4		
			+25˚C	1.5	2	mA	MB96F346/F347/F348
			+125˚C	2.1	5		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.35	0.5	mA	MB96345/346
			+125˚C	0.7	2.3		
			+25˚C	0.11	0.2	mA	MB96F345
			+125˚C	0.63	2.2		
			+25˚C	0.35	0.5	mA	MB96F346/F347/F348
			+125˚C	0.85	3.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.08	0.15	mA	MB96345/346
			+125˚C	0.47	1.9		
			+25˚C	0.08	0.15	mA	MB96F345
			+125˚C	0.6	2.1		
			+25˚C	0.08	0.15	mA	MB96F346/F347/F348
			+125˚C	0.6	2.9		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes*	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.35	0.5	mA	MB96345/346
			+125˚C	0.7	2.3		
			+25˚C	0.13	0.2	mA	MB96F345
			+125˚C	0.63	2.2		
			+25˚C	0.35	0.5	mA	MB96F346/F347/F348
			+125˚C	0.85	3.3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.07	0.15	mA	MB96345/346
			+125˚C	0.46	1.9		
			+25˚C	0.07	0.15	mA	MB96F345
			+125˚C	0.6	2.1		
			+25˚C	0.07	0.15	mA	MB96F346/F347/F348
			+125˚C	0.6	2.9		
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.3	0.45	mA	MB96345/346
			+125˚C	0.65	2.2		
			+25˚C	0.08	0.15	mA	MB96F345
			+125˚C	0.58	2.1		
			+25˚C	0.3	0.45	mA	MB96F346/F347/F348
			+125˚C	0.8	3.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.03	0.1	mA	MB96345/346
			+125˚C	0.41	1.85		
			+25˚C	0.03	0.1	mA	MB96F345
			+125˚C	0.53	2.05		
			+25˚C	0.03	0.1	mA	MB96F346/F347/F348
			+125˚C	0.53	2.85		


tCYL
X0
VIH
VIL
PWH
PWL

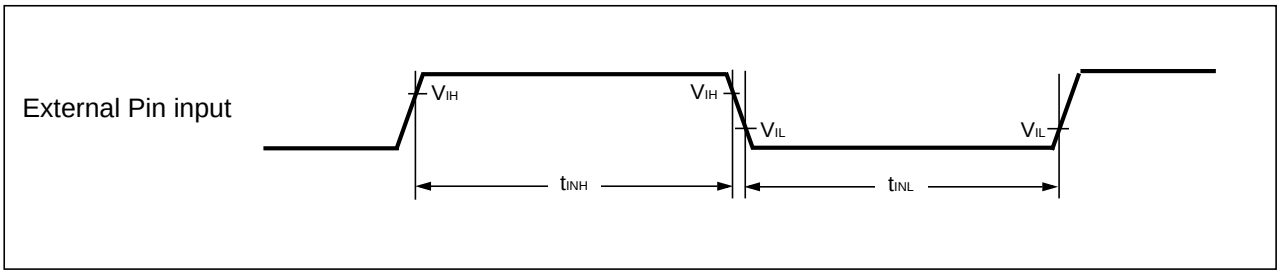
tCYLL
X0A
VIH
VIL
PWHL
PWLL

External Input timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	—	200	—	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2*t_{CLKP1}$ + 200 (t_{CLKP1}=1/ f_{CLKP1})	—	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

Note : Relocated Resource Inputs have same characteristics

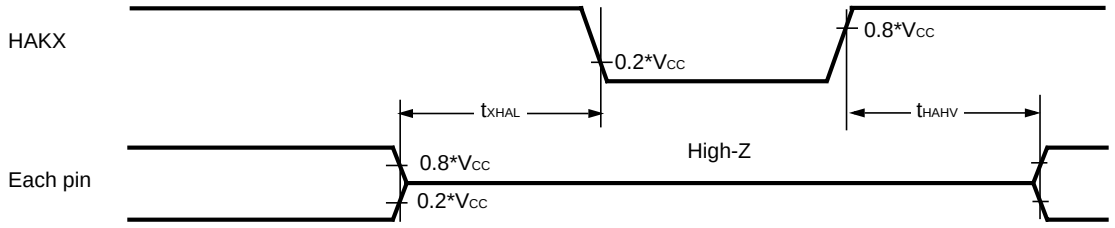


(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	—	$t_{CYC} - 15$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	—	ns	
			EACL:STS=1	– 10	—		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 50$	ns	

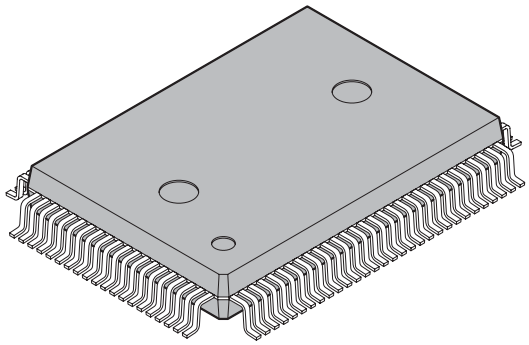
(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

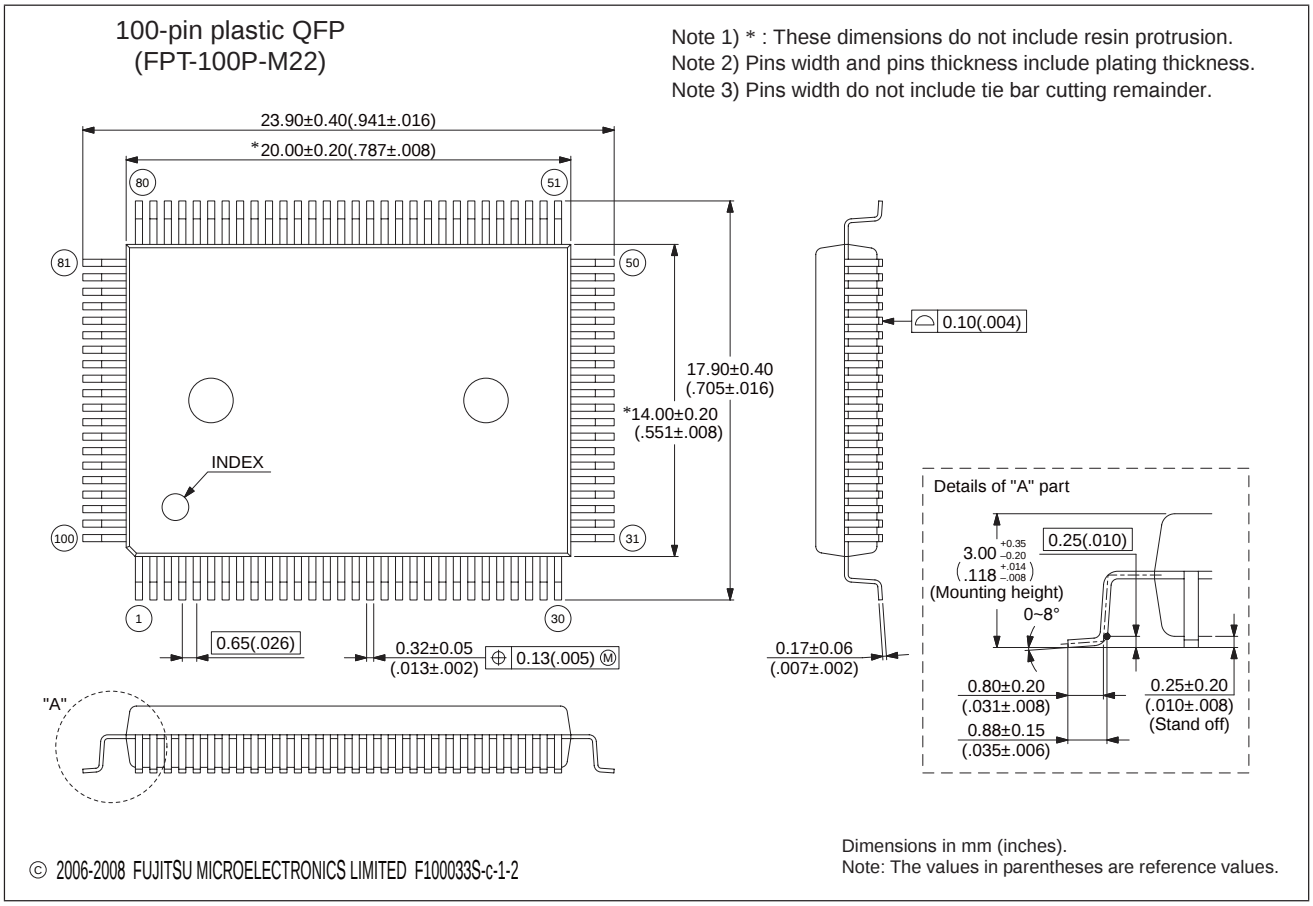
Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	—	ns	
			EACL:STS=1	$t_{CYC} - 8$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	—		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	—		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1	-20	—		



Refer to the Hardware Manual for detailed Timing Charts

■ PACKAGE DIMENSION MB96(F)34x QFP 100P

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M22)		



Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F348YSB PQC-GSE2	Flash A (544KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F348RSB PQC-GSE2			No	
MB96F348YWB PQC-GSE2		Yes	Yes	
MB96F348RWB PQC-GSE2			No	
MB96F348YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348RSB PMC-GSE2			No	
MB96F348YWB PMC-GSE2		Yes	Yes	
MB96F348RWB PMC-GSE2			No	
MB96F348YSC PQC-GSE2*1		No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F348RSC PQC-GSE2*1			No	
MB96F348YWC PQC-GSE2*1		Yes	Yes	
MB96F348RWC PQC-GSE2*1			No	
MB96F348YSC PMC-GSE2*1		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348RSC PMC-GSE2*1			No	
MB96F348YWC PMC-GSE2*1		Yes	Yes	
MB96F348RWC PMC-GSE2*1			No	
MB96F348TSC PQC-GSE2	Flash A (544KB) Flash B (32KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F348HSC PQC-GSE2			No	
MB96F348TWC PQC-GSE2		Yes	Yes	
MB96F348HWC PQC-GSE2			No	
MB96F348TSC PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348HSC PMC-GSE2			No	
MB96F348TWC PMC-GSE2		Yes	Yes	
MB96F348HWC PMC-GSE2			No	
MB96V300BRB-ES (for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)

Revision	Date	Modification
10	2010-06-23	• I/O map: IOABK0-5 added at address 000A00H-000A05H • Ordering Information: Suffix “A” added to all MB96F345 device versions • AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg • Corrected MB96F345 part names in ordering information • Low voltage detector: Detection levels of MB96F345 updated • Example characteristics updated, new figures added showing dependency of PLL Run mode current on frequency • Updated Power Supply current spec in Run/Sleep/Timer/Stop modes (new spec items in PLL Run/Sleep mode, small adjustment of most other values) • Note added that PLL phase jitter spec does not include jitter coming from Main clock • Alarm comparator: Maximum power-up stabilization time increased to 10ms • Removed PHDR register from IO map • Note added in DC characteristics how to select driving strength of ports • I2C AC spec updated: tof, Cb and tSP spec added, wrong footnotes and Condition removed • I/O Circuit type: Note added for type “N” (slew rate control according to I2C spec) • Package dimension: Added the following sentence under the figure: “Please confirm the latest Package dimension by following URL. http://edevice.fujitsu.com/package/en-search/” • AD converter: Impact of input pin capacitance and external capacitance added to formula for calculation of the sampling time • Added specification of RC clock stabilization time • Feature description I2C: ‘8-bit addressing’ corrected to ‘7-bit addressing’ • Feature description PPG: ‘Reload timer overflow as clock input’ corrected to ‘Reload timer underflow as clock input’ • Company name updated on the cover page: Fujitsu Microelectronics Limited -> Fujitsu Semiconductor Limited • ICCLVD specification updated, at 125deg typical value is 7uA and maximum value is 20uA • Ordering information: added devices under development MB96F346A*C, MB96F347A*C, MB96F348A*C, MB96F346Y*C, MB96F347Y*C, MB96F348Y*C, MB96F346R*C, MB96F347R*C, MB96F348R*C