Infineon Technologies - MB96F347RSCPQC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347rscpqc-gse2

■ PIN CIRCUIT TYPE

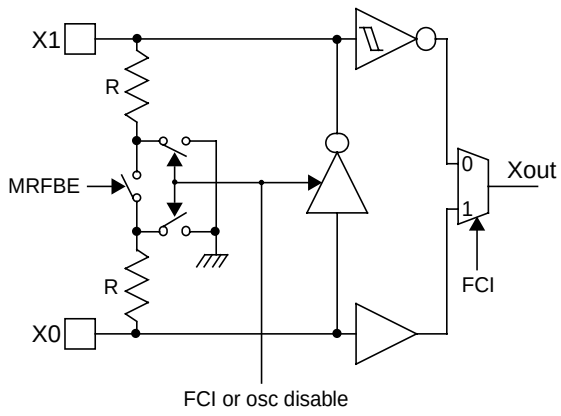
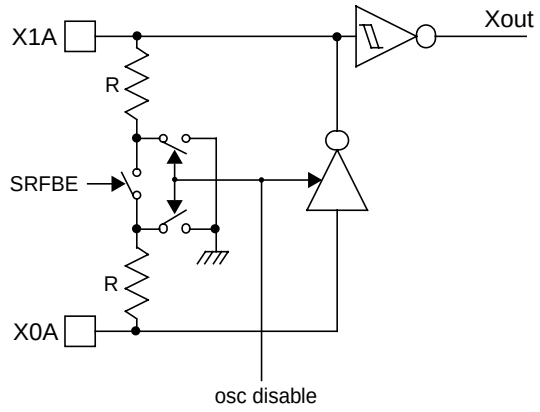
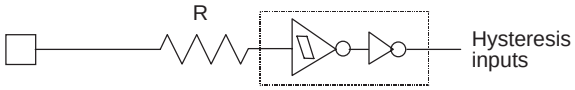
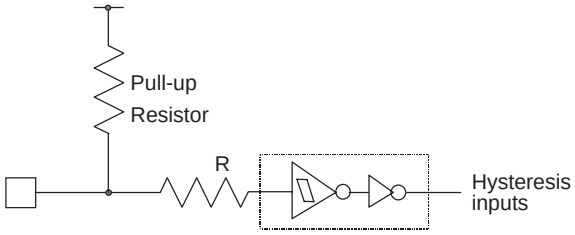
Pin circuit types

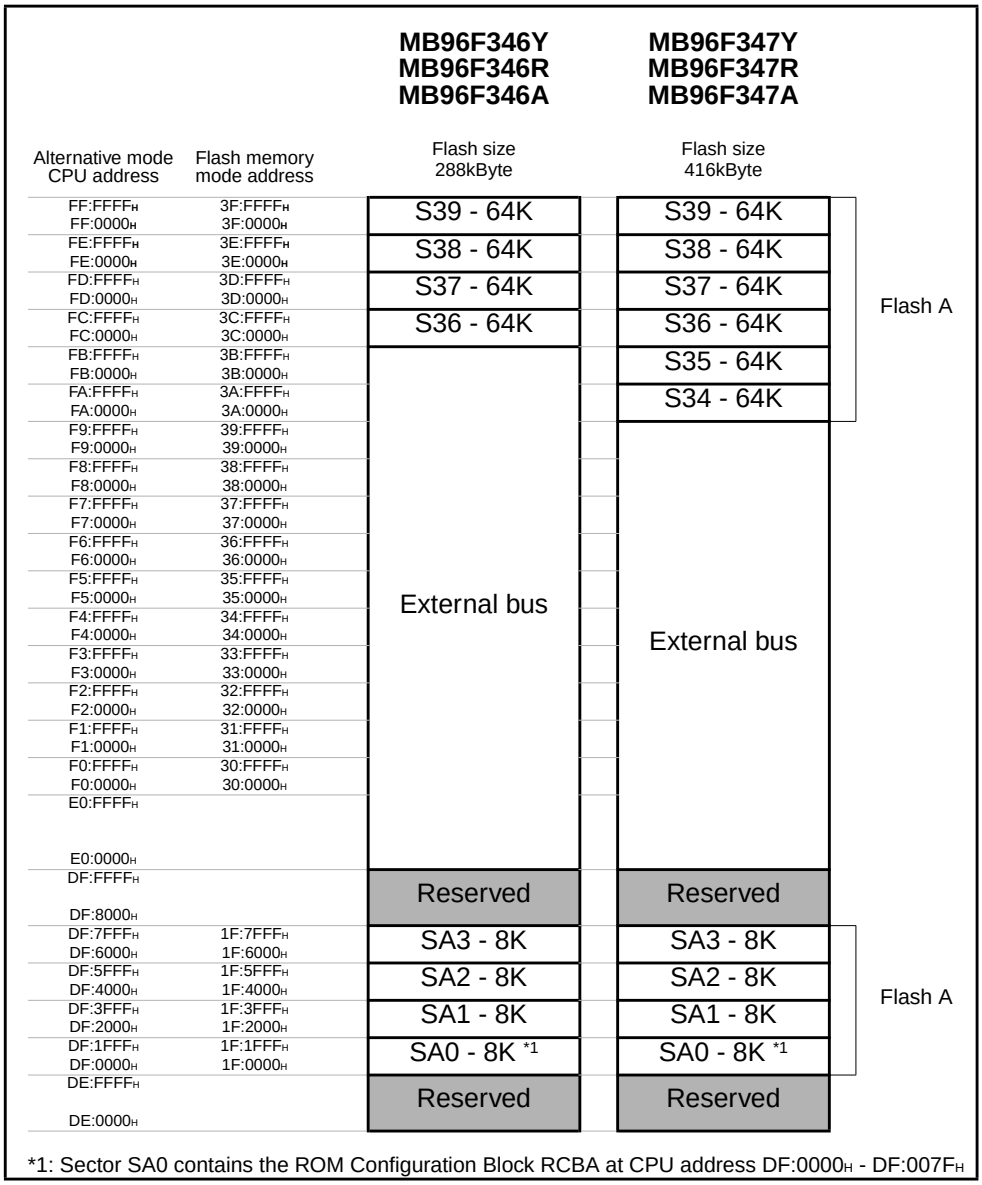
FPT-100P-M20	
Pin no.	Circuit type *1
1-10	H
11,12	B *2
11,12	H *3
13,14	Supply
15	F
16,17	H
18-21	N
22-29	I
30	Supply
31-32	G
33	Supply
34 to 41	I
42	Supply
43 to 48	I
49 to 51	C
52	E
53 to 54	I
55 to 62	H
63, 64	Supply
65 to 87	H
88,89	Supply
90, 91	A
92-100	H

FPT-100P-M22	
Pin no.	Circuit type *1
1-12	H
13, 14	B *2
13, 14	H *3
15,16	Supply
17	F
18,19	H
20-23	N
24-31	I
32	Supply
33-34	G
35	Supply
36 to 43	I
44	Supply
45 to 50	I
51 to 53	C
54	E
55 to 56	I
57 to 64	H
65, 66	Supply
67 to 89	H
90, 91	Supply
92, 93	A
94 to 100	H

*1: Please refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types
*2: Devices with suffix ”W”
*3: Devices without suffix ”W”

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: • Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		• Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		• CMOS Hysteresis input pin • Pull-up resistor value: approx. 50 kΩ



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000H - DF:007FH

I/O map MB96(F)34x (2 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000026H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028H	OCU0 - Output Compare Control Status	OCS0		R/W
000029H	OCU1 - Output Compare Control Status	OCS1		R/W
00002AH	OCU0 - Compare Register		OCCP0	R/W
00002BH	OCU0 - Compare Register			R/W
00002CH	OCU1 - Compare Register		OCCP1	R/W
00002DH	OCU1 - Compare Register			R/W
00002EH	OCU2 - Output Compare Control Status	OCS2		R/W
00002FH	OCU3 - Output Compare Control Status	OCS3		R/W
000030H	OCU2 - Compare Register		OCCP2	R/W
000031H	OCU2 - Compare Register			R/W
000032H	OCU3 - Compare Register		OCCP3	R/W
000033H	OCU3 - Compare Register			R/W
000034H	OCU4 - Output Compare Control Status	OCS4		R/W
000035H	OCU5 - Output Compare Control Status	OCS5		R/W
000036H	OCU4 - Compare Register		OCCP4	R/W
000037H	OCU4 - Compare Register			R/W
000038H	OCU5 - Compare Register		OCCP5	R/W
000039H	OCU5 - Compare Register			R/W
00003AH	OCU6 - Output Compare Control Status	OCS6		R/W
00003BH	OCU7 - Output Compare Control Status	OCS7		R/W
00003CH	OCU6 - Compare Register		OCCP6	R/W
00003DH	OCU6 - Compare Register			R/W
00003EH	OCU7 - Compare Register		OCCP7	R/W
00003FH	OCU7 - Compare Register			R/W
000040H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041H	ICU0/ICU1 - Edge register	ICE01		R/W
000042H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R

I/O map MB96(F)34x (7 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000AB$_H$	PPG5 - Control status register High	PCNH5		R/W
0000AC$_H$	I2C0 - Bus Status Register	IBSR0		R
0000AD$_H$	I2C0 - Bus Control Register	IBCR0		R/W
0000AE$_H$	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
0000AF$_H$	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
0000B0$_H$	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
0000B1$_H$	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
0000B2$_H$	I2C0 - Seven bit Slave address Register	ISBA0		R/W
0000B3$_H$	I2C0 - Seven bit Address mask Register	ISMK0		R/W
0000B4$_H$	I2C0 - Data Register	IDAR0		R/W
0000B5$_H$	I2C0 - Clock Control Register	ICCR0		R/W
0000B6$_H$	I2C1 - Bus Status Register	IBSR1		R
0000B7$_H$	I2C1 - Bus Control Register	IBCR1		R/W
0000B8$_H$	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
0000B9$_H$	I2C1 - Ten bit Slave address Register High	ITBAH1		R/W
0000BA$_H$	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
0000BB$_H$	I2C1 - Ten bit Address mask Register High	ITMKH1		R/W
0000BC$_H$	I2C1 - Seven bit Slave address Register	ISBA1		R/W
0000BD$_H$	I2C1 - Seven bit Address mask Register	ISMK1		R/W
0000BE$_H$	I2C1 - Data Register	IDAR1		R/W
0000BF$_H$	I2C1 - Clock Control Register	ICCR1		R/W
0000C0$_H$	USART0 - Serial Mode Register	SMR0		R/W
0000C1$_H$	USART0 - Serial Control Register	SCR0		R/W
0000C2$_H$	USART0 - TX Register	TDR0		W
0000C2$_H$	USART0 - RX Register	RDR0		R
0000C3$_H$	USART0 - Serial Status	SSR0		R/W
0000C4$_H$	USART0 - Control/Com. Register	ECCR0		R/W
0000C5$_H$	USART0 - Ext. Status Register	ESCR0		R/W
0000C6$_H$	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W
0000C7$_H$	USART0 - Baud Rate Generator Register High	BGRH0		R/W

I/O map MB96(F)34x (8 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000C8H	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
0000C9H	Reserved			-
0000CAH	USART1 - Serial Mode Register	SMR1		R/W
0000CBH	USART1 - Serial Control Register	SCR1		R/W
0000CCH	USART1 - TX Register	TDR1		W
0000CCH	USART1 - RX Register	RDR1		R
0000CDH	USART1 - Serial Status	SSR1		R/W
0000CEH	USART1 - Control/Com. Register	ECCR1		R/W
0000CFH	USART1 - Ext. Status Register	ESCR1		R/W
0000D0H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
0000D1H	USART1 - Baud Rate Generator Register High	BGRH1		R/W
0000D2H	USART1 - Extended Serial Interrupt Register	ESIR1		R/W
0000D3H	Reserved			-
0000D4H	USART2 - Serial Mode Register	SMR2		R/W
0000D5H	USART2 - Serial Control Register	SCR2		R/W
0000D6H	USART2 - TX Register	TDR2		W
0000D6H	USART2 - RX Register	RDR2		R
0000D7H	USART2 - Serial Status	SSR2		R/W
0000D8H	USART2 - Control/Com. Register	ECCR2		R/W
0000D9H	USART2 - Ext. Status Register	ESCR2		R/W
0000DAH	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DBH	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DCH	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DDH	Reserved			-
0000DEH	USART3 - Serial Mode Register	SMR3		R/W
0000DFH	USART3 - Serial Control Register	SCR3		R/W
0000E0H	USART3 - TX Register	TDR3		W
0000E0H	USART3 - RX Register	RDR3		R
0000E1H	USART3 - Serial Status	SSR3		R/W
0000E2H	USART3 - Control/Com. Register	ECCR3		R/W

I/O map MB96(F)34x (29 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000840H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841H	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
00084AH	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
00084BH	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
00084CH	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
00084DH	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
00084EH	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
00084FH	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851H	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853H	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855H	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856H-00087FH	Reserved			-
000880H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R
000884H-00088FH	Reserved			-

■ INTERRUPT VECTOR TABLE

Interrupt vector table MB96(F)34x (1 of 4)

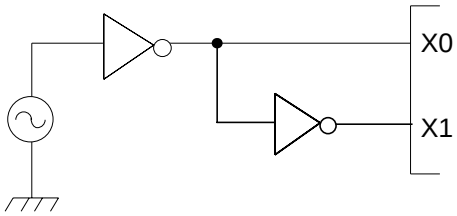
Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	
1	$3F8_H$	CALLV1	No	-	
2	$3F4_H$	CALLV2	No	-	
3	$3F0_H$	CALLV3	No	-	
4	$3EC_H$	CALLV4	No	-	
5	$3E8_H$	CALLV5	No	-	
6	$3E4_H$	CALLV6	No	-	
7	$3E0_H$	CALLV7	No	-	
8	$3DC_H$	RESET	No	-	
9	$3D8_H$	INT9	No	-	
10	$3D4_H$	EXCEPTION	No	-	
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	RESERVED	No	16	Reserved
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	EXTINT5	Yes	22	External Interrupt 5
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10

Interrupt vector table MB96(F)34x (4 of 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
83	$2B0_H$	LINR2	Yes	83	LIN USART 2 RX
84	$2AC_H$	LINT2	Yes	84	LIN USART 2 TX
85	$2A8_H$	LINR3	Yes	85	LIN USART 3 RX
86	$2A4_H$	LINT3	Yes	86	LIN USART 3 TX
87	$2A0_H$	FLASH_A	No	87	Flash memory A (only Flash devices)
88	$29C_H$	FLASH_B	No	88	Flash memory B (only MB96F348T/H/C)
89	298_H	LINR7	Yes	89	LIN USART 7 RX
90	294_H	LINT7	Yes	90	LIN USART 7 TX
91	290_H	LINR8	Yes	91	LIN USART 8 RX
92	$28C_H$	LINT8	Yes	92	LIN USART 8 TX
93	288_H	LINR9	Yes	93	LIN USART 9 RX
94	284_H	LINT9	Yes	94	LIN USART 9 TX
95	280_H	RTC0	No	95	Real Timer Clock
96	$27C_H$	CAL0	No	96	Clock Calibration Unit
97	278_H	DFLASH_A	Yes	97	Data Flash A (only MB96F345Dyy, MB96F345Fyy)

2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



4. Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

5. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

7. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

8. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

10. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output H voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -2mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -1.6mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA (PODR:OD=1)
	V_{OH5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -5mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA (PODR:OD=0)
	V_{OH3}	3mA out-puts	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -3mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	I/O circuit type “N”
Output L voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +2mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +1.6mA	-	-	0.4	V	Driving strength set to 2mA (PODR:OD=1)
	V_{OL5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +5mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +3mA	-	-	0.4	V	Driving strength set to 5mA (PODR:OD=0)
	V_{OL3}	3mA out-puts	3.0V ≤ V_{CC} ≤ 5.5V I_{OL} = +3mA	-	-	0.4	V	I/O circuit type “N”
Input leak current	I_{IL}	Pnn_m	V_{SS} < V_I < V_{CC} AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	-1	-	+1	µA	Single port pin
Pull-up resistance	R_{UP}	Pnn_m, $\overline{RSTX}$	V_{CC} = 3.3V ± 10%	40	100	160	kΩ	
			V_{CC} = 5.0V ± 10%	25	50	100	kΩ	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 16MHz, CLKP2 = 8MHz 1 Flash/ROM wait state (CLKRC and CLKSC stopped)	+25˚C	8	11	mA	MB96345/346
			+125˚C	8.5	13		
			+25˚C	15	20	mA	MB96F345
			+125˚C	16	23		
			+25˚C	17	22	mA	MB96F346/F347/F348Y/R/Ayy
			+125˚C	18.5	25.5		
			+25˚C	16	21	mA	MB96F348T/H/CyB/C
			+125˚C	17.5	24.5		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 32MHz, CLKP2 = 16MHz 2 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25˚C	14	18	mA	MB96345/346
			+125˚C	14.5	20		
			+25˚C	23.5	29.5	mA	MB96F345
			+125˚C	25	32.5		
			+25˚C	26	32	mA	MB96F346/F347/F348Y/R/Ayy
			+125˚C	28	36		
			+25˚C	25	31	mA	MB96F348T/H/CyB/C
			+125˚C	27	35		
		PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz 0 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25˚C	13	17	mA	MB96345/346
			+125˚C	13.5	19		
			+25˚C	27	39	mA	MB96F345
			+125˚C	29	42		
			+25˚C	31	43	mA	MB96F346/F347/F348Y/R/Ayy
			+125˚C	33	47		
			+25˚C	30	42	mA	MB96F348T/H/CyB/C
			+125˚C	32	46		

Internal Clock timing

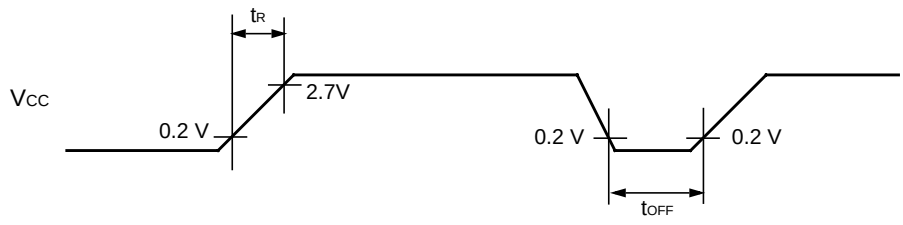
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	86	0	96	MHz	MB96F348T/H/CxB/C
		0	72	0	80	MHz	MB96F345
		0	68	0	74	MHz	MB96F34xY/R/Axx
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	Others than below
		0	36	0	40	MHz	MB96F345
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	Others than below
		0	26	0	28	MHz	MB96F34xY/R/Axx

Power On Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

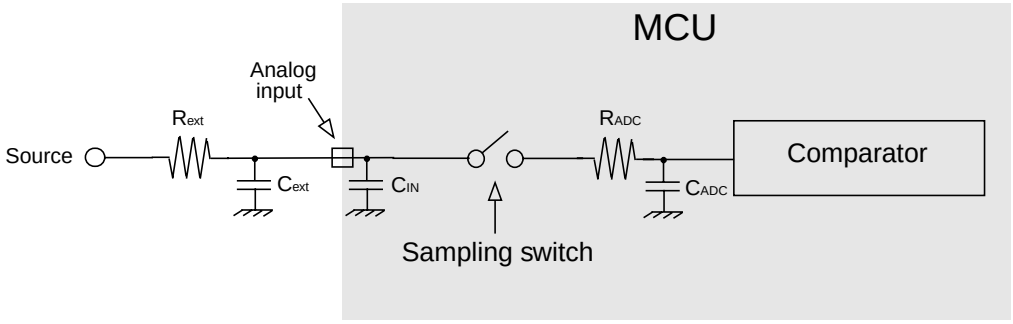
(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 – 20$	—	ns	
			EACL:ACE=1	$5t_{CYC}/2 – 20$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} – 20$	—	ns	
			EACL:ACE=1	$2t_{CYC} – 20$	—		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	—	$3t_{CYC} – 60$	ns	w/o cycle extension
			EACL:ACE=1	—	$4t_{CYC} – 60$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	—	$5t_{CYC}/2 – 60$	ns	w/o cycle extension
			EACL:ACE=1	—	$7t_{CYC}/2 – 60$		
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2 – 8$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2 – 55$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 – 15$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 – 15$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	—	$t_{CYC} – 20$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 – 20$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 – 15$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 – 15$	—	ns	
			EACL:STS=1	– 15	—		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} – 55$	ns	

Accuracy and setting of the A/D Converter sampling time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{cc} voltage level. The following replacement model can be used for the calculation:



R_{ext}: external driving impedance
C_{ext}: capacitance of PCB at A/D converter input
C_{IN}: capacitance of MCU input pin: 15pF (max)
R_{ADC}: resistance within MCU: 2.6kΩ (max) for $4.5V \le AV_{cc} \le 5.5V$
12kΩ (max) for $3.0V \le AV_{cc} < 4.5V$
C_{ADC}: sampling capacitance within MCU: 10pF (max)

The sampling time should be set to minimum “7τ“. The following approximation formula for the replacement model above can be used:

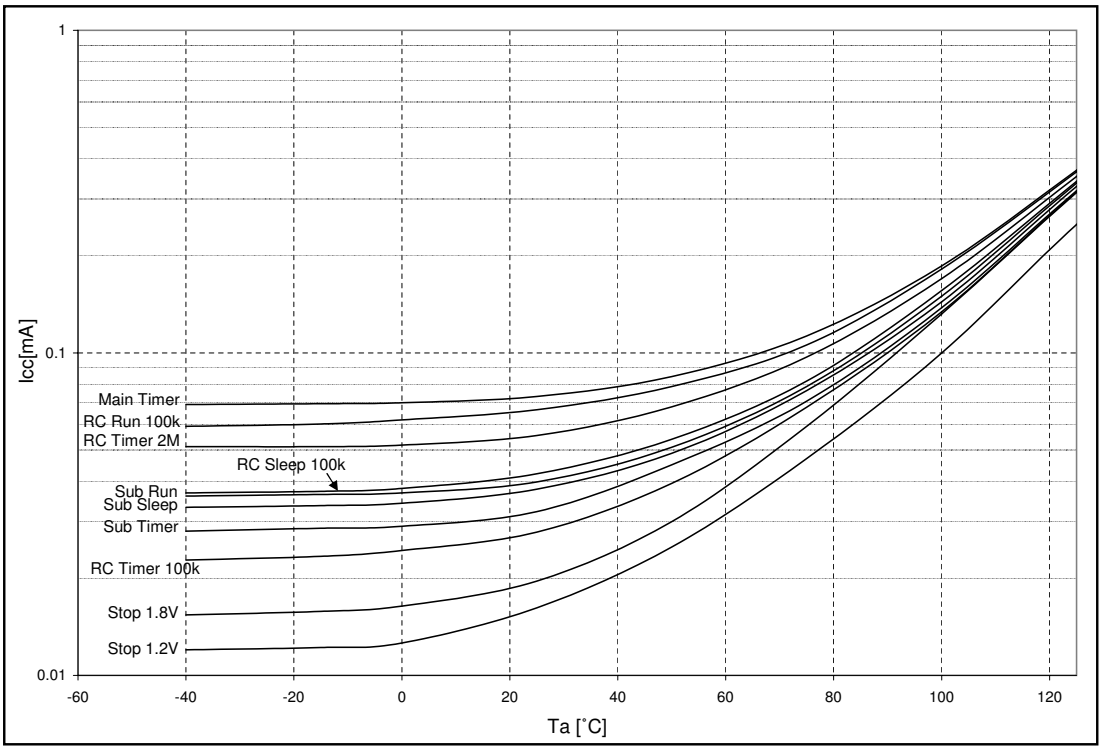
$$T_{samp}\ [min] = 7 \times (R_{ext} \times (C_{ext} + C_{IN}) + (R_{ext} + R_{ADC}) \times C_{ADC})$$

- Do not select a sampling time below the absolute minimum permitted value (0.5µs for $4.5V \le AV_{cc} \le 5.5V$; 1.2 µs for $3.0V \le AV_{cc} < 4.5V$).
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin. In this case the internal sampling capacitance C_{ADC} will be charged out of this external capacitance.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.

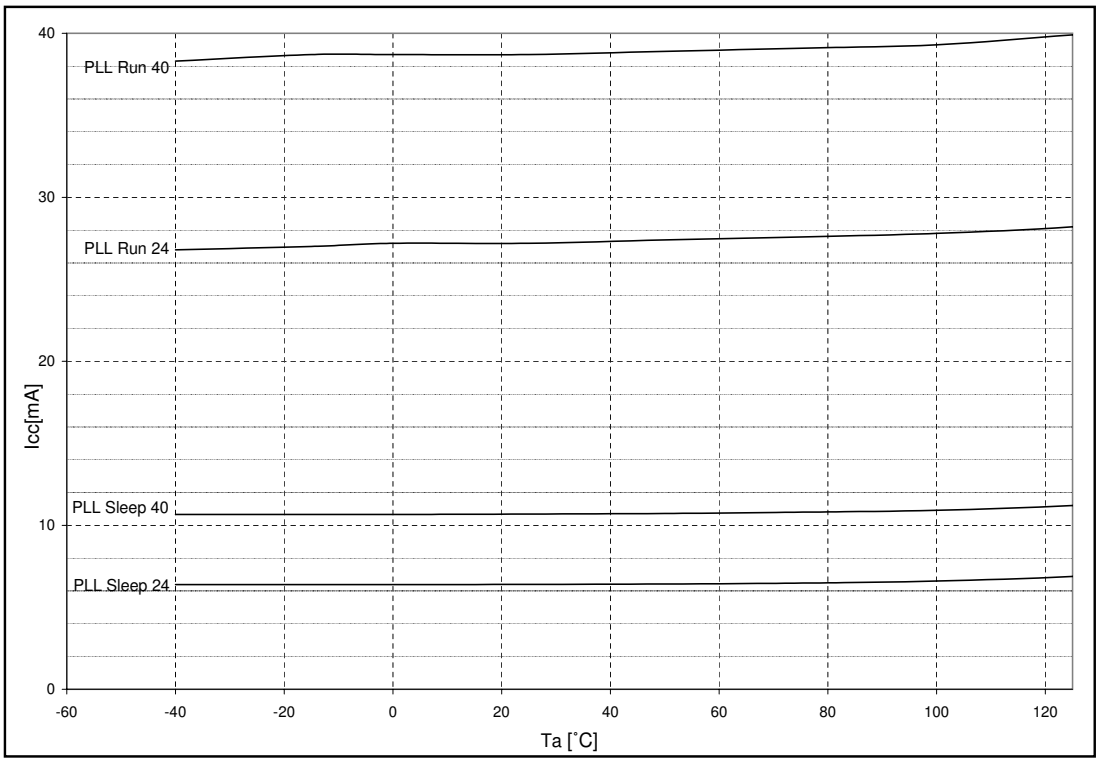
Mode name	Details
PLL Sleep 48	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 96MHz$ • $f_{CLKP1} = 48MHz$ • $f_{CLKP2} = 24MHz$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 40	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 80MHz$ • $f_{CLKP1} = 40MHz$ • $f_{CLKP2} = 20MHz$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 36	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 72MHz$ • $f_{CLKP1} = 36MHz$ • $f_{CLKP2} = 18MHz$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 24	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 48MHz$ • $f_{CLKP1} = f_{CLKP2} = 24MHz$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Sleep	Main Sleep mode current $I_{CCSMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 4MHz$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, RC oscillator and Sub oscillator stopped
RC Sleep 2M	RC Sleep mode current I_{CCSRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 2MHz$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, Main oscillator and Sub oscillator stopped
RC Sleep 100k	RC Sleep mode current I_{CCSRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 100kHz$ • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped

Mode name	Details
Sub Sleep	Sub Sleep mode current I_{CCSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped
PLL Timer 48	PLL Timer mode current I_{CCTPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 48MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Timer	Main Timer mode current $I_{CCTMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 4MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Sub oscillator stopped
RC Timer 2M	RC Timer mode current I_{CCTRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2}$ = 2MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
RC Timer 100k	RC Timer mode current I_{CCTRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Timer	Sub Timer mode current I_{CCTSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped
Stop 1.8V	Stop mode current I_{CCH} with the following settings: • Regulator in Low Power Mode B (by hardware) • Core voltage at 1.8V (VRCR:LPMB[2:0] = 110_B)
Stop 1.2V	Stop mode current I_{CCH} with the following settings: • Regulator in Low Power Mode B (by hardware) • Core voltage at 1.2V (VRCR:LPMB[2:0] = 000_B)

MB96345/346 Low power mode currents



MB96F345 PLL Run and Sleep mode currents



2. Frequency dependency of power supply currents in PLL Run mode

The following diagrams show the current consumption of samples with typical wafer process parameters in PLL Run mode at different frequencies and Flash timing settings.

Measurement conditions:

- V_{CC} = AV_{CC} = 5.0V
- Ta = 25˚C
- f_{CLKS1} = f_{CLKB} or f_{CLKS1} = 2*f_{CLKB} as described in diagram
- f_{CLKS2} = f_{CLKS1}
- f_{CLKP1} = f_{CLKB}
- f_{CLKP2} = f_{CLKB}/2
- Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) or 1.9V (VRCR:HPM[1:0] = 11_B) as described in diagram
- Main clock = 4MHz external clock
- Flash memory timing settings:
  - MTCRA=2128_H/2208_H (0 Flash wait states, f_{CLKS1} = 2*f_{CLKB})
  - MTCRA=0239_H/2129_H (1 Flash wait state, f_{CLKS1} = f_{CLKB})
  - MTCRA=$4C09_H$/$6B09_H$ (1 Flash wait state, f_{CLKS1} = 2*f_{CLKB})
  - MTCRA=$233A_H$ (2 Flash wait states, f_{CLKS1} = f_{CLKB})
- Average Flash access rate (number of read accesses to the Flash per CLKB clock cycle, no buffer hit):
  - 0 Flash wait states: 0.5
  - 1 Flash wait states: 0.33
  - 2 Flash wait states: 0.25

MB96F345 PLL Run mode currents