Infineon Technologies - MB96F347RWCPMC-GSE2 Datasheet

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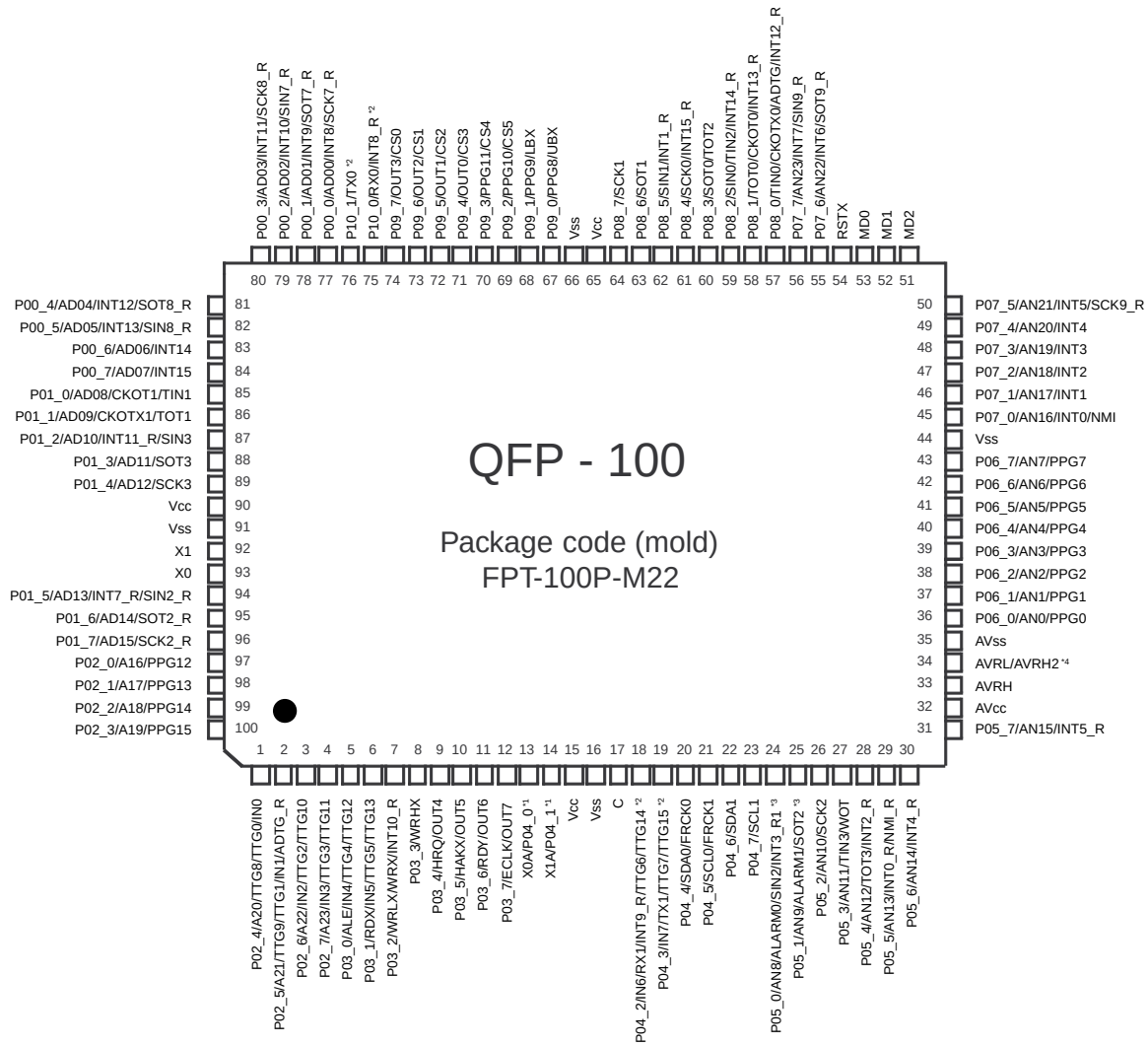
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347rwcpmc-gse2

■ PIN ASSIGNMENTS

Pin assignment of MB96(F)34x (FPT-100P-M22)



*1: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

*2: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

*3: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

*4: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

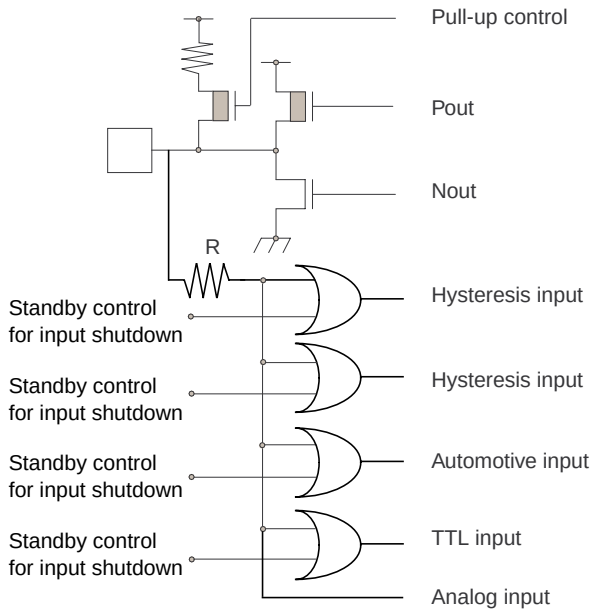
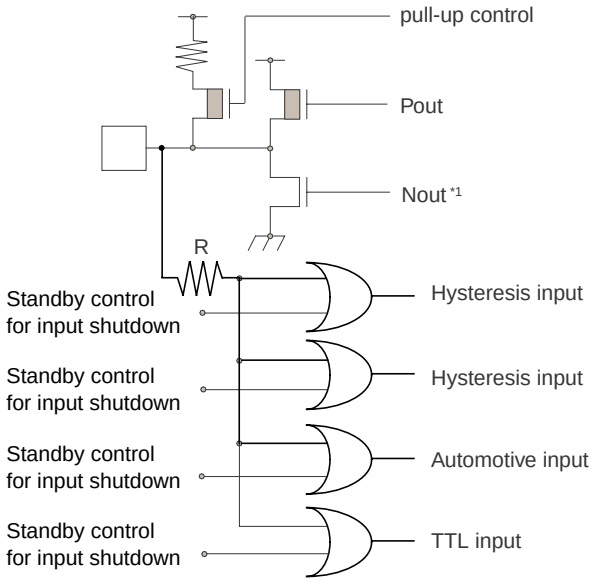
(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F²MC-16LX family MB90340 series.

Pin Function description (2 of 2)

Pin name	Feature	Description
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I2C interface n clock I/O input/output
SDAn	I2C	I2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

Type	Circuit	Remarks
I		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function * • Automotive input with input shutdown function • TTL input with input shutdown function * • Programmable pull-up resistor: 50kΩ approx. • Analog input Note: MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • 2 different CMOS hysteresis inputs with input shutdown function * • Automotive input with input shutdown function • TTL input with input shutdown function * • Programmable pull-up resistor: 50kΩ approx. *1: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage Note: MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

■ USER ROM MEMORY MAP FOR FLASH DEVICES

MB96F345D
MB96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	External bus	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$		
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$		
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$		
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$		
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$		
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$		
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$		
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$		
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$		
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$		
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$		
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$		
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$		
E0:FFFF$_H$ E0:0000$_H$			
DF:FFFF$_H$ DF:8000$_H$		Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K *1	
DE:FFFF$_H$ DE:0000$_H$		Reserved	
0E:FFFF$_H$ 0E:FF00$_H$	(0E:FFFF$_H$) (0E:FF00$_H$)	SDA0-256 *2	Data Flash A
0E:FEFF$_H$ 0E:0000$_H$		Reserved	
0D:FFFF$_H$ 0D:C000$_H$	(0F:FFFF$_H$) (0F:C000$_H$)	SDA4-16K	Data Flash A
0D:BFFF$_H$ 0D:8000$_H$	(0F:BFFF$_H$) (0F:8000$_H$)	SDA3-16K	
0D:7FFF$_H$ 0D:4000$_H$	(0F:7FFF$_H$) (0F:4000$_H$)	SDA2-16K	
0D:3FFF$_H$ 0D:0000$_H$	(0F:3FFF$_H$) (0F:0000$_H$)	SDA1-16K	
0C:FFFF$_H$ 0C:0000$_H$		Reserved	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

*2: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address DE:FF00$_H$ - DE:FF2F$_H$

■ I/O MAP

I/O map MB96(F)34x (1 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000H	I/O Port P00 - Port Data Register	PDR00		R/W
000001H	I/O Port P01 - Port Data Register	PDR01		R/W
000002H	I/O Port P02 - Port Data Register	PDR02		R/W
000003H	I/O Port P03 - Port Data Register	PDR03		R/W
000004H	I/O Port P04 - Port Data Register	PDR04		R/W
000005H	I/O Port P05 - Port Data Register	PDR05		R/W
000006H	I/O Port P06 - Port Data Register	PDR06		R/W
000007H	I/O Port P07 - Port Data Register	PDR07		R/W
000008H	I/O Port P08 - Port Data Register	PDR08		R/W
000009H	I/O Port P09 - Port Data Register	PDR09		R/W
00000AH	I/O Port P10 - Port Data Register	PDR10		R/W
00000BH-000017H	Reserved			-
000018H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019H	ADC0 - Control Status register High	ADCSH		R/W
00001AH	ADC0 - Data Register Low	ADCRL	ADCR	R
00001BH	ADC0 - Data Register High	ADCRH		R
00001CH	ADC0 - Setting Register		ADSR	R/W
00001DH	ADC0 - Setting Register			R/W
00001EH	ADC0 - Extended Configuration Register	ADECR		R/W
00001FH	Reserved			-
000020H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021H	FRT0 - Data register of free-running timer			R/W
000022H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025H	FRT1 - Data register of free-running timer			R/W

I/O map MB96(F)34x (5 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000072H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075H	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077H	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078H	PPG0 - Timer register		PTMR0	R
000079H	PPG0 - Timer register			R
00007AH	PPG0 - Period setting register		PCSR0	W
00007BH	PPG0 - Period setting register			W
00007CH	PPG0 - Duty cycle register		PDUT0	W
00007DH	PPG0 - Duty cycle register			W
00007EH	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007FH	PPG0 - Control status register High	PCNH0		R/W
000080H	PPG1 - Timer register		PTMR1	R
000081H	PPG1 - Timer register			R
000082H	PPG1 - Period setting register		PCSR1	W
000083H	PPG1 - Period setting register			W
000084H	PPG1 - Duty cycle register		PDUT1	W
000085H	PPG1 - Duty cycle register			W
000086H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087H	PPG1 - Control status register High	PCNH1		R/W
000088H	PPG2 - Timer register		PTMR2	R
000089H	PPG2 - Timer register			R
00008AH	PPG2 - Period setting register		PCSR2	W
00008BH	PPG2 - Period setting register			W
00008CH	PPG2 - Duty cycle register		PDUT2	W

I/O map MB96(F)34x (8 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000C8H	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
0000C9H	Reserved			-
0000CAH	USART1 - Serial Mode Register	SMR1		R/W
0000CBH	USART1 - Serial Control Register	SCR1		R/W
0000CCH	USART1 - TX Register	TDR1		W
0000CCH	USART1 - RX Register	RDR1		R
0000CDH	USART1 - Serial Status	SSR1		R/W
0000CEH	USART1 - Control/Com. Register	ECCR1		R/W
0000CFH	USART1 - Ext. Status Register	ESCR1		R/W
0000D0H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
0000D1H	USART1 - Baud Rate Generator Register High	BGRH1		R/W
0000D2H	USART1 - Extended Serial Interrupt Register	ESIR1		R/W
0000D3H	Reserved			-
0000D4H	USART2 - Serial Mode Register	SMR2		R/W
0000D5H	USART2 - Serial Control Register	SCR2		R/W
0000D6H	USART2 - TX Register	TDR2		W
0000D6H	USART2 - RX Register	RDR2		R
0000D7H	USART2 - Serial Status	SSR2		R/W
0000D8H	USART2 - Control/Com. Register	ECCR2		R/W
0000D9H	USART2 - Ext. Status Register	ESCR2		R/W
0000DAH	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DBH	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DCH	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DDH	Reserved			-
0000DEH	USART3 - Serial Mode Register	SMR3		R/W
0000DFH	USART3 - Serial Control Register	SCR3		R/W
0000E0H	USART3 - TX Register	TDR3		W
0000E0H	USART3 - RX Register	RDR3		R
0000E1H	USART3 - Serial Status	SSR3		R/W
0000E2H	USART3 - Control/Com. Register	ECCR3		R/W

I/O map MB96(F)34x (10 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000117H	DMA2 - Data counter high byte	DCTH2		R/W
000118H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011AH	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011BH	DMA3 - DMA control register	DMACS3		R/W
00011CH	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011DH	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011EH	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011FH	DMA3 - Data counter high byte	DCTH3		R/W
000120H	DMA4 - Buffer address pointer low byte	BAPL4		R/W
000121H	DMA4 - Buffer address pointer middle byte	BAPM4		R/W
000122H	DMA4 - Buffer address pointer high byte	BAPH4		R/W
000123H	DMA4 - DMA control register	DMACS4		R/W
000124H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125H	DMA4 - I/O register address pointer high byte	IOAH4		R/W
000126H	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127H	DMA4 - Data counter high byte	DCTH4		R/W
000128H	DMA5 - Buffer address pointer low byte	BAPL5		R/W
000129H	DMA5 - Buffer address pointer middle byte	BAPM5		R/W
00012AH	DMA5 - Buffer address pointer high byte	BAPH5		R/W
00012BH	DMA5 - DMA control register	DMACS5		R/W
00012CH	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
00012DH	DMA5 - I/O register address pointer high byte	IOAH5		R/W
00012EH	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
00012FH	DMA5 - Data counter high byte	DCTH5		R/W
000130H-00017FH	Reserved			-
000180H-00037FH	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380H	DMA0 - Interrupt select	DISEL0		R/W
000381H	DMA1 - Interrupt select	DISEL1		R/W

I/O map MB96(F)34x (11 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000382H	DMA2 - Interrupt select	DISEL2		R/W
000383H	DMA3 - Interrupt select	DISEL3		R/W
000384H	DMA4 - Interrupt select	DISEL4		R/W
000385H	DMA5 - Interrupt select	DISEL5		R/W
000386H-00038FH	Reserved			-
000390H	DMA - Status register low byte	DSRL	DSR	R/W
000391H	DMA - Status register high byte	DSRH		R/W
000392H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393H	DMA - Stop status register high byte	DSSRH		R/W
000394H	DMA - Enable register low byte	DERL	DER	R/W
000395H	DMA - Enable register high byte	DERH		R/W
000396H-00039FH	Reserved			-
0003A0H	Interrupt level register	ILR	ICR	R/W
0003A1H	Interrupt index register	IDX		R/W
0003A2H	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3H	Interrupt vector table base register High	TBRH		R/W
0003A4H	Delayed Interrupt register	DIRR		R/W
0003A5H	Non Maskable Interrupt register	NMI		R/W
0003A6H-0003ABH	Reserved			-
0003ACH	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003ADH	EDSU communication interrupt selection High	EDSU2H		R/W
0003AEH	ROM mirror control register	ROMM		R/W
0003AFH	EDSU configuration register	EDSU		R/W
0003B0H	Memory patch control/status register ch 0/1		PFCS0	R/W
0003B1H	Memory patch control/status register ch 0/1			R/W
0003B2H	Memory patch control/status register ch 2/3		PFCS1	R/W
0003B3H	Memory patch control/status register ch 2/3			R/W
0003B4H	Memory patch control/status register ch 4/5		PFCS2	R/W

I/O map MB96(F)34x (17 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000483H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485H	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487H	I/O Port P07 - Port Output Drive Register	PODR07		R/W
000488H	I/O Port P08 - Port Output Drive Register	PODR08		R/W
000489H	I/O Port P09 - Port Output Drive Register	PODR09		R/W
00048AH	I/O Port P10 - Port Output Drive Register	PODR10		R/W
00048BH-0004A7H	Reserved			-
0004A8H	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
0004A9H	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
0004AAH	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
0004ABH	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
0004ACH	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
0004ADH	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
0004AEH	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
0004AFH	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
0004B0H	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		R/W
0004B1H	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		R/W
0004B2H	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		R/W
0004B3H-0004BBH	Reserved			-
0004BCH	I/O Port P00 - External Pin State Register	EPSR00		R
0004BDH	I/O Port P01 - External Pin State Register	EPSR01		R
0004BEH	I/O Port P02 - External Pin State Register	EPSR02		R
0004BFH	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0H	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1H	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2H	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3H	I/O Port P07 - External Pin State Register	EPSR07		R

I/O map MB96(F)34x (22 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00058B$_H$	PPG10 - Period setting register			W
00058C$_H$	PPG10 - Duty cycle register		PDUT10	W
00058D$_H$	PPG10 - Duty cycle register			W
00058E$_H$	PPG10 - Control status register Low	PCNL10	PCN10	R/W
00058F$_H$	PPG10 - Control status register High	PCNH10		R/W
000590$_H$	PPG11 - Timer register		PTMR11	R
000591$_H$	PPG11 - Timer register			R
000592$_H$	PPG11 - Period setting register		PCSR11	W
000593$_H$	PPG11 - Period setting register			W
000594$_H$	PPG11 - Duty cycle register		PDUT11	W
000595$_H$	PPG11 - Duty cycle register			W
000596$_H$	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597$_H$	PPG11 - Control status register High	PCNH11		R/W
000598$_H$	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599$_H$	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A$_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B$_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C$_H$	PPG12 - Timer register		PTMR12	R
00059D$_H$	PPG12 - Timer register			R
00059E$_H$	PPG12 - Period setting register		PCSR12	W
00059F$_H$	PPG12 - Period setting register			W
0005A0$_H$	PPG12 - Duty cycle register		PDUT12	W
0005A1$_H$	PPG12 - Duty cycle register			W
0005A2$_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3$_H$	PPG12 - Control status register High	PCNH12		R/W
0005A4$_H$	PPG13 - Timer register		PTMR13	R
0005A5$_H$	PPG13 - Timer register			R
0005A6$_H$	PPG13 - Period setting register		PCSR13	W
0005A7$_H$	PPG13 - Period setting register			W
0005A8$_H$	PPG13 - Duty cycle register		PDUT13	W

3. DC characteristics

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in MB96F345
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	Not available in MB96F345
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in MB96F34xY/R/AxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in MB96F345
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	Not available in MB96F345
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in MB96F34xY/R/AxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped)	+25˚C	1.4	1.9	mA	MB96345/346
			+125˚C	1.9	3.9		
			+25˚C	1.3	1.8	mA	MB96F345
			+125˚C	1.9	4		
			+25˚C	1.5	2	mA	MB96F346/F347/F348
			+125˚C	2.1	5		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.35	0.5	mA	MB96345/346
			+125˚C	0.7	2.3		
			+25˚C	0.11	0.2	mA	MB96F345
			+125˚C	0.63	2.2		
			+25˚C	0.35	0.5	mA	MB96F346/F347/F348
			+125˚C	0.85	3.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.08	0.15	mA	MB96345/346
			+125˚C	0.47	1.9		
			+25˚C	0.08	0.15	mA	MB96F345
			+125˚C	0.6	2.1		
			+25˚C	0.08	0.15	mA	MB96F346/F347/F348
			+125˚C	0.6	2.9		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	—	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	—	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

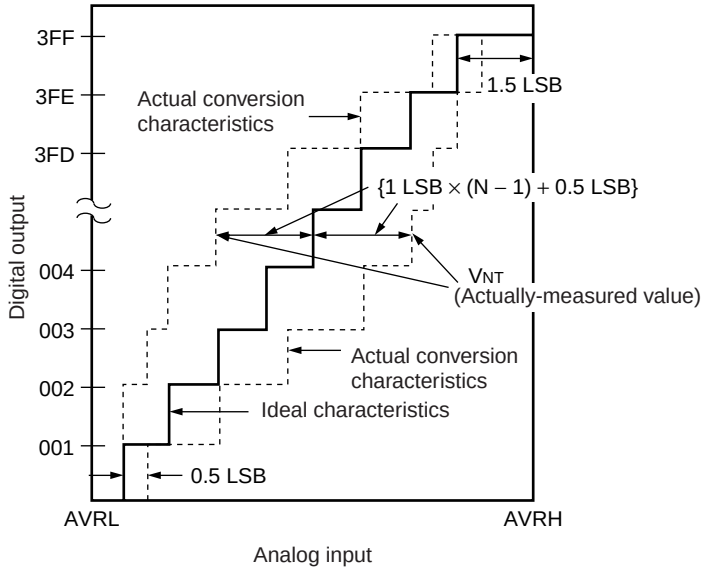
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

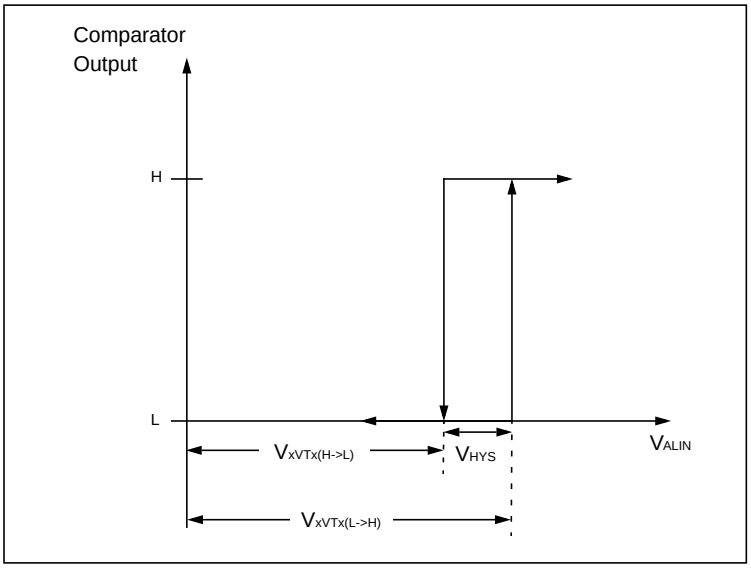
$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N: A/D converter digital output value

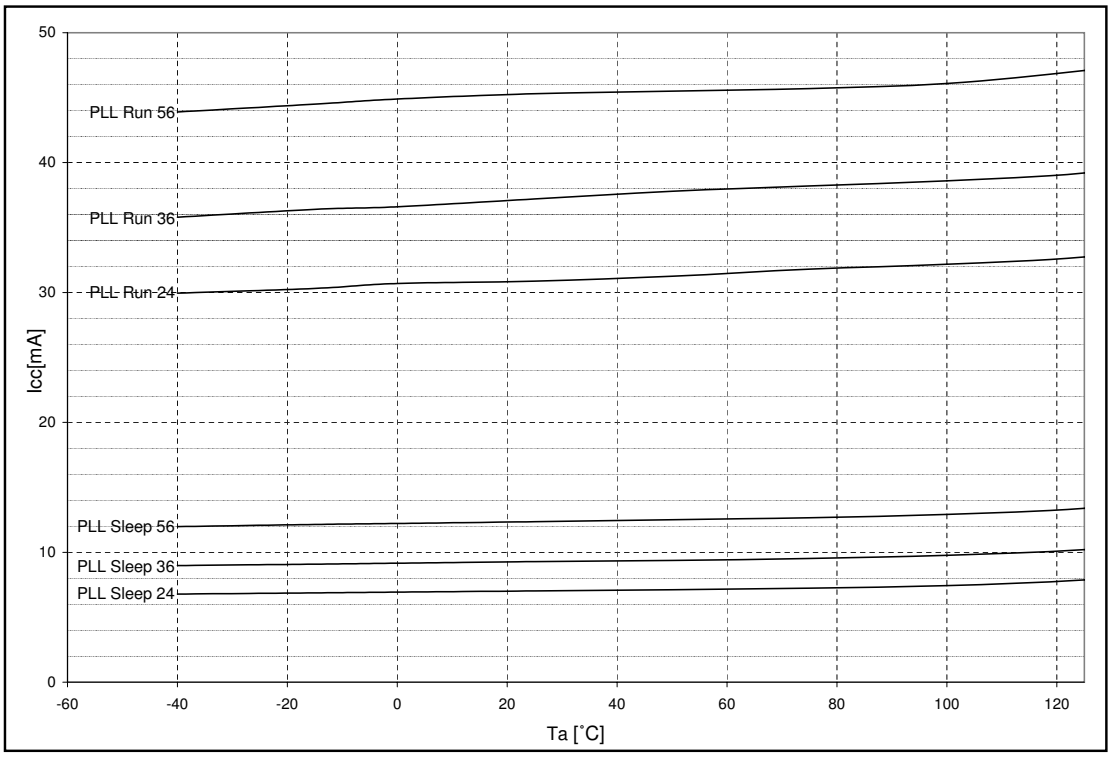
V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

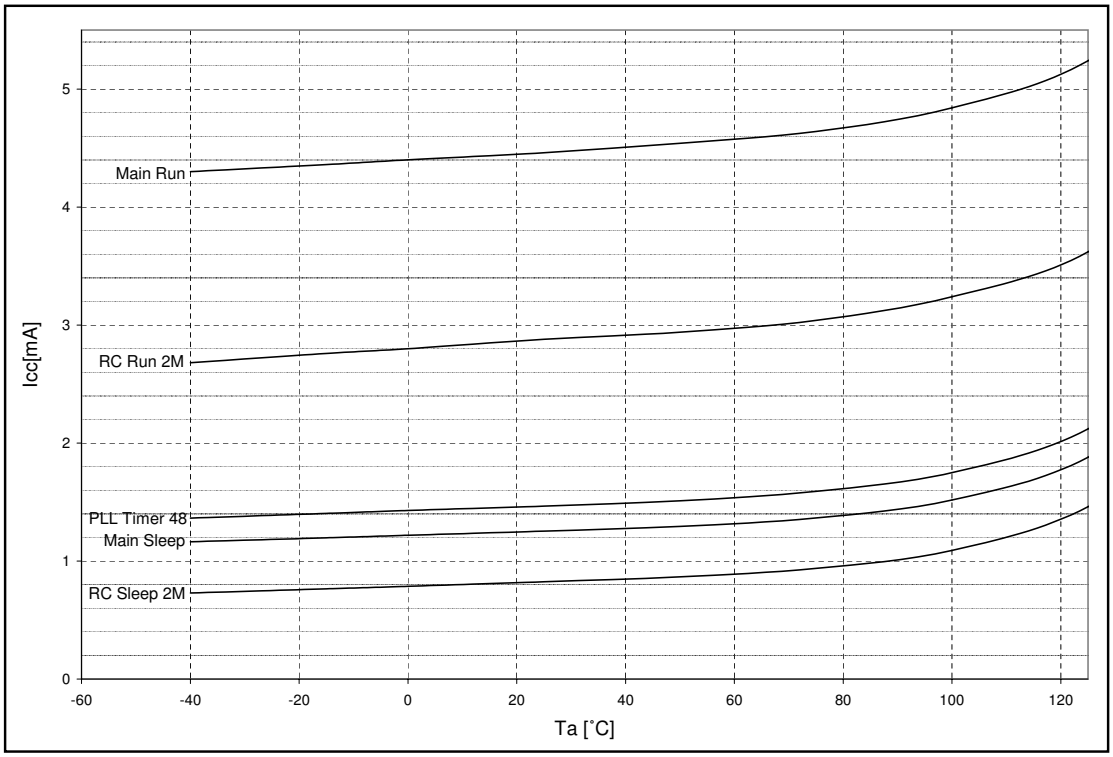
V_{NT} : A voltage at which digital output transitions from (N – 1) to N.


Comparator
Output
H
L
VALIN
VxVTx(H->L)
VHYS
VxVTx(L->H)

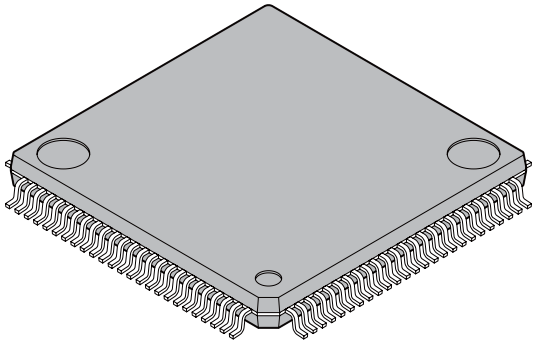
MB96F346/F347/F348Y/R/A PLL Run and Sleep mode currents



MB96F346/F347/F348Y/R/A operation modes with medium currents

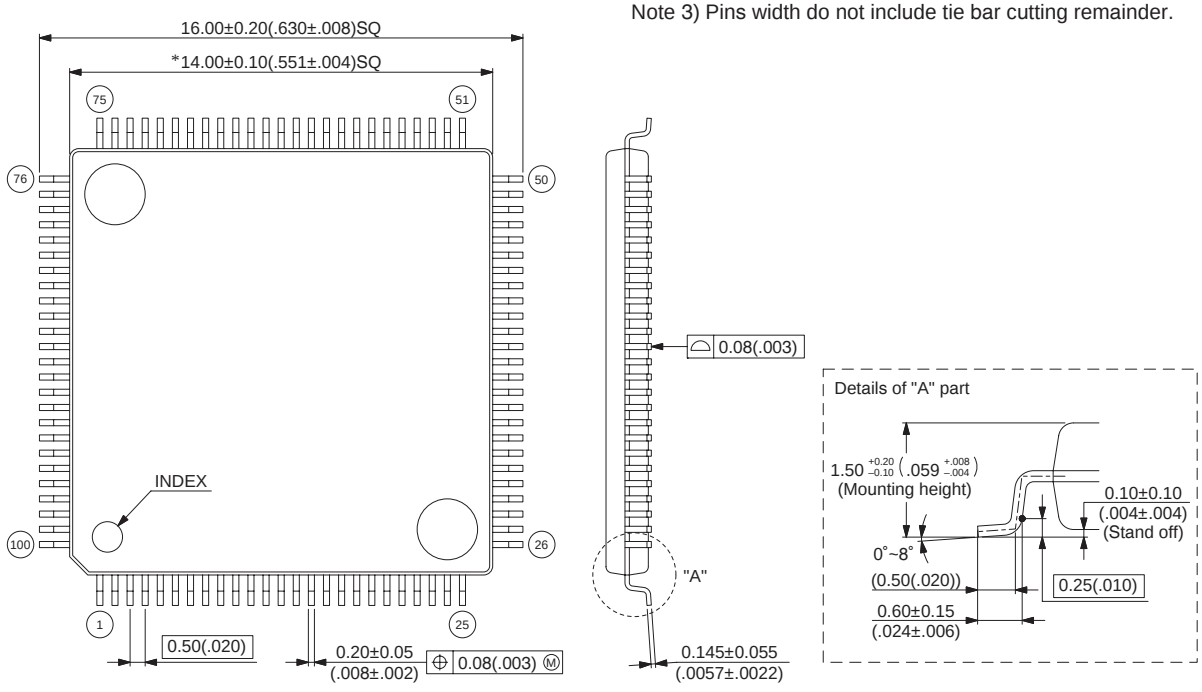


■ PACKAGE DIMENSION MB96(F)34x LQFP 100P

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MB96F346ASA, MB96F346AWA,
MB96F347ASA, MB96F347AWA,
MB96F348ASA, MB96F348AWA,
MB96F348CSB, MB96F348CWB

Revision	Date	Modification
10	2010-06-23	• I/O map: IOABK0-5 added at address 000A00H-000A05H • Ordering Information: Suffix “A” added to all MB96F345 device versions • AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg • Corrected MB96F345 part names in ordering information • Low voltage detector: Detection levels of MB96F345 updated • Example characteristics updated, new figures added showing dependency of PLL Run mode current on frequency • Updated Power Supply current spec in Run/Sleep/Timer/Stop modes (new spec items in PLL Run/Sleep mode, small adjustment of most other values) • Note added that PLL phase jitter spec does not include jitter coming from Main clock • Alarm comparator: Maximum power-up stabilization time increased to 10ms • Removed PHDR register from IO map • Note added in DC characteristics how to select driving strength of ports • I2C AC spec updated: tof, Cb and tSP spec added, wrong footnotes and Condition removed • I/O Circuit type: Note added for type “N” (slew rate control according to I2C spec) • Package dimension: Added the following sentence under the figure: “Please confirm the latest Package dimension by following URL. http://edevice.fujitsu.com/package/en-search/” • AD converter: Impact of input pin capacitance and external capacitance added to formula for calculation of the sampling time • Added specification of RC clock stabilization time • Feature description I2C: ‘8-bit addressing’ corrected to ‘7-bit addressing’ • Feature description PPG: ‘Reload timer overflow as clock input’ corrected to ‘Reload timer underflow as clock input’ • Company name updated on the cover page: Fujitsu Microelectronics Limited -> Fujitsu Semiconductor Limited • ICCLVD specification updated, at 125deg typical value is 7uA and maximum value is 20uA • Ordering information: added devices under development MB96F346A*C, MB96F347A*C, MB96F348A*C, MB96F346Y*C, MB96F347Y*C, MB96F348Y*C, MB96F346R*C, MB96F347R*C, MB96F348R*C