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What is "Embedded - Microcontrollers"?

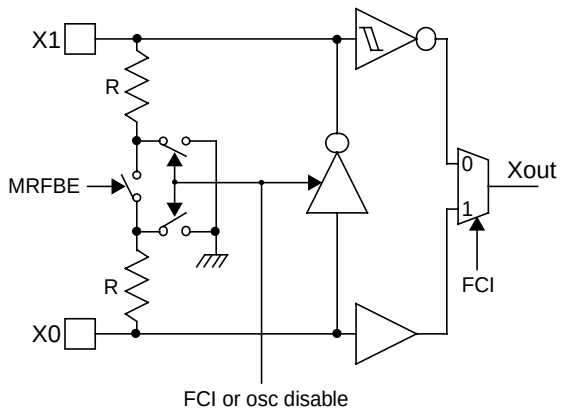
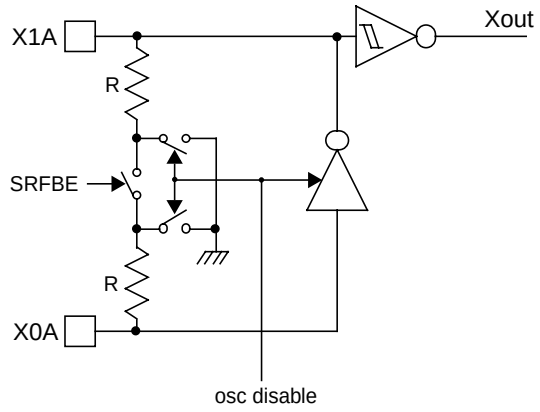
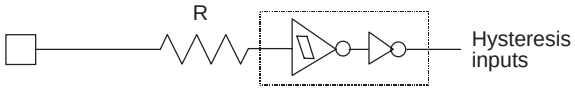
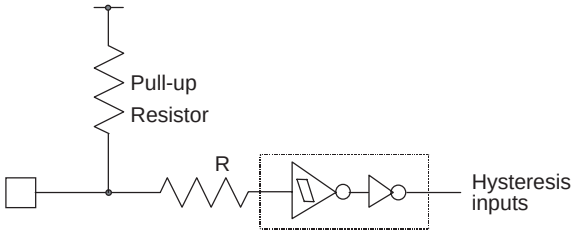
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347rwcpqc-gse2

Feature	Description
CAN	• Supports CAN protocol version 2.0 part A and B • ISO16845 certified • Bit rates up to 1 Mbit/s • 32 message objects • Each message object has its own identifier mask • Programmable FIFO mode (concatenation of message objects) • Maskable interrupt • Disabled Automatic Retransmission mode for Time Triggered CAN applications • Programmable loop-back mode for self-test operation
USART	• Full duplex USARTs (SCI/LIN) • Wide range of baud rate settings using a dedicated reload timer • Special synchronous options for adapting to different synchronous serial protocols • LIN functionality working either as master or slave LIN device
I^2C	• Up to 400 kbps • Master and Slave functionality, 7-bit and 10-bit addressing
A/D converter	• SAR-type • 10-bit resolution • Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer
A/D Converter Reference Voltage switch	• 2 independent positive A/D converter reference voltages available
Reload Timers	• 16-bit wide • Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency • Event count function
Free Running Timers	• Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency
Input Capture Units	• 16-bit wide • Signals an interrupt upon external event • Rising edge, falling edge or rising & falling edge sensitive
Output Compare Units	• 16-bit wide • Signals an interrupt when a match with 16-bit I/O Timer occurs • A pair of compare registers can be used to generate an output signal.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: • Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		• Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		• CMOS Hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

■ USER ROM MEMORY MAP FOR FLASH DEVICES

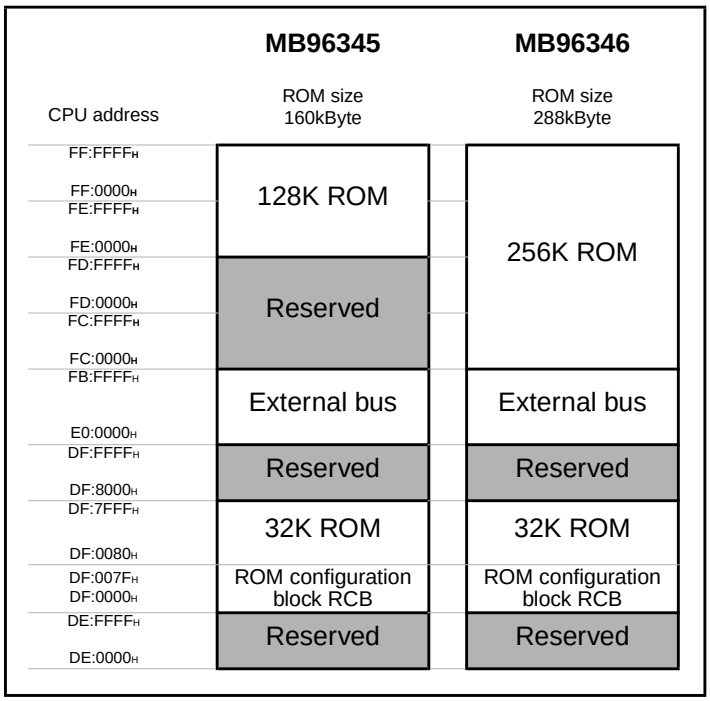
MB96F345D
MB96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	External bus	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$		
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$		
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$		
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$		
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$		
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$		
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$		
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$		
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$		
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$		
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$		
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$		
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$		
E0:FFFF$_H$ E0:0000$_H$			
DF:FFFF$_H$ DF:8000$_H$		Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K *1	
DE:FFFF$_H$ DE:0000$_H$		Reserved	
0E:FFFF$_H$ 0E:FF00$_H$	(0E:FFFF$_H$) (0E:FF00$_H$)	SDA0-256 *2	Data Flash A
0E:FEFF$_H$ 0E:0000$_H$		Reserved	
0D:FFFF$_H$ 0D:C000$_H$	(0F:FFFF$_H$) (0F:C000$_H$)	SDA4-16K	Data Flash A
0D:BFFF$_H$ 0D:8000$_H$	(0F:BFFF$_H$) (0F:8000$_H$)	SDA3-16K	
0D:7FFF$_H$ 0D:4000$_H$	(0F:7FFF$_H$) (0F:4000$_H$)	SDA2-16K	
0D:3FFF$_H$ 0D:0000$_H$	(0F:3FFF$_H$) (0F:0000$_H$)	SDA1-16K	
0C:FFFF$_H$ 0C:0000$_H$		Reserved	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

*2: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address DE:FF00$_H$ - DE:FF2F$_H$

■ USER ROM MEMORY MAP FOR MASK ROM DEVICES



■ I/O MAP

I/O map MB96(F)34x (1 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000H	I/O Port P00 - Port Data Register	PDR00		R/W
000001H	I/O Port P01 - Port Data Register	PDR01		R/W
000002H	I/O Port P02 - Port Data Register	PDR02		R/W
000003H	I/O Port P03 - Port Data Register	PDR03		R/W
000004H	I/O Port P04 - Port Data Register	PDR04		R/W
000005H	I/O Port P05 - Port Data Register	PDR05		R/W
000006H	I/O Port P06 - Port Data Register	PDR06		R/W
000007H	I/O Port P07 - Port Data Register	PDR07		R/W
000008H	I/O Port P08 - Port Data Register	PDR08		R/W
000009H	I/O Port P09 - Port Data Register	PDR09		R/W
00000AH	I/O Port P10 - Port Data Register	PDR10		R/W
00000BH-000017H	Reserved			-
000018H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019H	ADC0 - Control Status register High	ADCSH		R/W
00001AH	ADC0 - Data Register Low	ADCRL	ADCR	R
00001BH	ADC0 - Data Register High	ADCRH		R
00001CH	ADC0 - Setting Register		ADSR	R/W
00001DH	ADC0 - Setting Register			R/W
00001EH	ADC0 - Extended Configuration Register	ADECR		R/W
00001FH	Reserved			-
000020H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021H	FRT0 - Data register of free-running timer			R/W
000022H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025H	FRT1 - Data register of free-running timer			R/W

I/O map MB96(F)34x (7 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000AB$_H$	PPG5 - Control status register High	PCNH5		R/W
0000AC$_H$	I2C0 - Bus Status Register	IBSR0		R
0000AD$_H$	I2C0 - Bus Control Register	IBCR0		R/W
0000AE$_H$	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
0000AF$_H$	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
0000B0$_H$	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
0000B1$_H$	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
0000B2$_H$	I2C0 - Seven bit Slave address Register	ISBA0		R/W
0000B3$_H$	I2C0 - Seven bit Address mask Register	ISMK0		R/W
0000B4$_H$	I2C0 - Data Register	IDAR0		R/W
0000B5$_H$	I2C0 - Clock Control Register	ICCR0		R/W
0000B6$_H$	I2C1 - Bus Status Register	IBSR1		R
0000B7$_H$	I2C1 - Bus Control Register	IBCR1		R/W
0000B8$_H$	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
0000B9$_H$	I2C1 - Ten bit Slave address Register High	ITBAH1		R/W
0000BA$_H$	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
0000BB$_H$	I2C1 - Ten bit Address mask Register High	ITMKH1		R/W
0000BC$_H$	I2C1 - Seven bit Slave address Register	ISBA1		R/W
0000BD$_H$	I2C1 - Seven bit Address mask Register	ISMK1		R/W
0000BE$_H$	I2C1 - Data Register	IDAR1		R/W
0000BF$_H$	I2C1 - Clock Control Register	ICCR1		R/W
0000C0$_H$	USART0 - Serial Mode Register	SMR0		R/W
0000C1$_H$	USART0 - Serial Control Register	SCR0		R/W
0000C2$_H$	USART0 - TX Register	TDR0		W
0000C2$_H$	USART0 - RX Register	RDR0		R
0000C3$_H$	USART0 - Serial Status	SSR0		R/W
0000C4$_H$	USART0 - Control/Com. Register	ECCR0		R/W
0000C5$_H$	USART0 - Ext. Status Register	ESCR0		R/W
0000C6$_H$	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W
0000C7$_H$	USART0 - Baud Rate Generator Register High	BGRH0		R/W

I/O map MB96(F)34x (8 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000C8H	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
0000C9H	Reserved			-
0000CAH	USART1 - Serial Mode Register	SMR1		R/W
0000CBH	USART1 - Serial Control Register	SCR1		R/W
0000CCH	USART1 - TX Register	TDR1		W
0000CCH	USART1 - RX Register	RDR1		R
0000CDH	USART1 - Serial Status	SSR1		R/W
0000CEH	USART1 - Control/Com. Register	ECCR1		R/W
0000CFH	USART1 - Ext. Status Register	ESCR1		R/W
0000D0H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
0000D1H	USART1 - Baud Rate Generator Register High	BGRH1		R/W
0000D2H	USART1 - Extended Serial Interrupt Register	ESIR1		R/W
0000D3H	Reserved			-
0000D4H	USART2 - Serial Mode Register	SMR2		R/W
0000D5H	USART2 - Serial Control Register	SCR2		R/W
0000D6H	USART2 - TX Register	TDR2		W
0000D6H	USART2 - RX Register	RDR2		R
0000D7H	USART2 - Serial Status	SSR2		R/W
0000D8H	USART2 - Control/Com. Register	ECCR2		R/W
0000D9H	USART2 - Ext. Status Register	ESCR2		R/W
0000DAH	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DBH	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DCH	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DDH	Reserved			-
0000DEH	USART3 - Serial Mode Register	SMR3		R/W
0000DFH	USART3 - Serial Control Register	SCR3		R/W
0000E0H	USART3 - TX Register	TDR3		W
0000E0H	USART3 - RX Register	RDR3		R
0000E1H	USART3 - Serial Status	SSR3		R/W
0000E2H	USART3 - Control/Com. Register	ECCR3		R/W

I/O map MB96(F)34x (14 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003FC$_H$	Flash Memory Write Control register 4	FMWC4		R/W
0003FD$_H$	Flash Memory Write Control register 5	FMWC5		R/W
0003FE$_H$-0003FF$_H$	Reserved			-
000400$_H$	Standby Mode control register	SMCR		R/W
000401$_H$	Clock select register	CKSR		R/W
000402$_H$	Clock Stabilization select register	CKSSR		R/W
000403$_H$	Clock monitor register	CKMR		R
000404$_H$	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405$_H$	Clock Frequency control register High	CKFCRH		R/W
000406$_H$	PLL Control register Low	PLLCRL	PLLCR	R/W
000407$_H$	PLL Control register High	PLLCRH		R/W
000408$_H$	RC clock timer control register	RCTCR		R/W
000409$_H$	Main clock timer control register	MCTCR		R/W
00040A$_H$	Sub clock timer control register	SCTCR		R/W
00040B$_H$	Reset cause and clock status register with clear function	RCCSRC		R
00040C$_H$	Reset configuration register	RCR		R/W
00040D$_H$	Reset cause and clock status register	RCCSR		R
00040E$_H$	Watch dog timer configuration register	WDTC		R/W
00040F$_H$	Watch dog timer clear pattern register	WDTCP		W
000410$_H$-000414$_H$	Reserved			-
000415$_H$	Clock output activation register	COAR		R/W
000416$_H$	Clock output configuration register 0	COCR0		R/W
000417$_H$	Clock output configuration register 1	COCR1		R/W
000418$_H$	Clock Modulator control register	CMCR		R/W
000419$_H$	Reserved			-
00041A$_H$	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
00041B$_H$	Clock Modulator Parameter register High	CMPRH		R/W

I/O map MB96(F)34x (15 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00041C$_H$-00042B$_H$	Reserved			-
00042C$_H$	Voltage Regulator Control register	VRCR		R/W
00042D$_H$	Clock Input and LVD Control Register	CILCR		R/W
00042E$_H$-00042F$_H$	Reserved			-
000430$_H$	I/O Port P00 - Data Direction Register	DDR00		R/W
000431$_H$	I/O Port P01 - Data Direction Register	DDR01		R/W
000432$_H$	I/O Port P02 - Data Direction Register	DDR02		R/W
000433$_H$	I/O Port P03 - Data Direction Register	DDR03		R/W
000434$_H$	I/O Port P04 - Data Direction Register	DDR04		R/W
000435$_H$	I/O Port P05 - Data Direction Register	DDR05		R/W
000436$_H$	I/O Port P06 - Data Direction Register	DDR06		R/W
000437$_H$	I/O Port P07 - Data Direction Register	DDR07		R/W
000438$_H$	I/O Port P08 - Data Direction Register	DDR08		R/W
000439$_H$	I/O Port P09 - Data Direction Register	DDR09		R/W
00043A$_H$	I/O Port P10 - Data Direction Register	DDR10		R/W
00043B$_H$-000443$_H$	Reserved			-
000444$_H$	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445$_H$	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446$_H$	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447$_H$	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448$_H$	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449$_H$	I/O Port P05 - Port Input Enable Register	PIER05		R/W
00044A$_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
00044B$_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
00044C$_H$	I/O Port P08 - Port Input Enable Register	PIER08		R/W
00044D$_H$	I/O Port P09 - Port Input Enable Register	PIER09		R/W
00044E$_H$	I/O Port P10 - Port Input Enable Register	PIER10		R/W

I/O map MB96(F)34x (19 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004E9H	RTC - Timer Control Register High	WTCRH		R/W
0004EAH	CAL - Calibration unit Control register	CUCR		R/W
0004EBH	Reserved			-
0004ECH	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
0004EDH	CAL - Duration Timer Data Register High	CUTDH		R/W
0004EEH	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EFH	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0H	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1H	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2H-0004F9H	Reserved			-
0004FAH	RLT - Timer input select (for Cascading)	TMISR		R/W
0004FBH-00053DH	Reserved			-
00053EH	USART7 - Serial Mode Register	SMR7		R/W
00053FH	USART7 - Serial Control Register	SCR7		R/W
000540H	USART7 - Serial TX Register	TDR7		W
000540H	USART7 - Serial RX Register	RDR7		R
000541H	USART7 - Serial Status Register	SSR7		R/W
000542H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547H	Reserved			-
000548H	USART8 - Serial Mode Register	SMR8		R/W
000549H	USART8 - Serial Control Register	SCR8		R/W
00054AH	USART8 - Serial TX Register	TDR8		W
00054AH	USART8 - Serial RX Register	RDR8		R
00054BH	USART8 - Serial Status Register	SSR8		R/W
00054CH	USART8 - Ext. Control/Com. Register	ECCR8		R/W

I/O map MB96(F)34x (21 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00056D$_H$	PPG7 - Timer register			R
00056E$_H$	PPG7 - Period setting register		PCSR7	W
00056F$_H$	PPG7 - Period setting register			W
000570$_H$	PPG7 - Duty cycle register		PDUT7	W
000571$_H$	PPG7 - Duty cycle register			W
000572$_H$	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573$_H$	PPG7 - Control status register High	PCNH7		R/W
000574$_H$	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575$_H$	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576$_H$	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577$_H$	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578$_H$	PPG8 - Timer register		PTMR8	R
000579$_H$	PPG8 - Timer register			R
00057A$_H$	PPG8 - Period setting register		PCSR8	W
00057B$_H$	PPG8 - Period setting register			W
00057C$_H$	PPG8 - Duty cycle register		PDUT8	W
00057D$_H$	PPG8 - Duty cycle register			W
00057E$_H$	PPG8 - Control status register Low	PCNL8	PCN8	R/W
00057F$_H$	PPG8 - Control status register High	PCNH8		R/W
000580$_H$	PPG9 - Timer register		PTMR9	R
000581$_H$	PPG9 - Timer register			R
000582$_H$	PPG9 - Period setting register		PCSR9	W
000583$_H$	PPG9 - Period setting register			W
000584$_H$	PPG9 - Duty cycle register		PDUT9	W
000585$_H$	PPG9 - Duty cycle register			W
000586$_H$	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587$_H$	PPG9 - Control status register High	PCNH9		R/W
000588$_H$	PPG10 - Timer register		PTMR10	R
000589$_H$	PPG10 - Timer register			R
00058A$_H$	PPG10 - Period setting register		PCSR10	W

Interrupt vector table MB96(F)34x (2 of 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
28	38C$_H$	EXTINT11	Yes	28	External Interrupt 11
29	388$_H$	EXTINT12	Yes	29	External Interrupt 12
30	384$_H$	EXTINT13	Yes	30	External Interrupt 13
31	380$_H$	EXTINT14	Yes	31	External Interrupt 14
32	37C$_H$	EXTINT15	Yes	32	External Interrupt 15
33	378$_H$	CAN0	No	33	CAN Controller 0 (except MB96(F)34xAyy or MB96(F)34xCyy)
34	374$_H$	CAN1	No	34	CAN Controller 1 (except MB96(F)34xAyy, MB96(F)34xCyy, MB96F345Dyy or MB96F345Fyy)
35	370$_H$	PPG0	Yes	35	Programmable Pulse Generator 0
36	36C$_H$	PPG1	Yes	36	Programmable Pulse Generator 1
37	368$_H$	PPG2	Yes	37	Programmable Pulse Generator 2
38	364$_H$	PPG3	Yes	38	Programmable Pulse Generator 3
39	360$_H$	PPG4	Yes	39	Programmable Pulse Generator 4
40	35C$_H$	PPG5	Yes	40	Programmable Pulse Generator 5
41	358$_H$	PPG6	Yes	41	Programmable Pulse Generator 6
42	354$_H$	PPG7	Yes	42	Programmable Pulse Generator 7
43	350$_H$	PPG8	Yes	43	Programmable Pulse Generator 8
44	34C$_H$	PPG9	Yes	44	Programmable Pulse Generator 9
45	348$_H$	PPG10	Yes	45	Programmable Pulse Generator 10
46	344$_H$	PPG11	Yes	46	Programmable Pulse Generator 11
47	340$_H$	PPG12	Yes	47	Programmable Pulse Generator 12
48	33C$_H$	PPG13	Yes	48	Programmable Pulse Generator 13
49	338$_H$	PPG14	Yes	49	Programmable Pulse Generator 14
50	334$_H$	PPG15	Yes	50	Programmable Pulse Generator 15
51	330$_H$	RLT0	Yes	51	Reload Timer 0
52	32C$_H$	RLT1	Yes	52	Reload Timer 1
53	328$_H$	RLT2	Yes	53	Reload Timer 2
54	324$_H$	RLT3	Yes	54	Reload Timer 3

11. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

12. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13. Handling of Data Flash

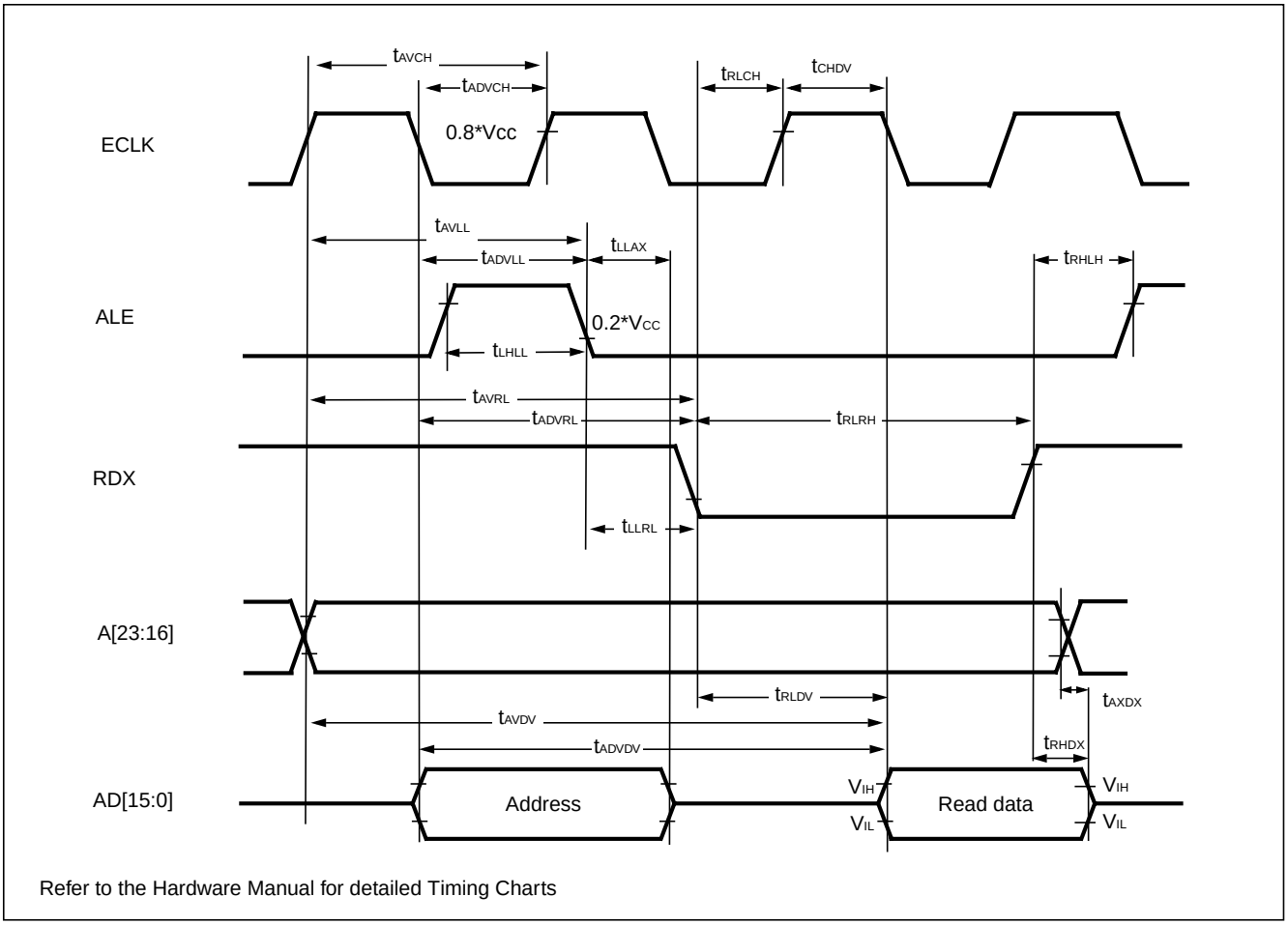
The Data Flash requires different and additional control signals for parallel programming. Please check with your programming equipment maker for support of this interface.

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	12.5	16	mA	MB96345/346
			+125˚C	13	18		
			+25˚C	12.5	16	mA	MB96F346/F347/F348Y/R/Ayy
			+125˚C	13.5	19		
			+25˚C	13.5	17	mA	MB96F348T/H/CyB/C
			+125˚C	14.5	20		
		PLL Sleep mode with CLKS1/2 = 72MHz, CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	9.5	12.5	mA	MB96F346/F347/F348Y/R/Ayy
			+125˚C	10.5	15.5		
		PLL Sleep mode with CLKS1/2 = 80MHz, CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	11	13.5	mA	MB96F345
			+125˚C	11.7	16		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	13	16	mA	MB96345/346
			+125˚C	13.5	18		
			+25˚C	15	18	mA	MB96F348T/H/CyB/C
			+125˚C	16	21		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25˚C	1.3	1.8	mA	MB96345/346
			+125˚C	1.8	3.7		
			+25˚C	1	1.3	mA	MB96F345
			+125˚C	1.6	3.4		
			+25˚C	1.3	1.8	mA	MB96F346/F347/F348
			+125˚C	1.9	4.6		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}
* The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.							



Refer to the Hardware Manual for detailed Timing Charts

Bus Timing (Write)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$ – 15	—	ns	
			EACL:ACE=1	$5t_{CYC}/2$ – 15	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC} – 15	—	ns	
			EACL:ACE=1	$2t_{CYC}$ – 15	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	t_{CYC} – 5	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	t_{CYC} – 20	—	ns	w/o cycle extension

6. Alarm Comparator

(T_A = -40 ˚C to +125 ˚C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	µA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	µA	T_A = 25 ˚C
			-3	-	+3	µA	T_A = 125 ˚C
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		0.36 * AV_{CC} -0.25	0.36 * AV_{CC} -0.1	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$		-	0.36 * AV_{CC} +0.1	0.36 * AV_{CC} +0.25	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		0.78 * AV_{CC} -0.25	0.78 * AV_{CC} -0.1	-	V	
External high threshold low->high transition	$V_{EVTH(L->H)}$			0.78 * AV_{CC} +0.1	0.78 * AV_{CC} +0.25	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	µs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	µs	CMD = 0 (slow)
Power-up stabilization time after enabling alarm comparator	t_{PD}		-	1	10	ms	Threshold levels specified above are not guaranteed within this time
Slow/Fast mode transition time	t_{CMD}		-	100	500	µs	

8. FLASH memory program/erase characteristics

(T_A = -40˚C to 105˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time Program/Data Flash (Main Flash)	-	0.9	3.6	s	Without erasure pre-programming time
Sector erase time Data Flash	-	0.5	2	s	Without erasure pre-programming time
	-	0.8	3.6	s	Including erasure pre-programming time
Chip erase time Program/Data Flash (Main Flash)	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Chip erase time Data Flash	-	2.5	10	s	Without erasure pre-programming time
	-	3.7	16.4	s	Including erasure pre-programming time
Word (16-bit width) programming time Program/Data Flash (Main Flash)	-	23	370	us	Without overhead time for submitting write command
Byte (8-bit width) programming time Data Flash	-	15	100	us	Without overhead time for submitting write command
Program/Erase cycle	10 000	-	-	cycle	100 000 Program/Erase cycles are under evaluation by Fujitsu Microelectronics
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

Mode name	Details
Sub Sleep	Sub Sleep mode current I_{CCSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped
PLL Timer 48	PLL Timer mode current I_{CCTPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 48MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Timer	Main Timer mode current $I_{CCTMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 4MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Sub oscillator stopped
RC Timer 2M	RC Timer mode current I_{CCTRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2}$ = 2MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
RC Timer 100k	RC Timer mode current I_{CCTRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Timer	Sub Timer mode current I_{CCTSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped
Stop 1.8V	Stop mode current I_{CCH} with the following settings: • Regulator in Low Power Mode B (by hardware) • Core voltage at 1.8V (VRCR:LPMB[2:0] = 110_B)
Stop 1.2V	Stop mode current I_{CCH} with the following settings: • Regulator in Low Power Mode B (by hardware) • Core voltage at 1.2V (VRCR:LPMB[2:0] = 000_B)

■ REVISION HISTORY

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.