Infineon Technologies - MB96F348RSCPMC-GSE2 Datasheet

Welcome to E-XFL.COM

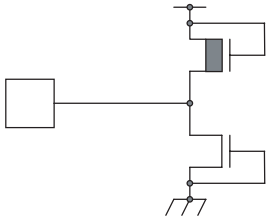
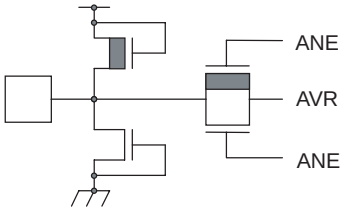
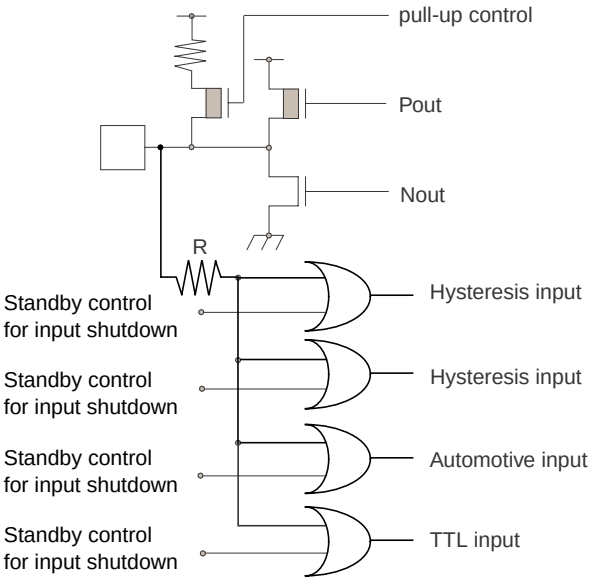
What is "Embedded - Microcontrollers"?

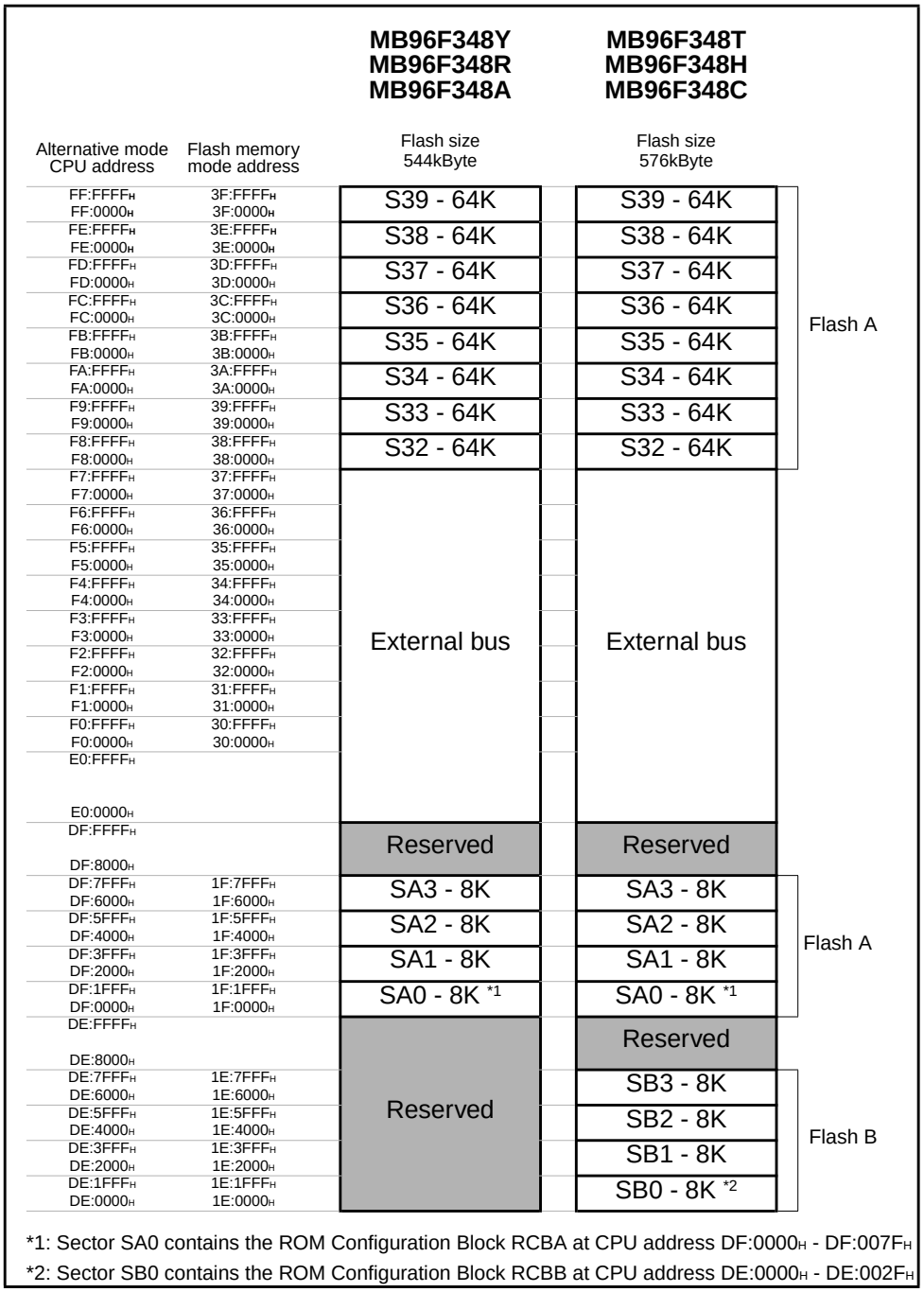
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348rscpmc-gse2

Feature	Description
I/O Ports	• Virtually all external pins can be used as general purpose I/O • All push-pull outputs (except when used as I2C SDA/SCL line) • Bit-wise programmable as input/output or peripheral signal • Bit-wise programmable input enable • Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices) • Bit-wise programmable pull-up resistor • Bit-wise programmable output driving strength for EMI optimization
Packages	• 100-pin plastic QFP and LQFP
Flash Memory	• Supports automatic programming, Embedded Algorithm • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 • Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function * • Automotive input with input shutdown function • TTL input with input shutdown function * • Programmable pull-up resistor: 50kΩ approx. Note: MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000H - DF:007FH

*2: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000H - DE:002FH

I/O map MB96(F)34x (2 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000026H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028H	OCU0 - Output Compare Control Status	OCS0		R/W
000029H	OCU1 - Output Compare Control Status	OCS1		R/W
00002AH	OCU0 - Compare Register		OCCP0	R/W
00002BH	OCU0 - Compare Register			R/W
00002CH	OCU1 - Compare Register		OCCP1	R/W
00002DH	OCU1 - Compare Register			R/W
00002EH	OCU2 - Output Compare Control Status	OCS2		R/W
00002FH	OCU3 - Output Compare Control Status	OCS3		R/W
000030H	OCU2 - Compare Register		OCCP2	R/W
000031H	OCU2 - Compare Register			R/W
000032H	OCU3 - Compare Register		OCCP3	R/W
000033H	OCU3 - Compare Register			R/W
000034H	OCU4 - Output Compare Control Status	OCS4		R/W
000035H	OCU5 - Output Compare Control Status	OCS5		R/W
000036H	OCU4 - Compare Register		OCCP4	R/W
000037H	OCU4 - Compare Register			R/W
000038H	OCU5 - Compare Register		OCCP5	R/W
000039H	OCU5 - Compare Register			R/W
00003AH	OCU6 - Output Compare Control Status	OCS6		R/W
00003BH	OCU7 - Output Compare Control Status	OCS7		R/W
00003CH	OCU6 - Compare Register		OCCP6	R/W
00003DH	OCU6 - Compare Register			R/W
00003EH	OCU7 - Compare Register		OCCP7	R/W
00003FH	OCU7 - Compare Register			R/W
000040H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041H	ICU0/ICU1 - Edge register	ICE01		R/W
000042H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R

I/O map MB96(F)34x (6 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00008D$_H$	PPG2 - Duty cycle register			W
00008E$_H$	PPG2 - Control status register Low	PCNL2	PCN2	R/W
00008F$_H$	PPG2 - Control status register High	PCNH2		R/W
000090$_H$	PPG3 - Timer register		PTMR3	R
000091$_H$	PPG3 - Timer register			R
000092$_H$	PPG3 - Period setting register		PCSR3	W
000093$_H$	PPG3 - Period setting register			W
000094$_H$	PPG3 - Duty cycle register		PDUT3	W
000095$_H$	PPG3 - Duty cycle register			W
000096$_H$	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097$_H$	PPG3 - Control status register High	PCNH3		R/W
000098$_H$	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099$_H$	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
00009A$_H$	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
00009B$_H$	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
00009C$_H$	PPG4 - Timer register		PTMR4	R
00009D$_H$	PPG4 - Timer register			R
00009E$_H$	PPG4 - Period setting register		PCSR4	W
00009F$_H$	PPG4 - Period setting register			W
0000A0$_H$	PPG4 - Duty cycle register		PDUT4	W
0000A1$_H$	PPG4 - Duty cycle register			W
0000A2$_H$	PPG4 - Control status register Low	PCNL4	PCN4	R/W
0000A3$_H$	PPG4 - Control status register High	PCNH4		R/W
0000A4$_H$	PPG5 - Timer register		PTMR5	R
0000A5$_H$	PPG5 - Timer register			R
0000A6$_H$	PPG5 - Period setting register		PCSR5	W
0000A7$_H$	PPG5 - Period setting register			W
0000A8$_H$	PPG5 - Duty cycle register		PDUT5	W
0000A9$_H$	PPG5 - Duty cycle register			W
0000AA$_H$	PPG5 - Control status register Low	PCNL5	PCN5	R/W

I/O map MB96(F)34x (10 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000117H	DMA2 - Data counter high byte	DCTH2		R/W
000118H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011AH	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011BH	DMA3 - DMA control register	DMACS3		R/W
00011CH	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011DH	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011EH	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011FH	DMA3 - Data counter high byte	DCTH3		R/W
000120H	DMA4 - Buffer address pointer low byte	BAPL4		R/W
000121H	DMA4 - Buffer address pointer middle byte	BAPM4		R/W
000122H	DMA4 - Buffer address pointer high byte	BAPH4		R/W
000123H	DMA4 - DMA control register	DMACS4		R/W
000124H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125H	DMA4 - I/O register address pointer high byte	IOAH4		R/W
000126H	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127H	DMA4 - Data counter high byte	DCTH4		R/W
000128H	DMA5 - Buffer address pointer low byte	BAPL5		R/W
000129H	DMA5 - Buffer address pointer middle byte	BAPM5		R/W
00012AH	DMA5 - Buffer address pointer high byte	BAPH5		R/W
00012BH	DMA5 - DMA control register	DMACS5		R/W
00012CH	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
00012DH	DMA5 - I/O register address pointer high byte	IOAH5		R/W
00012EH	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
00012FH	DMA5 - Data counter high byte	DCTH5		R/W
000130H-00017FH	Reserved			-
000180H-00037FH	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380H	DMA0 - Interrupt select	DISEL0		R/W
000381H	DMA1 - Interrupt select	DISEL1		R/W

I/O map MB96(F)34x (16 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00044F$_H$-000457$_H$	Reserved			-
000458$_H$	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459$_H$	I/O Port P01 - Port Input Level Register	PILR01		R/W
00045A$_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
00045B$_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
00045C$_H$	I/O Port P04 - Port Input Level Register	PILR04		R/W
00045D$_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
00045E$_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
00045F$_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460$_H$	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461$_H$	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462$_H$	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463$_H$-00046B$_H$	Reserved			-
00046C$_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
00046D$_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
00046E$_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
00046F$_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470$_H$	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471$_H$	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472$_H$	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473$_H$	I/O Port P07 - Extended Port Input Level Register	EPILR07		R/W
000474$_H$	I/O Port P08 - Extended Port Input Level Register	EPILR08		R/W
000475$_H$	I/O Port P09 - Extended Port Input Level Register	EPILR09		R/W
000476$_H$	I/O Port P10 - Extended Port Input Level Register	EPILR10		R/W
000477$_H$-00047F$_H$	Reserved			-
000480$_H$	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481$_H$	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482$_H$	I/O Port P02 - Port Output Drive Register	PODR02		R/W

I/O map MB96(F)34x (20 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00054D$_H$	USART8 - Ext. Status Com. Register	ESCR8		R/W
00054E$_H$	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
00054F$_H$	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550$_H$	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551$_H$	Reserved			-
000552$_H$	USART9 - Serial Mode Register	SMR9		R/W
000553$_H$	USART9 - Serial Control Register	SCR9		R/W
000554$_H$	USART9 - Serial TX Register	TDR9		W
000554$_H$	USART9 - Serial RX Register	RDR9		R
000555$_H$	USART9 - Serial Status Register	SSR9		R/W
000556$_H$	USART9 - Ext. Control/Com. Register	ECCR9		R/W
000557$_H$	USART9 - Ext. Status Com. Register	ESCR9		R/W
000558$_H$	USART9 - Baud Rate Generator Register Low	BGRL9	BGR9	R/W
000559$_H$	USART9 - Baud Rate Generator Register High	BGRH9		R/W
00055A$_H$	USART9 - Extended Serial Interrupt Register	ESIR9		R/W
00055B$_H$-00055F$_H$	Reserved			-
000560$_H$	ALARM0 - Control Status Register	ACSR0		R/W
000561$_H$	ALARM0 - Extended Control Status Register	AECSR0		R/W
000562$_H$	ALARM1 - Control Status Register	ACSR1		R/W
000563$_H$	ALARM1 - Extended Control Status Register	AECSR1		R/W
000564$_H$	PPG6 - Timer register		PTMR6	R
000565$_H$	PPG6 - Timer register			R
000566$_H$	PPG6 - Period setting register		PCSR6	W
000567$_H$	PPG6 - Period setting register			W
000568$_H$	PPG6 - Duty cycle register		PDUT6	W
000569$_H$	PPG6 - Duty cycle register			W
00056A$_H$	PPG6 - Control status register Low	PCNL6	PCN6	R/W
00056B$_H$	PPG6 - Control status register High	PCNH6		R/W
00056C$_H$	PPG7 - Timer register		PTMR7	R

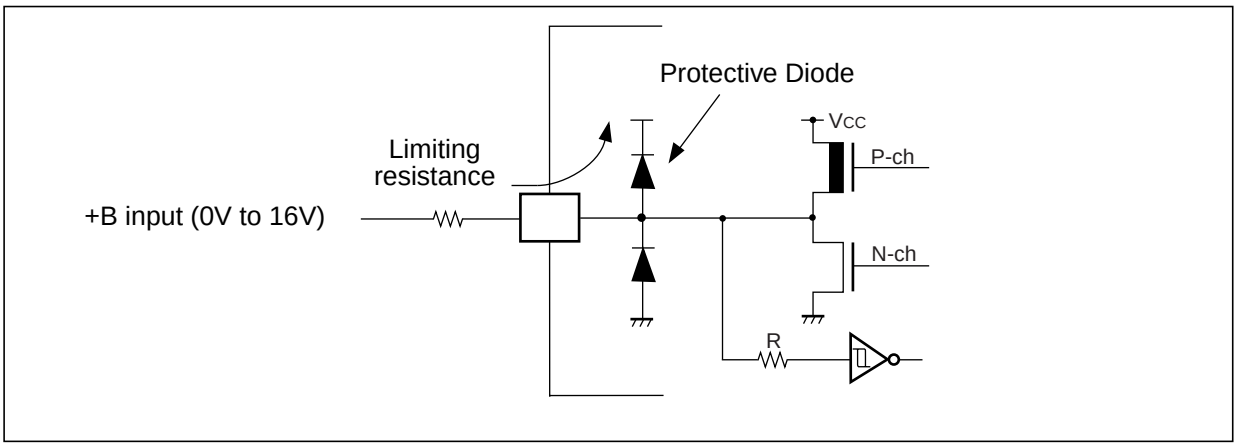
I/O map MB96(F)34x (27 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000790H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791H	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793H	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794H-00079FH	Reserved			-
0007A0H	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
0007A1H	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
0007A2H	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R
0007A3H	CAN0 - Interrupt Pending 2 Register High	INTPND2H0		R
0007A4H-0007AFH	Reserved			-
0007B0H	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
0007B1H	CAN0 - Message Valid 1 Register High	MSGVAL1H0		R
0007B2H	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
0007B3H	CAN0 - Message Valid 2 Register High	MSGVAL2H0		R
0007B4H-0007CDH	Reserved			-
0007CEH	CAN0 - Output enable register	COER0		R/W
0007CFH-0007FFH	Reserved			-
000800H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803H	CAN1 - Status register High (reserved)	STATRH1		R
000804H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809H	CAN1 - Interrupt Register High	INTRH1		R

I/O map MB96(F)34x (29 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000840H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841H	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
00084AH	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
00084BH	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
00084CH	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
00084DH	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
00084EH	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
00084FH	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851H	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853H	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855H	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856H-00087FH	Reserved			-
000880H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R
000884H-00088FH	Reserved			-

• Sample recommended circuits:



*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \sum (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
I_A is the analog current consumption into AV_{CC}.

*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*6: Please contact Fujitsu for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

3. DC characteristics

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in MB96F345
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	Not available in MB96F345
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in MB96F34xY/R/AxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in MB96F345
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	Not available in MB96F345
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in MB96F34xY/R/AxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	12.5	16	mA	MB96345/346
			+125˚C	13	18		
			+25˚C	12.5	16	mA	MB96F346/F347/F348Y/R/Ayy
			+125˚C	13.5	19		
			+25˚C	13.5	17	mA	MB96F348T/H/CyB/C
			+125˚C	14.5	20		
		PLL Sleep mode with CLKS1/2 = 72MHz, CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	9.5	12.5	mA	MB96F346/F347/F348Y/R/Ayy
			+125˚C	10.5	15.5		
		PLL Sleep mode with CLKS1/2 = 80MHz, CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	11	13.5	mA	MB96F345
			+125˚C	11.7	16		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	13	16	mA	MB96345/346
			+125˚C	13.5	18		
			+25˚C	15	18	mA	MB96F348T/H/CyB/C
			+125˚C	16	21		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25˚C	1.3	1.8	mA	MB96345/346
			+125˚C	1.8	3.7		
			+25˚C	1	1.3	mA	MB96F345
			+125˚C	1.6	3.4		
			+25˚C	1.3	1.8	mA	MB96F346/F347/F348
			+125˚C	1.9	4.6		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped)	+25˚C	1.4	1.9	mA	MB96345/346
			+125˚C	1.9	3.9		
			+25˚C	1.3	1.8	mA	MB96F345
			+125˚C	1.9	4		
			+25˚C	1.5	2	mA	MB96F346/F347/F348
			+125˚C	2.1	5		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.35	0.5	mA	MB96345/346
			+125˚C	0.7	2.3		
			+25˚C	0.11	0.2	mA	MB96F345
			+125˚C	0.63	2.2		
			+25˚C	0.35	0.5	mA	MB96F346/F347/F348
			+125˚C	0.85	3.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.08	0.15	mA	MB96345/346
			+125˚C	0.47	1.9		
			+25˚C	0.08	0.15	mA	MB96F345
			+125˚C	0.6	2.1		
			+25˚C	0.08	0.15	mA	MB96F346/F347/F348
			+125˚C	0.6	2.9		

I²C Timing

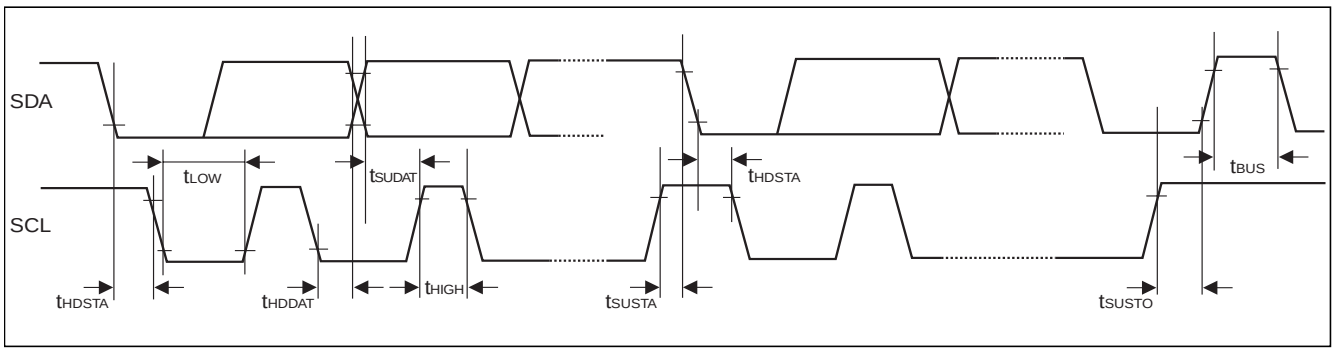
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V,V_{SS} = AV_{SS} =0V)

Parameter	Symbol	Standard-mode		Fast-mode*1		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}	4.0	—	0.6	—	µs
“L” width of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
“H” width of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}	4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}	0	3.45	0	0.9	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}	250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}	4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}	4.7	—	1.3	—	µs
Output fall time from 0.7*Vcc to 0.3*Vcc with a bus capacitance from 10 pF to 400 pF	t_{of}	20 + 0.1*C_b *2	250	20 + 0.1*C_b *2	250	ns
Capacitive load for each bus line	C_b	—	400	—	400	pF
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	n/a	n/a	0	1*t_{CLKP1}*3	ns

*1 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.

*2 : C_b = capacitance of one bus line in pF.

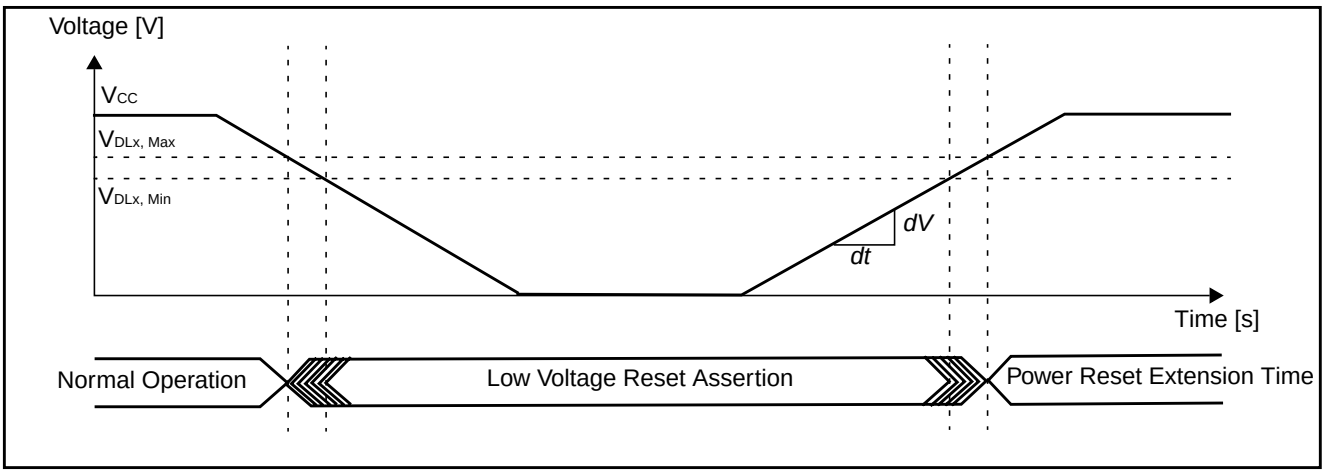
*3 : t_{CLKP1} is the cycle time of the periperal clock CLKP1.



- V_{OH} = 0.7 * V_{CC}
- V_{OL} = 0.3 * V_{CC}
- CMOS Hysteresis 0.7/0.3 input selected

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



■ EXAMPLE CHARACTERISTICS

1. Temperature dependency of power supply currents

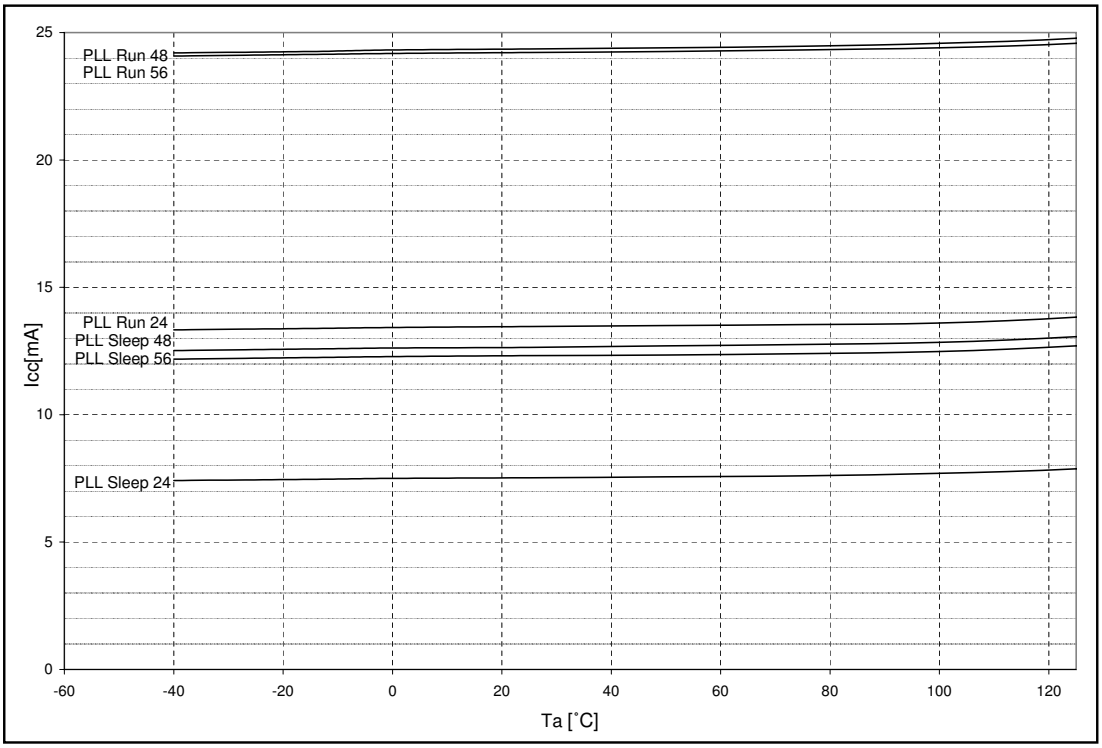
The following diagrams show the current consumption of samples with typical wafer process parameters in different operation modes.

Common condition for all operation modes:
- V_{CC} = AV_{CC} = 5.0V
- Main clock = 4MHz external clock
- Sub clock = 32kHz external clock

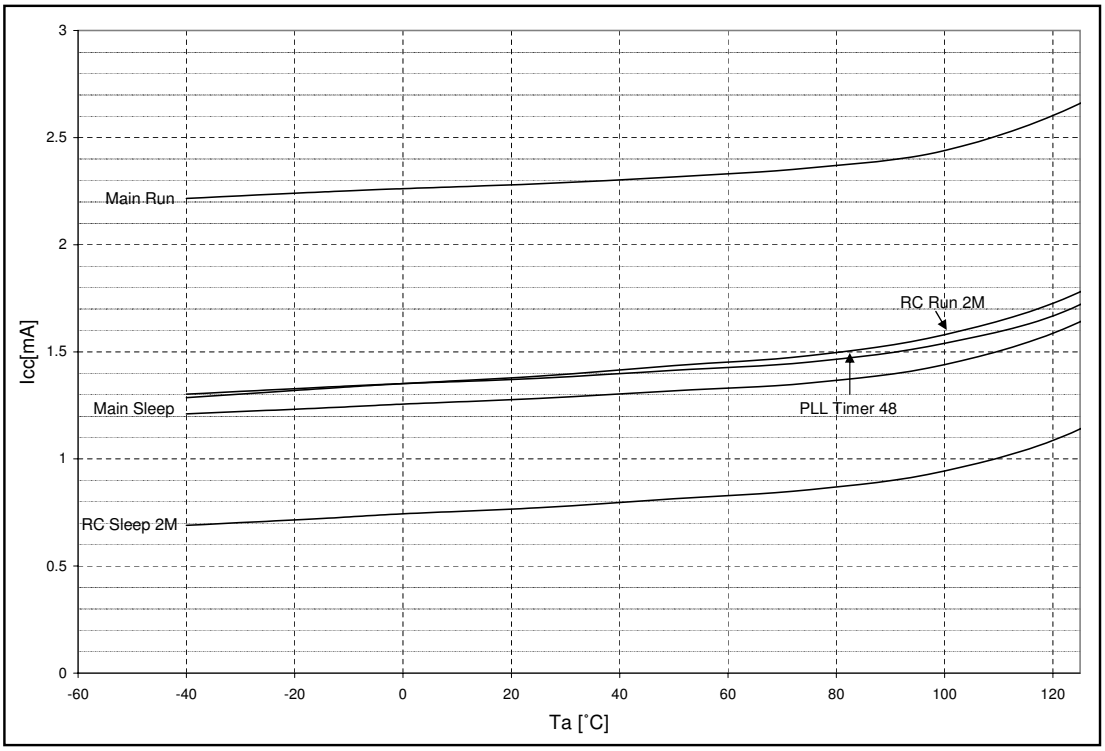
Operation mode details:

Mode name	Details
PLL Run 56	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = 56MHz • f_{CLKP2} = 28MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 2 Flash/ROM wait states (MTCRA=$233A_H$) • RC oscillator and Sub oscillator stopped
PLL Run 48	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 96MHz • f_{CLKB} = f_{CLKP1} = 48MHz • f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 1 Flash/ROM wait states (MTCRA=$6B09_H$) • RC oscillator and Sub oscillator stopped
PLL Run 40	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 80MHz • f_{CLKB} = f_{CLKP1} = 40MHz • f_{CLKP2} = 20MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 1 Flash/ROM wait states (MTCRA=$6B09_H$) • RC oscillator and Sub oscillator stopped
PLL Run 36	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 72MHz • f_{CLKB} = f_{CLKP1} = 36MHz • f_{CLKP2} = 18MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 1 Flash/ROM wait states (MTCRA=$6B09_H$) • RC oscillator and Sub oscillator stopped

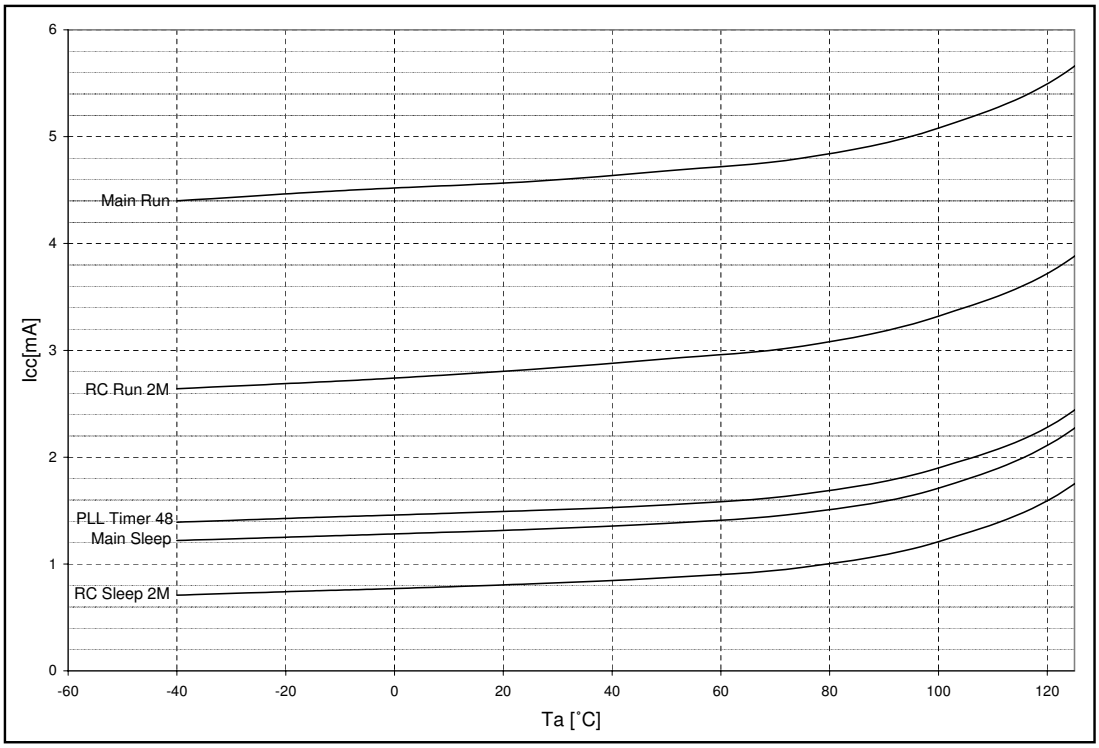
MB96345/346 PLL Run and Sleep mode currents



MB96345/346 operation modes with medium currents



MB96F348T/H/C operation modes with medium currents



MB96F348T/H/C Low power mode currents