Infineon Technologies - MB96F348RWCPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

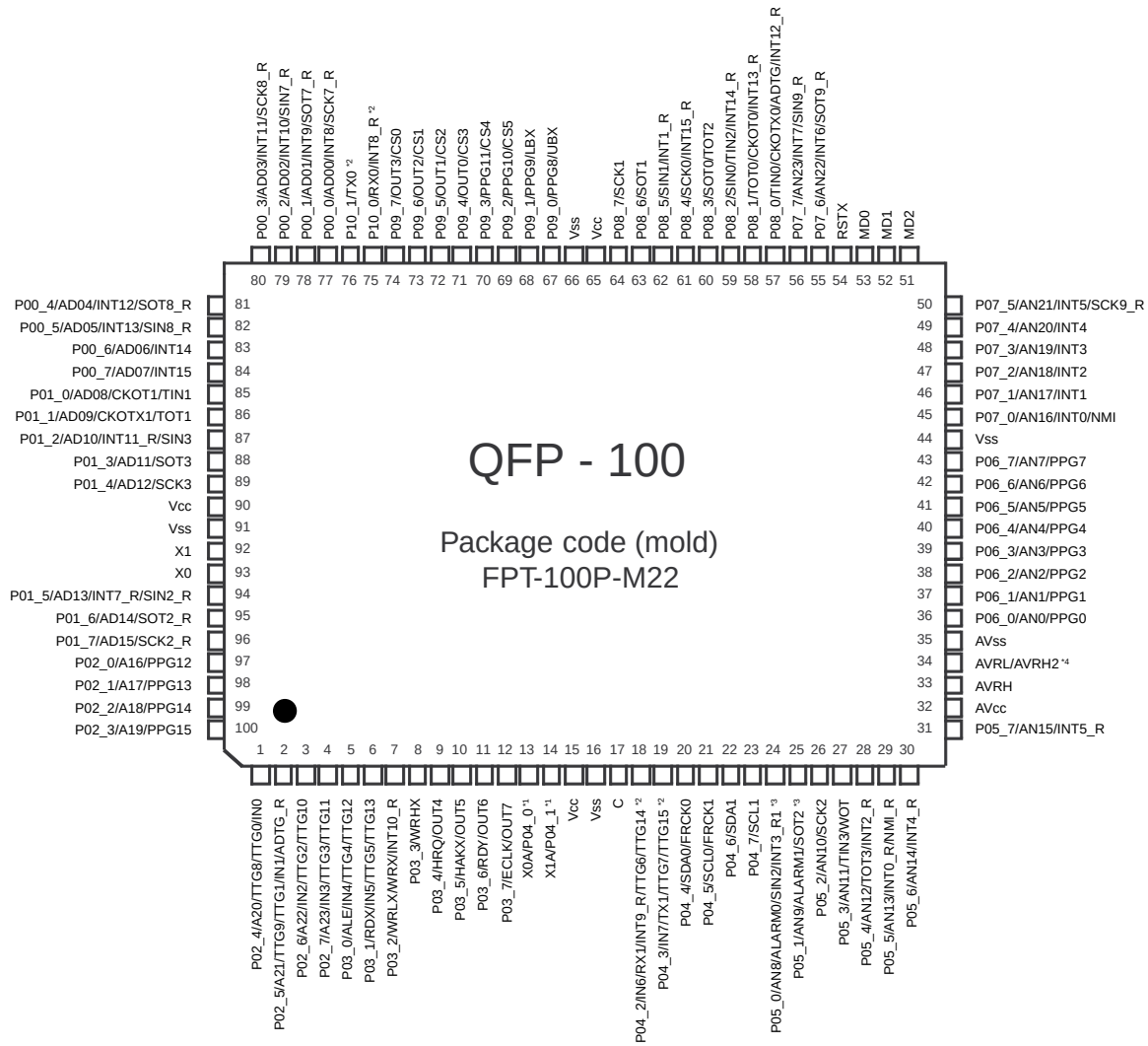
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348rwcpmc-gse2

Features	MB96V300B	MB96(F)34x
DMA	16 channels	6 channels
USART	10 channels	7 channels
I2C	2 channels	2 channels
A/D Converter	40 channels	24 channels
A/D Converter Reference Voltage switch	yes	yes (except MB96F345Dyy or MB96F345Fyy)
16-bit Reload Timer	6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer	4 channels	2 channels
16-bit Output Compare	12 channels	8 channels
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	16 channels
CAN Interface	5 channels	MB96(F)34xAyy or MB96(F)34xCyy: no MB96F345Dyy or MB96F345Fyy: 1 channel others: 2 channels
External Interrupts	16 channels	
Non-Maskable Interrupt	1 channel	
Real Time Clock	1	
I/O Ports	136	80 for part number with suffix "W", 82 for part number with suffix "S"
Alarm comparator	2 channels	MB96F345Dyy or MB96F345Fyy: no others: 2 channels
External bus interface	Yes	Yes (multiplexed address/data)
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

■ PIN ASSIGNMENTS

Pin assignment of MB96(F)34x (FPT-100P-M22)



*1: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

*2: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

*3: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

*4: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F²MC-16LX family MB90340 series.

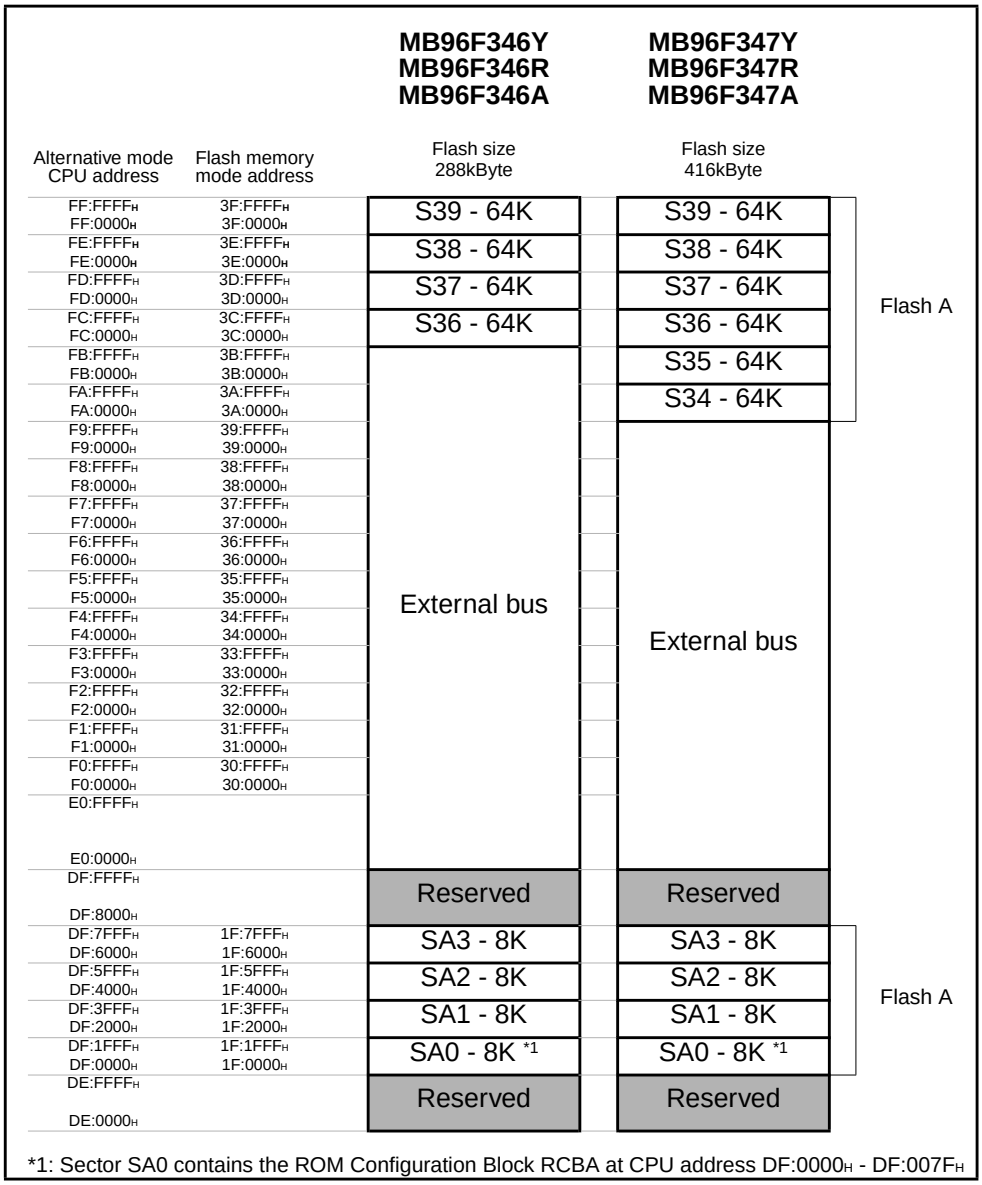
■ USER ROM MEMORY MAP FOR FLASH DEVICES

MB96F345D
MB96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	External bus	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$		
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$		
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$		
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$		
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$		
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$		
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$		
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$		
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$		
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$		
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$		
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$		
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$		
E0:FFFF$_H$ E0:0000$_H$			
DF:FFFF$_H$ DF:8000$_H$		Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K *1	
DE:FFFF$_H$ DE:0000$_H$		Reserved	
0E:FFFF$_H$ 0E:FF00$_H$	(0E:FFFF$_H$) (0E:FF00$_H$)	SDA0-256 *2	Data Flash A
0E:FEFF$_H$ 0E:0000$_H$		Reserved	
0D:FFFF$_H$ 0D:C000$_H$	(0F:FFFF$_H$) (0F:C000$_H$)	SDA4-16K	Data Flash A
0D:BFFF$_H$ 0D:8000$_H$	(0F:BFFF$_H$) (0F:8000$_H$)	SDA3-16K	
0D:7FFF$_H$ 0D:4000$_H$	(0F:7FFF$_H$) (0F:4000$_H$)	SDA2-16K	
0D:3FFF$_H$ 0D:0000$_H$	(0F:3FFF$_H$) (0F:0000$_H$)	SDA1-16K	
0C:FFFF$_H$ 0C:0000$_H$		Reserved	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

*2: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address DE:FF00$_H$ - DE:FF2F$_H$



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000H - DF:007FH

I/O map MB96(F)34x (8 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000C8H	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
0000C9H	Reserved			-
0000CAH	USART1 - Serial Mode Register	SMR1		R/W
0000CBH	USART1 - Serial Control Register	SCR1		R/W
0000CCH	USART1 - TX Register	TDR1		W
0000CCH	USART1 - RX Register	RDR1		R
0000CDH	USART1 - Serial Status	SSR1		R/W
0000CEH	USART1 - Control/Com. Register	ECCR1		R/W
0000CFH	USART1 - Ext. Status Register	ESCR1		R/W
0000D0H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
0000D1H	USART1 - Baud Rate Generator Register High	BGRH1		R/W
0000D2H	USART1 - Extended Serial Interrupt Register	ESIR1		R/W
0000D3H	Reserved			-
0000D4H	USART2 - Serial Mode Register	SMR2		R/W
0000D5H	USART2 - Serial Control Register	SCR2		R/W
0000D6H	USART2 - TX Register	TDR2		W
0000D6H	USART2 - RX Register	RDR2		R
0000D7H	USART2 - Serial Status	SSR2		R/W
0000D8H	USART2 - Control/Com. Register	ECCR2		R/W
0000D9H	USART2 - Ext. Status Register	ESCR2		R/W
0000DAH	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DBH	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DCH	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DDH	Reserved			-
0000DEH	USART3 - Serial Mode Register	SMR3		R/W
0000DFH	USART3 - Serial Control Register	SCR3		R/W
0000E0H	USART3 - TX Register	TDR3		W
0000E0H	USART3 - RX Register	RDR3		R
0000E1H	USART3 - Serial Status	SSR3		R/W
0000E2H	USART3 - Control/Com. Register	ECCR3		R/W

I/O map MB96(F)34x (9 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000E3H	USART3 - Ext. Status Register	ESCR3		R/W
0000E4H	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
0000E5H	USART3 - Baud Rate Generator Register High	BGRH3		R/W
0000E6H	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
0000E7H-0000EFH	Reserved			-
0000F0H-0000FFH	External Bus area	EXTBUS0		R/W
000100H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103H	DMA0 - DMA control register	DMACS0		R/W
000104H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107H	DMA0 - Data counter high byte	DCTH0		R/W
000108H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010AH	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010BH	DMA1 - DMA control register	DMACS1		R/W
00010CH	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
00010DH	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010EH	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010FH	DMA1 - Data counter high byte	DCTH1		R/W
000110H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113H	DMA2 - DMA control register	DMACS2		R/W
000114H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W

I/O map MB96(F)34x (12 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003B5H	Memory patch control/status register ch 4/5			R/W
0003B6H	Memory patch control/status register ch 6/7		PFCS3	R/W
0003B7H	Memory patch control/status register ch 6/7			R/W
0003B8H	Memory Patch function - Patch address 0 low	PFAL0		R/W
0003B9H	Memory Patch function - Patch address 0 middle	PFAM0		R/W
0003BAH	Memory Patch function - Patch address 0 high	PFAH0		R/W
0003BBH	Memory Patch function - Patch address 1 low	PFAL1		R/W
0003BCH	Memory Patch function - Patch address 1 middle	PFAM1		R/W
0003BDH	Memory Patch function - Patch address 1 high	PFAH1		R/W
0003BEH	Memory Patch function - Patch address 2 low	PFAL2		R/W
0003BFH	Memory Patch function - Patch address 2 middle	PFAM2		R/W
0003C0H	Memory Patch function - Patch address 2 high	PFAH2		R/W
0003C1H	Memory Patch function - Patch address 3 low	PFAL3		R/W
0003C2H	Memory Patch function - Patch address 3 middle	PFAM3		R/W
0003C3H	Memory Patch function - Patch address 3 high	PFAH3		R/W
0003C4H	Memory Patch function - Patch address 4 low	PFAL4		R/W
0003C5H	Memory Patch function - Patch address 4 middle	PFAM4		R/W
0003C6H	Memory Patch function - Patch address 4 high	PFAH4		R/W
0003C7H	Memory Patch function - Patch address 5 low	PFAL5		R/W
0003C8H	Memory Patch function - Patch address 5 middle	PFAM5		R/W
0003C9H	Memory Patch function - Patch address 5 high	PFAH5		R/W
0003CAH	Memory Patch function - Patch address 6 low	PFAL6		R/W
0003CBH	Memory Patch function - Patch address 6 middle	PFAM6		R/W
0003CCH	Memory Patch function - Patch address 6 high	PFAH6		R/W
0003CDH	Memory Patch function - Patch address 7 low	PFAL7		R/W
0003CEH	Memory Patch function - Patch address 7 middle	PFAM7		R/W
0003CFH	Memory Patch function - Patch address 7 high	PFAH7		R/W
0003D0H	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
0003D1H	Memory Patch function - Patch data 0 High	PFDH0		R/W
0003D2H	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W

I/O map MB96(F)34x (16 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00044F$_H$-000457$_H$	Reserved			-
000458$_H$	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459$_H$	I/O Port P01 - Port Input Level Register	PILR01		R/W
00045A$_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
00045B$_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
00045C$_H$	I/O Port P04 - Port Input Level Register	PILR04		R/W
00045D$_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
00045E$_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
00045F$_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460$_H$	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461$_H$	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462$_H$	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463$_H$-00046B$_H$	Reserved			-
00046C$_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
00046D$_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
00046E$_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
00046F$_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470$_H$	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471$_H$	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472$_H$	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473$_H$	I/O Port P07 - Extended Port Input Level Register	EPILR07		R/W
000474$_H$	I/O Port P08 - Extended Port Input Level Register	EPILR08		R/W
000475$_H$	I/O Port P09 - Extended Port Input Level Register	EPILR09		R/W
000476$_H$	I/O Port P10 - Extended Port Input Level Register	EPILR10		R/W
000477$_H$-00047F$_H$	Reserved			-
000480$_H$	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481$_H$	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482$_H$	I/O Port P02 - Port Output Drive Register	PODR02		R/W

I/O map MB96(F)34x (23 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005A9H	PPG13 - Duty cycle register			W
0005AAH	PPG13 - Control status register Low	PCNL13	PCN13	R/W
0005ABH	PPG13 - Control status register High	PCNH13		R/W
0005ACH	PPG14 - Timer register		PTMR14	R
0005ADH	PPG14 - Timer register			R
0005AEH	PPG14 - Period setting register		PCSR14	W
0005AFH	PPG14 - Period setting register			W
0005B0H	PPG14 - Duty cycle register		PDUT14	W
0005B1H	PPG14 - Duty cycle register			W
0005B2H	PPG14 - Control status register Low	PCNL14	PCN14	R/W
0005B3H	PPG14 - Control status register High	PCNH14		R/W
0005B4H	PPG15 - Timer register		PTMR15	R
0005B5H	PPG15 - Timer register			R
0005B6H	PPG15 - Period setting register		PCSR15	W
0005B7H	PPG15 - Period setting register			W
0005B8H	PPG15 - Duty cycle register		PDUT15	W
0005B9H	PPG15 - Duty cycle register			W
0005BAH	PPG15 - Control status register Low	PCNL15	PCN15	R/W
0005BBH	PPG15 - Control status register High	PCNH15		R/W
0005BCH-00065FH	Reserved			-
000660H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663H	Peripheral Resource Relocation Register 13	PRRR13		W
000664H-0006DFH	Reserved			-
0006E0H	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
0006E1H	External Bus - Area configuration register 0 High	EACH0		R/W
0006E2H	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
0006E3H	External Bus - Area configuration register 1 High	EACH1		R/W

I/O map MB96(F)34x (26 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000740H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
00074AH	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
00074BH	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
00074CH	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
00074DH	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W
00074EH	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	R/W
00074FH	CAN0 - IF2 Data A1 High	IF2DTA1H0		R/W
000750H	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	R/W
000751H	CAN0 - IF2 Data A2 High	IF2DTA2H0		R/W
000752H	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	R/W
000753H	CAN0 - IF2 Data B1 High	IF2DTB1H0		R/W
000754H	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	R/W
000755H	CAN0 - IF2 Data B2 High	IF2DTB2H0		R/W
000756H-00077FH	Reserved			-
000780H	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781H	CAN0 - Transmission Request 1 Register High	TREQR1H0		R
000782H	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783H	CAN0 - Transmission Request 2 Register High	TREQR2H0		R
000784H-00078FH	Reserved			-

Interrupt vector table MB96(F)34x (3 of 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
55	320H	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG
56	31CH	ICU0	Yes	56	Input Capture Unit 0
57	318H	ICU1	Yes	57	Input Capture Unit 1
58	314H	ICU2	Yes	58	Input Capture Unit 2
59	310H	ICU3	Yes	59	Input Capture Unit 3
60	30CH	ICU4	Yes	60	Input Capture Unit 4
61	308H	ICU5	Yes	61	Input Capture Unit 5
62	304H	ICU6	Yes	62	Input Capture Unit 6
63	300H	ICU7	Yes	63	Input Capture Unit 7
64	2FCH	OCU0	Yes	64	Output Compare Unit 0
65	2F8H	OCU1	Yes	65	Output Compare Unit 1
66	2F4H	OCU2	Yes	66	Output Compare Unit 2
67	2F0H	OCU3	Yes	67	Output Compare Unit 3
68	2ECH	OCU4	Yes	68	Output Compare Unit 4
69	2E8H	OCU5	Yes	69	Output Compare Unit 5
70	2E4H	OCU6	Yes	70	Output Compare Unit 6
71	2E0H	OCU7	Yes	71	Output Compare Unit 7
72	2DCH	FRT0	Yes	72	Free Running Timer 0
73	2D8H	FRT1	Yes	73	Free Running Timer 1
74	2D4H	IIC0	Yes	74	I2C interface
75	2D0H	IIC1	Yes	75	I2C interface
76	2CCH	ADC0	Yes	76	A/D Converter
77	2C8H	ALARM0	No	77	Alarm Comparator 0 (except MB96F345Dyy or MB96F345Fyy)
78	2C4H	ALARM1	No	78	Alarm Comparator 1 (except MB96F345Dyy or MB96F345Fyy)
79	2C0H	LINR0	Yes	79	LIN USART 0 RX
80	2BCH	LINT0	Yes	80	LIN USART 0 TX
81	2B8H	LINR1	Yes	81	LIN USART 1 RX
82	2B4H	LINT1	Yes	82	LIN USART 1 TX

3. DC characteristics

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in MB96F345
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	Not available in MB96F345
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in MB96F34xY/R/AxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in MB96F345
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	Not available in MB96F345
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in MB96F34xY/R/AxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	

Internal Clock timing

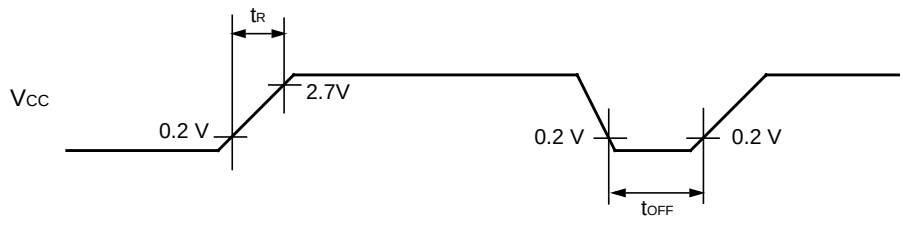
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	86	0	96	MHz	MB96F348T/H/CxB/C
		0	72	0	80	MHz	MB96F345
		0	68	0	74	MHz	MB96F34xY/R/Axx
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	Others than below
		0	36	0	40	MHz	MB96F345
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	Others than below
		0	26	0	28	MHz	MB96F34xY/R/Axx

Power On Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

I²C Timing

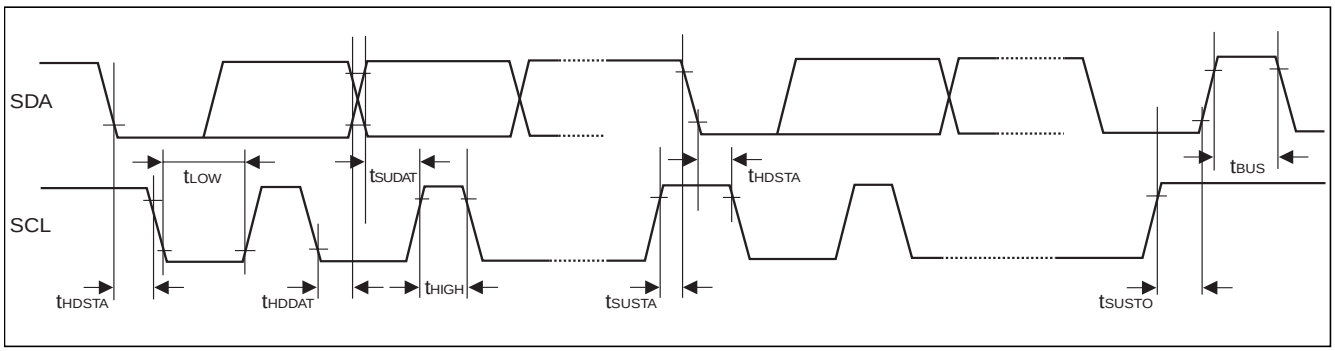
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V,V_{SS} = AV_{SS} =0V)

Parameter	Symbol	Standard-mode		Fast-mode*1		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}	4.0	—	0.6	—	µs
“L” width of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
“H” width of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}	4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}	0	3.45	0	0.9	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}	250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}	4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}	4.7	—	1.3	—	µs
Output fall time from 0.7*Vcc to 0.3*Vcc with a bus capacitance from 10 pF to 400 pF	t_{of}	20 + 0.1*C_b *2	250	20 + 0.1*C_b *2	250	ns
Capacitive load for each bus line	C_b	—	400	—	400	pF
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	n/a	n/a	0	1*t_{CLKP1}*3	ns

*1 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.

*2 : C_b = capacitance of one bus line in pF.

*3 : t_{CLKP1} is the cycle time of the periperal clock CLKP1.



- V_{OH} = 0.7 * V_{CC}
- V_{OL} = 0.3 * V_{CC}
- CMOS Hysteresis 0.7/0.3 input selected

5. Analog Digital Converter

(T_A = -40 ˚C to +125 ˚C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-	-	± 3	LSB	
Nonlinearity error	-	-	-	-	± 2.5	LSB	
Differential nonlinearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	AVRL - 1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale transition voltage	V_{FST}	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog input leakage current (during conversion)	I_{AIN}	ANn	-1	-	+1	µA	T_A ≤ 105 ˚C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-1.2	-	+1.2	µA	105 ˚C < T_A ≤ 125 ˚C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRH2	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

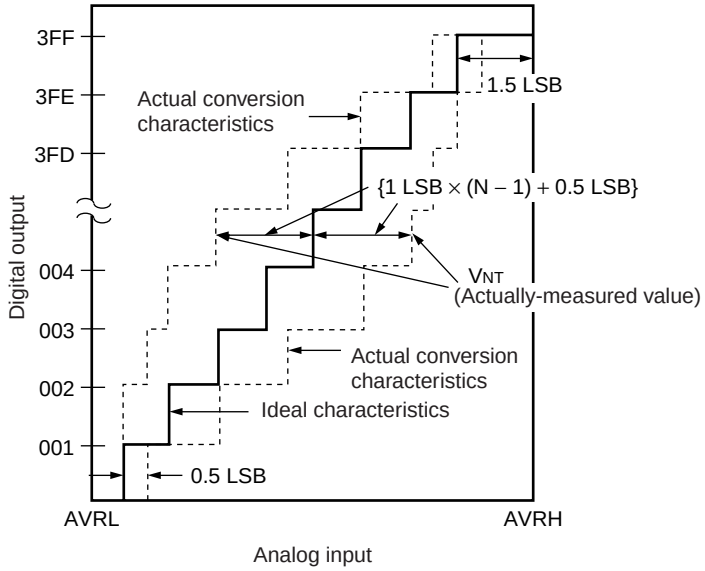
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

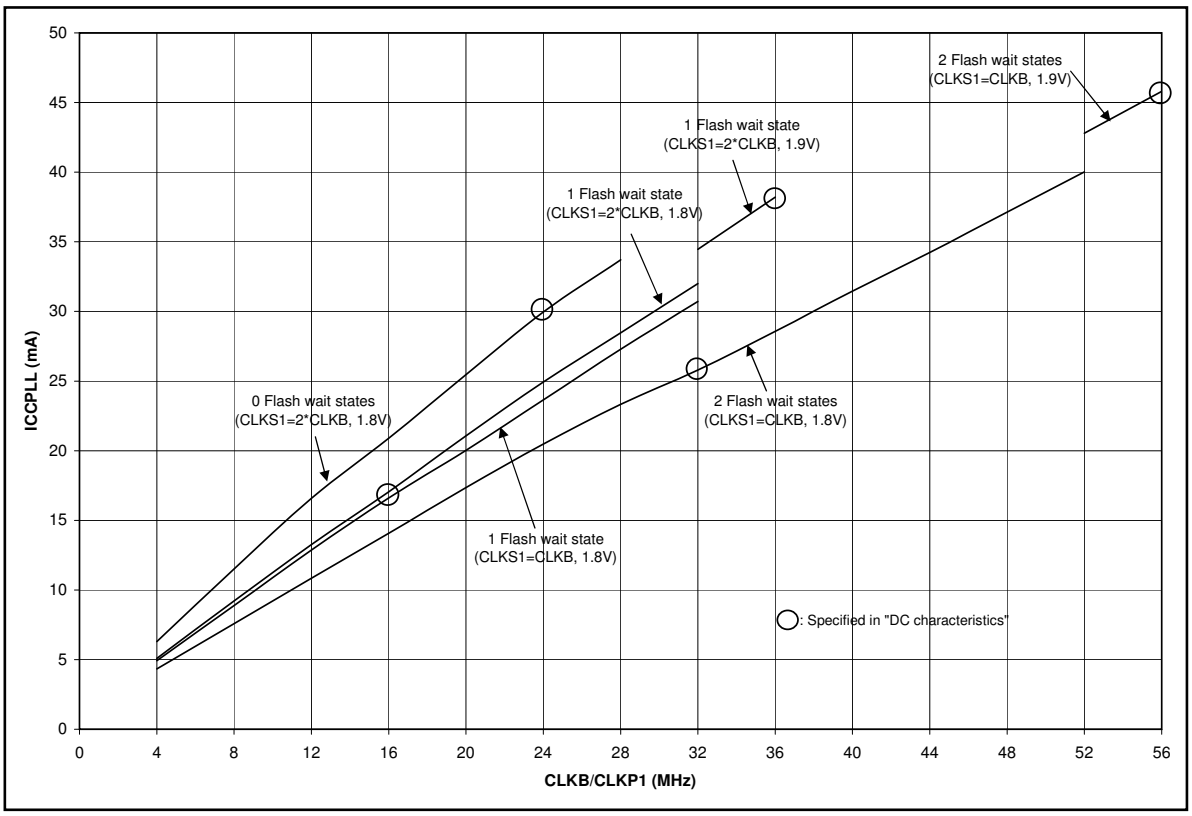
V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

6. Alarm Comparator

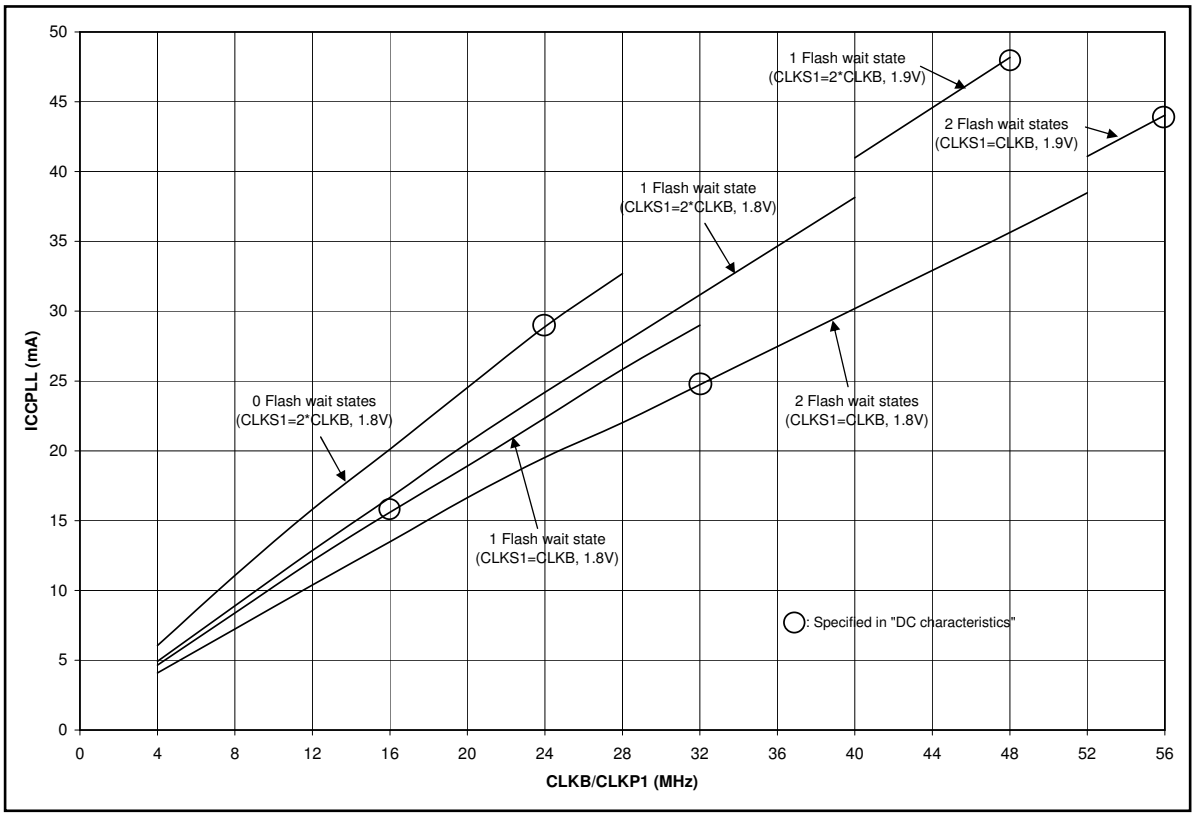
(T_A = -40 ˚C to +125 ˚C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	µA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	µA	T_A = 25 ˚C
			-3	-	+3	µA	T_A = 125 ˚C
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		0.36 * AV_{CC} -0.25	0.36 * AV_{CC} -0.1	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$		-	0.36 * AV_{CC} +0.1	0.36 * AV_{CC} +0.25	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		0.78 * AV_{CC} -0.25	0.78 * AV_{CC} -0.1	-	V	
External high threshold low->high transition	$V_{EVTH(L->H)}$			0.78 * AV_{CC} +0.1	0.78 * AV_{CC} +0.25	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	µs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	µs	CMD = 0 (slow)
Power-up stabilization time after enabling alarm comparator	t_{PD}		-	1	10	ms	Threshold levels specified above are not guaranteed within this time
Slow/Fast mode transition time	t_{CMD}		-	100	500	µs	

MB96F346/F347/F348Y/R/A PLL Run mode currents



MB96F348T/H/C PLL Run mode currents



MCU without CAN controller

Part number	Flash/ROM	Subclock	Package
MB96F346ASB PQC-GSE2	Flash A (288KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F346AWB PQC-GSE2		Yes	
MB96F346ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346AWB PMC-GSE2		Yes	
MB96F346ASC PQC-GSE2*1		No	100 pin Plastic QFP (FPT-100P-M22)
MB96F346AWC PQC-GSE2*1		Yes	
MB96F346ASC PMC-GSE2*1		No	
MB96F346AWC PMC-GSE2*1		Yes	
MB96F347ASB PQC-GSE2	Flash A (416KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F347AWB PQC-GSE2		Yes	
MB96F347ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F347AWB PMC-GSE2		Yes	
MB96F347ASC PQC-GSE2*1		No	100 pin Plastic QFP (FPT-100P-M22)
MB96F347AWC PQC-GSE2*1		Yes	
MB96F347ASC PMC-GSE2*1		No	
MB96F347AWC PMC-GSE2*1		Yes	
MB96F348ASB PQC-GSE2	Flash A (544KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F348AWB PQC-GSE2		Yes	
MB96F348ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348AWB PMC-GSE2		Yes	
MB96F348ASC PQC-GSE2*1		No	100 pin Plastic QFP (FPT-100P-M22)
MB96F348AWC PQC-GSE2*1		Yes	
MB96F348ASC PMC-GSE2*1		No	
MB96F348AWC PMC-GSE2*1		Yes	
MB96F348CSC PQC-GSE2	Flash A (544KB) Flash B (32KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F348CWC PQC-GSE2		Yes	
MB96F348CSC PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348CWC PMC-GSE2		Yes	

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

This datasheet is also valid for the following outdated devices:

MB96F346YSA, MB96F346RSA, MB96F346YWA, MB96F346RWA,
MB96F347YSA, MB96F347RSA, MB96F347YWA, MB96F347RWA,
MB96F348YSA, MB96F348RSA, MB96F348YWA, MB96F348RWA,
MB96F348TSB, MB96F348HSB, MB96F348TWB, MB96F348HWB,